ANALOG DEVICES

SoundComm Controller

AD1815

FEATURES

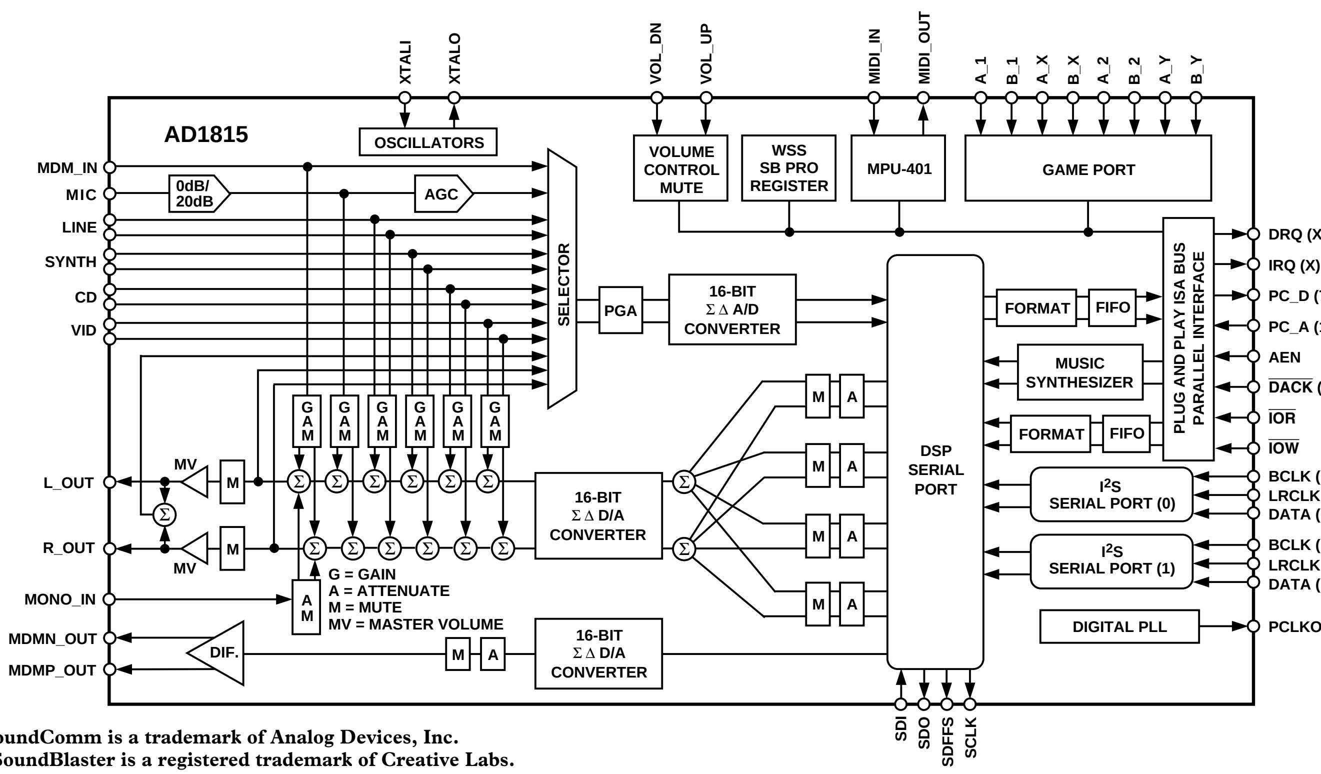
- Supports Applications Written for SoundBlaster* Pro, AdLib/OPL3† Win 3.1, Win 95
- Stereo Audio 16-Bit ΣΔ Codec
- MPC Level-2/3 Mixer
- ISA Plug and Play Compatible
- Dual Type F FIFO DMA Support
- MPU-401 Compatible MIDI Port
- Integrated V.34, Modem Analog Front End
- Integrated Enhanced Digital Game Port
- Supports Wavetable Synthesizers
- Two I²S Digital Audio Serial Port Inputs
- Software & Hardware Volume Control
- Integrated FM Compatible Music Synthesizer
- Full-Duplex Capture and Playback Operation at Different Sample Rates
- Supports Up to Six Different Sample Rates Simultaneously
- Supports Voice Over Data
- 1 Hz Resolution Programmable Sample Rates from 4 kHz to 55.2 kHz
- Bidirectional DSP Serial Port
- Power Management Modes
- Operation from +5 V Supply
- Built-In 24 mA Bus Drivers
- 100-Pin PQFP Package

PRODUCT OVERVIEW

The AD1815 SoundComm™ Controller is a single chip Plug and Play audio subsystem for adding 16-bit stereo audio and communications support to personal computers. The AD1815 is compatible with applications written for SoundBlaster Pro and AdLib/OPL3. The AD1815 provides an integrated audio solution for Windows 95, Windows 3.1, DirectSound‡ and multimedia applications. The AD1815 supports telephony and advanced audio applications by providing a V.34 compatible modem analog front end and a serial port linking a companion media pump or DSP to the subsystem.

The AD1815 on-chip Plug and Play hardware provides configuration services for all integrated logical devices.

FUNCTIONAL BLOCK DIAGRAM



SoundComm is a trademark of Analog Devices, Inc.
*SoundBlaster is a registered trademark of Creative Labs.
†AdLib is a trademark of AdLib Multimedia and OPL is a registered trademark of Yamaha Corporation.
‡DirectSound is a trademark of Microsoft Corp.

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STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	5.0	V
Analog Supply (V_{CC})	5.0	V
Sample Rate (F_S)		
Audio	48	kHz
Modem	12.8	kHz
Input Signal	1008	Hz
Audio Output Passband	20 Hz to 20 kHz	
Modem Output Passband	400 Hz to 4.2 kHz	
V_{IH}	5.0	V
V_{IL}	0	V

DAC Test Conditions
Calibrated
0 dB Attenuation
Input Full Scale
16-Bit Linear Mode
100 kΩ Output Load
Mute Off
Measured at Line Output

ADC Test Conditions
Calibrated
0 dB Gain
Input –1.0 dB Relative to Full Scale
Line Input Selected
16-Bit Linear Mode

ANALOG INPUT

Parameter	Min	Typ	Max	Units
Full-Scale Input Voltage (RMS Values Assume Sine Wave Input)				
MONO_IN, LINE, SYNTH, CD, VID		1		V rms
		2.83		V p-p
MDM_IN		3.156		V p-p
MIC with +20 dB Gain (MGE = 1)		0.1		V rms
		0.283		V p-p
MIC with 0 dB Gain (MGE = 0)		1		V rms
		2.83		V p-p
Input Impedance*		17		kΩ
Input Capacitance*		15		pF

PROGRAMMABLE GAIN AMPLIFIER—ADC

Parameter	Min	Typ	Max	Units
Step Size (0 dB to 22.5 dB) (All Steps Tested)	1.3	1.5	1.7	dB
PGA Gain Range Span	21.5	22.5	23.5	dB

CD, LINE, MICROPHONE, MODEM, SYNTHESIZER, AND VIDEO INPUT ANALOG GAIN/ AMPLIFIERS/ATTENUATORS

Parameter	Min	Typ	Max	Units
CD, LINE, MIC, SYNTH, VID, MDM_IN				
Step Size: (All Steps Tested)				
+12 dB to –31.5 dB	1.3	1.5	1.7	dB
–33 dB to –34.5 dB	1.0	1.5	2.0	dB
Input Gain/Attenuation Range	45.5	46.5	47.5	dB
MONO_IN				
Step Size 0 dB to –45 dB: (All Steps Tested)	2.6	3.0	3.4	dB
Input Gain/Attenuation Range	43	45	46	dB

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

Parameter	Min	Typ	Max	Units
Audio Passband	0		$0.4 \times F_S$	Hz
Audio Passband Ripple			±0.09	dB
Audio Transition Band	$0.4 \times F_S$		$0.6 \times F_S$	Hz
Audio Stopband	$0.6 \times F_S$		∞	Hz
Audio Stopband Rejection	82			dB
Modem Passband	0		$0.4 \times F_S$	Hz
Modem Passband Ripple			±0.2	dB
Modem Transition Band	$0.442 \times F_S$		$0.542 \times F_S$	Hz
Modem Stopband	$0.542 \times F_S$		∞	Hz
Modem Stopband Rejection (3 dB Roll Off After Stop Band Edge)	78			dB
Audio Group Delay			$12/F_S$	sec
Modem Group Delay			$18/F_S$	sec
Group Delay Variation Over Passband			0.0	µs

ANALOG-TO-DIGITAL CONVERTERS

Parameter	Min	Typ	Max	Units
Resolution		16		Bits
Audio Dynamic Range (–60 dB Input THD+N Referenced to Full-Scale, A-Weighted)	80	82		dB
Audio THD+N (Referenced to Full Scale)			0.036	%
		–74	–70	dB
Modem Dynamic Range (–60 dB Input THD+N Referenced to Full Scale, F_S = 12.8 kHz)	85	89		dB
Modem THD+N (Referenced to Full Scale, F_S = 12.8 kHz)			0.025	%
		–75	–72	dB
Signal-to-Intermodulation Distortion* (CCIF Method)		85		dB
ADC Crosstalk*				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L Read L)		–90	–80	dB
Line to MIC (Input LINE, Ground and Select MIC, Read ADC)		–90	–80	dB
Line to SYNTH		–90	–80	dB
Line to CD		–90	–80	dB
Line to VID		–90	–80	dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±1	dB
ADC Offset Error			±5	mV

DIGITAL-TO-ANALOG CONVERTERS

Parameter	Min	Typ	Max	Units
Resolution		16		Bits
Audio Dynamic Range (–60 dB Input THD+N Referenced to Full Scale, A-Weighted)	80	82		dB
Audio THD+N (Referenced to Full Scale)			0.020	%
		–78	–74	dB
Modem Dynamic Range (–60 dB Input THD+N Referenced to Full Scale, 4.2 kHz Analog Output Passband, Differential Output F_S = 12.8 kHz)	82	88		dB
Modem THD+N (Referenced to Full Scale, F_S = 12.8 kHz, Differential Output 4.2 kHz Analog Passband)			0.008	%
		–88	–82	dB
Signal-to-Intermodulation Distortion* (CCIF Method)		90		dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
DAC Crosstalk* (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			–80	dB
Total Out-of-Band Energy (Measured from 0.6 × F_S to 100 kHz at L-OUT and R_OUT)*			–45	dB
Audible Out-of-Band Energy (Measured from 0.6 × F_S to 20 kHz at L-OUT and R_OUT)*			–75	dB

MASTER VOLUME & MODEM ATTENUATOR

Parameter	Min	Typ	Max	Units
Master Volume Step Size (0 dB to –22.5 dB)	1.3	1.5	1.7	dB
Master Volume Step Size (–22.5 dB to –46.5 dB)	1.0	1.5	2.0	dB
Master Volume Output Attenuation Range Span	45.5	46.5	47.5	dB
Modem Volume Step Size (0 dB to –31 dB)	0.8	1.0	1.2	dB
Modem Attenuation Range	30	31	32	dB
Mute Attenuation of 0 dB Fundamental*	80			dB

DIGITAL MIX ATTENUATORS

Parameter	Min	Typ	Max	Units
Step Size: I^2S (0), I^2S (1), Music, ISA*		1.505		dB
Digital Mix Attenuation Range Span*		94.8		dB

ANALOG OUTPUT

Parameter	Min	Typ	Max	Units
Full-Scale Output Voltage (at L_OUT and R_OUT)		2.8		V p-p
Full-Scale Output Voltage MDMN_OUT (at MDMN_OUT, MDMP_OUT; Differential)		6.312		V p-p
Output Impedance*			800	Ω
External Load Impedance*	10			kΩ
Output Capacitance*		15		pF
External Load Capacitance			100	pF
V_{REFX}*	2.10	2.25	2.40	V
V_{REFX} Current Drive*		100		µA
V_{REFX} Output Impedance*		6.5		kΩ
Mute Click (Muted Analog Mixers), Muted Output Minus Unmuted Output at 0 dB*		±5		mV

SYSTEM SPECIFICATIONS*

Parameter	Min	Typ	Max	Units
System Frequency Response Ripple (Line In to Line Out)			1.0	dB
Differential Nonlinearity			±1	LSB
Phase Linearity Deviation			5	Degrees

STATIC DIGITAL SPECIFICATIONS

Parameter	Min	Typ	Max	Units
High Level Input Voltage (V_{IH})	2			V
XTALI	2.4			V
Low Level Input Voltage (V_{IL})			0.8	V
High Level Output Voltage (V_{OH}), I_{OH} = 8 mA†	2.4			V
Low Level Output Voltage (V_{OL}), I_{OL} = 8 mA	0.4			V
Input Leakage Current	–10		+10	µA
Output Leakage Current	–10		+10	µA

POWER SUPPLY

Parameter	Min	Typ	Max	Units
Power Supply Range—Analog	4.75		5.25	V
Power Supply Range—Digital	4.75		5.25	V
Power Supply Current			193	mA
Power Dissipation			965	mW
Analog Supply Current			35	mA
Digital Supply Current			158	mA
Analog Power Supply Current—Powerdown			2	mA
Digital Power Supply Current—Powerdown			23	mA
Analog Power Supply Current—RESET			0.2	mA
Digital Power Supply Current—RESET			10	mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)* (At Both Analog and Digital Supply Pins, Both ADCs and DACs)		40		dB

CLOCK SPECIFICATIONS*

Parameter	Min	Typ	Max	Units
Input Clock Frequency		33		MHz
Recommended Clock Duty Cycle	25	50	75	%
Power Up Initialization Time			500	ms

TIMING PARAMETERS (Guaranteed Over Operating Temperature Range)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{IOW}/\overline{IOR}$ Strobe Width	t_{STW}	100			ns
$\overline{IOW}/\overline{IOR}$ Rising to $\overline{IOW}/\overline{IOR}$ Falling	t_{BWDN}	80			ns
Write Data Setup to $\overline{IOW}$ Rising	t_{WDSU}	10			ns
$\overline{IOW}$ Falling to Valid Read Data	t_{RDDV}			40	ns
AEN Setup to $\overline{IOW}/\overline{IOR}$ Falling	t_{AESU}	10			ns
AEN Hold from $\overline{IOW}/\overline{IOR}$ Rising	t_{AEHD}	0			ns
Adr Setup to $\overline{IOW}/\overline{IOR}$ Falling	t_{ADSU}	10			ns
Adr Hold from $\overline{IOW}/\overline{IOR}$ Rising	t_{ADHD}	0			ns
$\overline{DACK}$ Rising to $\overline{IOW}/\overline{IOR}$ Falling	t_{DKSU}	20			ns
Data Hold from $\overline{IOR}$ Rising	t_{DHD1}			20	ns
Data Hold from $\overline{IOW}$ Rising	t_{DHD2}	15			ns
DRQ Hold from $\overline{IOW}/\overline{IOR}$ Falling	t_{DRHD}			25	ns
$\overline{DACK}$ Hold from $\overline{IOW}/\overline{IOR}$ Rising	t_{DKHD}	10			ns
Data [SDI] Input Setup Time to SCLK*	t_S	10			ns
Data [SDI] Input Hold Time from SCLK*	t_H	10			ns
Frame Sync [SDFS] HI Pulse Width*	t_{FSW}		80		ns
Clock [SCLK] to Frame Sync [SDFS] Propagation Delay*	t_{PD}			15	ns
Clock [SCLK] to Output Data [SDO] Valid*	t_{DV}			15	ns
$\overline{RESET}$ Pulse Width	t_{RPWL}	100			ns
BCLK HI Pulse Width	t_{DBH}	25			ns
BCLK LO Pulse Width	t_{DBL}	25			ns
BCLK Period	t_{DBP}	50			ns
LRCLK Setup	t_{DLS}	5			ns
SDATA Setup	t_{DDS}	2			ns
SDATA Hold	t_{DDH}	5			ns

NOTES
*Guaranteed, not tested.
†(All ISA pins MIDI_OUT IOL = 24 mA. Refer to pin description for individual output drive levels.

Specifications subject to change without notice.

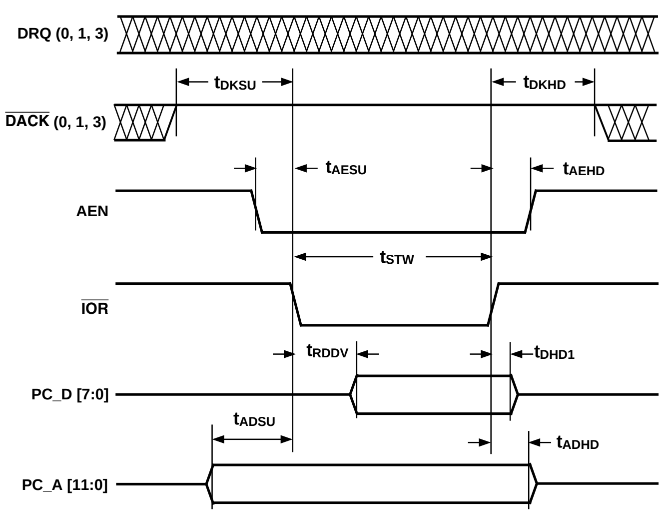


Figure 1. PIO Read Cycle

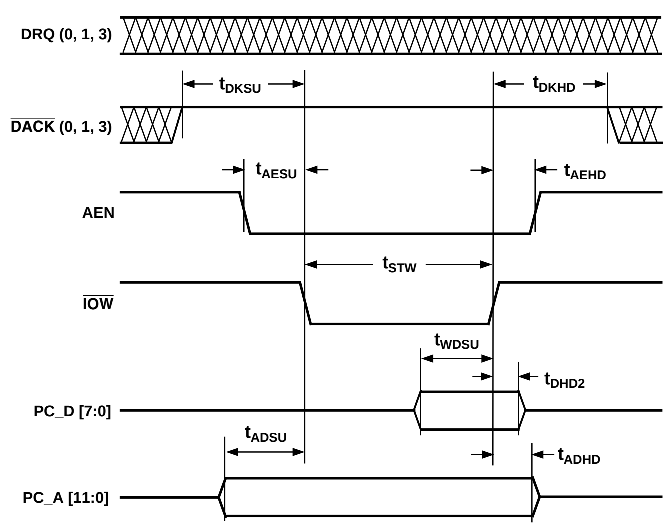


Figure 2. PIO Write Cycle

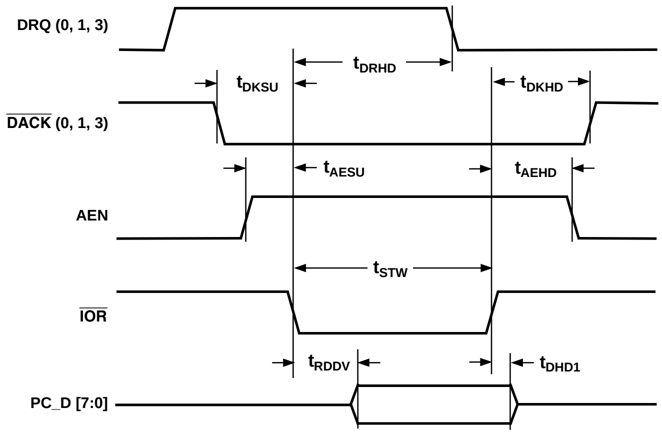


Figure 3. DMA Read Cycle

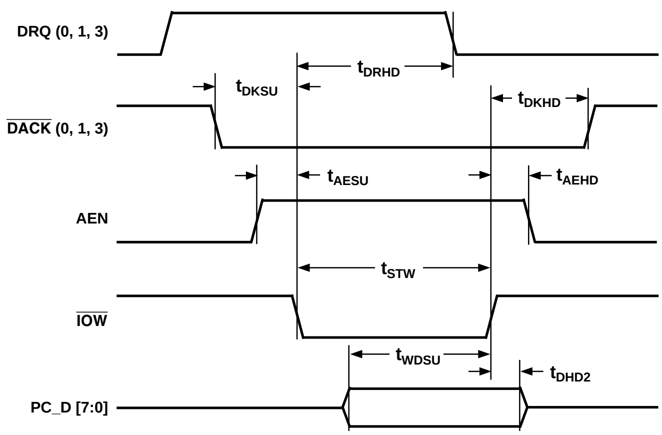


Figure 4. DMA Write Cycle

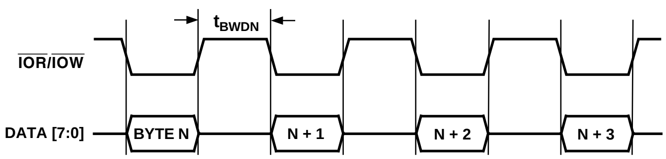


Figure 5. Codec Transfers

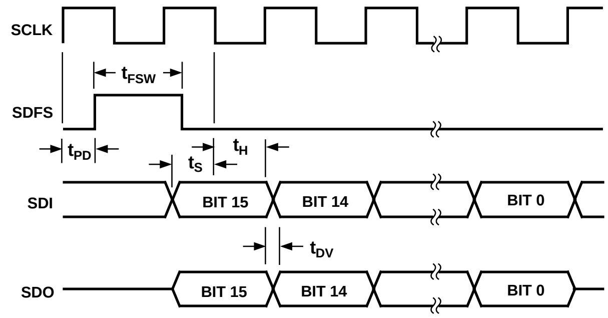


Figure 6. DSP Port Timing

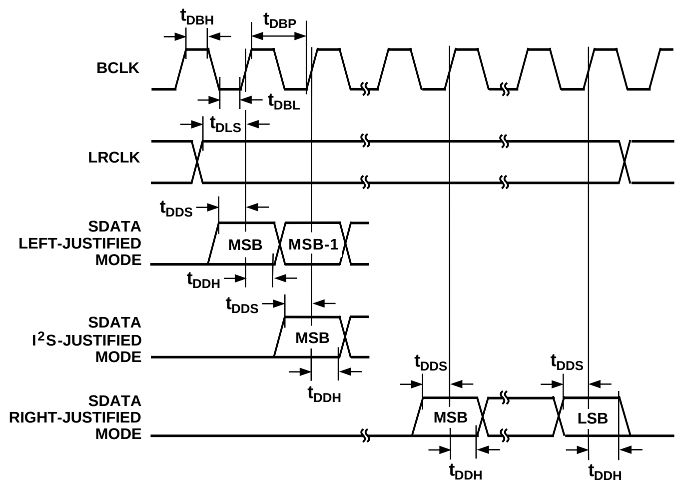


Figure 7. I^2S Serial Port Timing

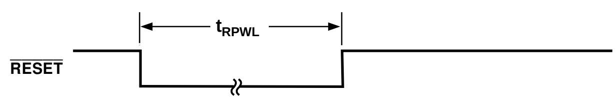


Figure 8. Reset Pulse Width

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Units
Power Supplies			
Digital (V_{DD})	–0.3	6.0	V
Analog (V_{CC})	–0.3	6.0	V
Input Current (Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	–0.3	V_{CC} + 0.3	V
Digital Input Voltage (Signal Pins)	–0.3	V_{DD} + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	–65	+150	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$

T_{CASE} = Case Temperature in °C

PD = Power Dissipation in W

θ_{CA} = Thermal Resistance (Case-to-Ambient)

θ_{JA} = Thermal Resistance (Junction-to-Ambient)

θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PQFP	77°C	7°C	70°C

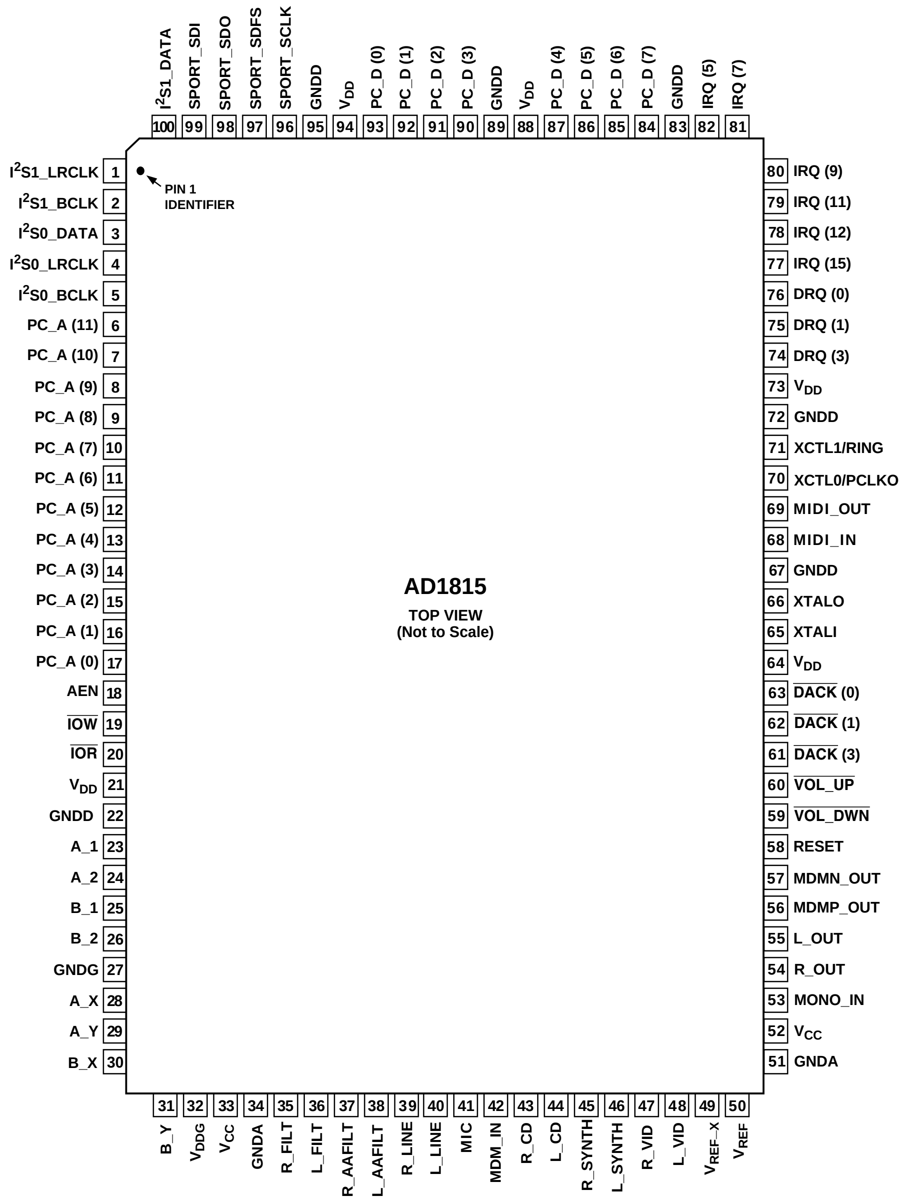
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1815JS	0°C to +70°C	100-Lead PQFP	S-100

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1815 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Analog Signals

Pin Name	PQFP	I/O	Description
MDM_IN	42	I	Modem Input mono telephony signal from DAA. The input may be sent to the right channel of the ADC if the AD1815 is in modem mode; gained or attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with left and right line out (L_OUT and R_OUT).
MIC	41	I	Microphone Input. The MIC input may be either line-level or –20 dB from line-level (the difference being made up through a software controlled 20 dB gain block). The mono MIC input may be sent to the left and right channel of the ADC for conversion, or gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with left and right line out (L_OUT and R_OUT), before the Master Volume stage.
L_LINE	40	I	Left Line-Level Input. The left line-level input may be: sent to the left channel of the ADC; gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with left line out (L_OUT).
R_LINE	39	I	Right Line-Level Input. The right line-level input may be: sent to the right channel of the ADC; gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with right line out (R_OUT).
L_SYNTH	46	I	Left Synthesizer Input. The left MIDI upgrade line-level input may be: sent to the left channel of the ADC; gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with left line out (L_OUT).
R_SYNTH	45	I	Right Synthesizer Input. The right MIDI upgrade line-level input may be: sent to the right channel of the ADC; gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with right line out (R_OUT).
L_CD	44	I	Left CD Line-Level Input. The left CD line-level input may be: sent to the left channel of the ADC; gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with left line out (L_OUT).
R_CD	43	I	Right CD Line-Level Input. The right CD line-level input may be: sent to the right channel of the ADC; gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with right line out (R_OUT).
L_VID	48	I	Left Video Input. The left audio track for a video line-level input may be: sent to the left channel of the ADC; gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with left line out (L_OUT).
R_VID	47	I	Right Video Input. The right audio track for a video line-level input may be: sent to the right channel of the ADC; gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps and then summed with right line out (R_OUT).
L_OUT	55	O	Left Output. Left channel line-level post-mixed output. The final stage passes through the Master Volume block and may be attenuated 0 dB to –45 dB in 1.5 dB steps.
R_OUT	54	O	Right Output. Right channel line-level post-mixed output. The final stage passes through the Master Volume block and may be attenuated 0 dB to –45 dB in 1.5 dB steps.
MDMN_OUT	57	O	Differential Modem Output Negative.
MDMP_OUT	56	O	Differential Modem Output Positive.
MONO_IN	53	I	Mono Line-Level Input.

Parallel Interface (All Outputs are 24 mA Drivers)

Pin Name	PQFP	I/O	Description
PC_D[7:0]	84–87, 90–93	I/O	Bidirectional ISA Bus PC Data, 24 mA drive. Connects the AD1815 to the low byte data on the bus.
IRQ(x)	77–82	O	Host Interrupt Request, 24 mA drive. IRQ(5), IRQ(7), IRQ(9), IRQ(11), IRQ(12), IRQ(15). Active HI signals indicating a pending interrupt. These signals are always edge triggered, not level triggered.
DRQ(x)	74–76	O	DMA Request, 24 mA drive. DRQ(0), DRQ(1), DRQ(3). Active HI signals indicating a request for DMA bus operation.
PC_A[11:0]	6–17	I	ISA Bus PC Address. Connects the AD1815 to the ISA bus address lines.
AEN	18	I	Address Enable. Low signal indicates a PIO transfer.
$\overline{\text{DACK}}$ (x)	61–63	I	DMA Acknowledge. DACK(0), DACK(1), DACK(3). Active LO signal indicating that a DMA operation can begin.
$\overline{\text{IOR}}$	20	I	I/O Read. Active LO signal indicates a read operation.
$\overline{\text{IOW}}$	19	I	I/O Write. Active HI signal indicates a write operation.
RESET	58	I	Reset. Active HI.

Game Port

Pin Name	PQFP	I/O	Description
A_1	23	I	Game Port A, Button #1.
A_2	24	I	Game Port A, Button #2.
A_X	28	I	Game Port A, X-Axis.
A_Y	29	I	Game Port A, Y-Axis.
B_1	25	I	Game Port B, Button #1.
B_2	26	I	Game Port B, Button #2.
B_X	30	I	Game Port B, X-Axis.
B_Y	31	I	Game Port B, Y-Axis.

MIDI Interface Signal (24 mA Drivers)

Pin Name	PQFP	I/O	Description
MIDI_IN	68	I	RXD MIDI Input. This pin is typically connected to Pin 15 of the game port connector via an optoisolator.
MIDI_OUT	69	O	TXD MIDI Output. This pin is typically connected to Pin 12 of the game port connector to form a 5 mA current loop.

Serial Ports (8 mA Drivers)

Pin Name	PQFP	I/O	Description
I^2S0_BCLK	5	I	I^2S (0) Bit Clock.
I^2S0_LRCLK	4	I	I^2S (0) Left/Right Clock.
I^2S0_DATA	3	I	I^2S (0) Serial Data Input.
I^2S1_BCLK	2	I	I^2S (1) Bit Clock.
I^2S1_LRCLK	1	I	I^2S (1) Left/Right Clock.
I^2S1_DATA	100	I	I^2S (1) Serial Data Input.
SPORT_SDI	99	I	Serial Port Digital Serial Input.
SPORT_SCLK	96	O	Serial Port Serial Clock.
SPORT_SDFS	97	O	Serial Port Serial Data Frame Synchronization.
SPORT_SDO	98	O	Serial Port Serial Data Output.

Miscellaneous Analog Pins

Pin Name	PQFP	I/O	Description
V_{REF_X}	49	O	Voltage Reference. Nominal 2.25 volt reference available for dc-coupling and level-shifting. V_{REF_X} should not be used to sink or source signal current.
V_{REF}	50	I	Voltage Reference Filter. Voltage reference filter point for external bypassing only.
L_FILT	36	I	Left Channel Filter. Requires a 1.0 µF to analog ground for proper operation.
R_FILT	35	I	Right Channel Filter. Requires a 1.0 µF to analog ground for proper operation.
L_AAFILT	38	I	Left Channel Antialias Filter. This pin requires a 270 pF NPO capacitor to analog ground for proper operation.
R_AAFILT	37	I	Right Channel Antialias Filter. This pin requires a 270 pF NPO capacitor to analog ground for proper operation.

Crystal Pin

Pin Name	PQFP	I/O	Description
XTALO	66	O	33 MHz Crystal Output. If no Crystal is present leave XTALO unconnected.
XTALI	65	I	33 MHz Clock. When using a crystal as a clock source, the crystal should be connected between the XTALI and XTALO pins. Clock input may be driven into XTALI in place of a crystal. When using an external clock, V_{IH} must be 2.4 V rather than the V_{IH} of 2.0 V specified for all other digital inputs.

Hardware Volume Pins

Pin Name	PQFP	I/O	Description
$\overline{\text{VOL\_DWN}}$	59	I	Master Volume Down. Modifies output level on pins L_OUT and R_OUT. Contains a 10 kΩ internal pull-up resistor. When asserted LO, decreases Master Volume by 1.5 dB/sec. Must be asserted at least 25 ms to be recognized. When asserted simultaneously with VOL_UP, output is muted. Output level modification reflected in indirect register 0 × 29.
$\overline{\text{VOL\_UP}}$	60	I	Master Volume Up. Modifies output level on pins L_OUT and R_OUT. Contains a 10 kΩ internal pull-up resistor. When asserted LO, increases Master Volume by 1.5 dB/sec. Must be asserted at least 25 ms to be recognized. When asserted simultaneously with VOL_UP, output is muted. Output level modification reflected in indirect register 0 × 29.

Muxed Control Pins

Pin Name	PQFP	I/O	Description
XCTL0	70	O	External Control 0. The state of this pin (TTL HI or LO) is reflected in codec indexed register. This pin is an open drain driver.
PCLKO	70	O	Programmable Clock Output. This pin can be programmed to generate an output clock equal to F_S, 8 × F_S, 16 × F_S, 32 × F_S, 64 × F_S, 128 × F_S or 256 × F_S. MPEG decoders typically require a master clock of 256 × F_S for audio synchronization.
XCTL1	71	O	External Control 1. The state of this pin (TTL HI or LO) is reflected in codec indexed register. Open drain, 8 mA active 0.5 mA internal pull-up resistor.
RING	71	I	Ring Indicator. Used to accept the ring indicator flag from the DAA.

Power Supplies

Pin Name	PQFP	I/O	Description
V_{CC}	33, 52	I	Analog Supply Voltage (+5 V).
GNDA	34, 51	I	Analog Ground.
V_{DD}	21, 64, 73, 88, 94	I	Digital Supply Voltage (+5 V).
GNDD	22, 67, 72, 83, 89, 95	I	Digital Ground.
V_{DDG}	32	I	Game Port Digital Supply Voltage (+5 V).
GNDG	27	I	Game Port Digital Ground.

HOST INTERFACE

The AD1815 contains all necessary ISA bus interface logic on chip. This logic includes address decoding for all onboard resources, control and signal interpretation, DMA selection and control logic, IRQ selection and control logic, and all interface configuration logic.

The AD1815 supports a Type "F" DMA request/grant architecture for transferring data with the ISA bus through the 8-bit interface. The AD1815 also supports DACK preemption. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. The AD1815 includes dual DMA count registers for full-duplex operation enabling simultaneous capture and playback on separate DMA channels.

Codec Functional Description

The AD1815's full-duplex stereo codec supports business audio and multimedia applications. The codec includes stereo audio converters, complete on-chip filtering, MPC Level-2 and Level-3 compliant analog mixing, programmable gain and attenuation, a variable sample rate converter, extensive digital mixing, and FIFOs buffering the Plug and Play ISA bus interface.

Analog Inputs

The codec contains a stereo pair of ΣΔ analog-to-digital converters (ADC). Inputs to the ADC can be selected from the following analog signals: mono modem or telephony (MDM_IN), mono microphone (MIC), stereo line (LINE), external stereo synthesizer (SYNTH), stereo CD ROM (CD), stereo audio from a video source (VID), and post-mixed stereo or mono line output (OUT).

Analog Mixing

MDM_IN, MIC, MONO_IN, LINE, SYNTH, CD, and VID can be mixed in the analog domain with the stereo line OUT from the ΣΔ digital-to-analog converters (DAC). Each channel of the stereo analog inputs can be independently gained or attenuated from +12 dB to –34.5 dB in 1.5 dB steps. The summing path for the mono inputs (MDM_IN, MIC, and MONO_IN to line OUT) duplicates mono channel data on both the left and right line OUT which can also be gained or attenuated from +12 dB to –34.5 dB in 1.5 dB steps for MDM_IN and MIC, and +0 dB to –45.5 dB in 3 dB steps for MONO_IN. The left and right mono summing signals are always identical being gained or attenuated equally.

Analog-to-Digital Datapath

The selector sends left and right channel information to the programmable gain amplifier (PGA). The PGA following the selector allows independent gain for each channel entering the ADC from 0 dB to 22.5 dB in 1.5 dB steps.

When the modem converters are enabled, each channel of the ADC is independent and can process left and right channel data at different sample rates. The right channel of the ADC samples modem information received from the DAA in the programmable range between 4 kHz and 13.8 kHz. All programmed sample rates have a resolution of 1 Hz. The AD1815 also supports the following irrational V.34 sample rates: 8/7 × 7,200 Hz, 8/7 × 9,000 Hz, and 8/7 × 12,000 Hz.

For supporting time correlated I/O echo cancellation, the ADC is capable of sampling microphone data on the left channel and the mono summation of left and right OUT on the right channel.

The codec can operate either in global stereo mode or in a global mono mode with left channel inputs appearing at both channels of the 16-bit ΣΔ converters. Data can be sampled at the programmed sampling frequency (from 4 kHz to 55.2 kHz with 1 Hz resolution).

Digital Mixing & Sample Rates

The audio ADC sample rate and the audio DAC sample rates are completely independent. The AD1815 includes a variable sample rate converter that lets the codec instantaneously change and process sample rates from 4 kHz to 55.2 kHz with a resolution of 1 Hz. The in-band integrated noise and distortion artifacts introduced by rate conversions are below –90 dB. When the modem converters are enabled, the right channel of the ADC and the modem DAC convert modem data at the same sample rate.

Up to four channels of digital data can be summed together and presented to the stereo DAC for conversion. Each digital channel pair can contain information encoded at a different sample rate. For example, 8 kHz .wav data received from the ISA interface, 48 kHz MPEG audio data received from $I^2S(0)$, digital 44.1 kHz CD data received from $I^2S(1)$, and internally generated 22.05 kHz music data may be summed together and then converted by the DACs.

Digital-to-Analog Datapath

The internally generated music synthesizer data, PCM data received from the ISA interface, data received from the $I^2S(0)$ port, and data received from the $I^2S(1)$ port, and the DSP serial port passes through an attenuation mute stage. The attenuator allows independent control over each digital channel which can be attenuated from 0 dB to –94.5 dB in 1.5 dB steps before being summed together and passed to the DAC or the channel may be muted entirely.

Analog Outputs

The analog output of the DAC can be summed with any of the analog input signals. The summed analog signal enters the Master Volume stage where each channel of the line OUT can be attenuated from 0 dB to –46.5 dB in 1.5 dB steps or muted.

Digital Data Types

The codec can process 16-bit twos-complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit µ-law or A-law companded digital data as specified in the control registers. The AD1815 also supports ADPCM encoded in the Creative SoundBlaster ADPCM formats.

Host-Based Echo Cancellation Support

The AD1815 supports time correlated I/O data format by presenting MIC data on the left channel of the ADC and the mono summation of left and right OUT on the right channel. The ADC sample rates are independent of the DAC sample rate allowing the AD1815 to support ADC time correlated I/O data at 8 kHz and DAC data at any other sample rate in the range of 4 kHz to 55.2 kHz simultaneously.

Telephony Modem Support

AD1815 contains a V.34 capable analog front end for supporting host-based and data pump modems. The modem DAC typical dynamic range is 90 dB over a 4.2 kHz analog output passband. In modem mode, the right channel of the ADC and a dedicated DAC convert modem data at the same sample rate in the range between 4 kHz and 13.8 kHz. All programmed sample rates have a 1 Hz resolution. The AD1815 also supports the following irrational V.34 sample rates:

$8/7 \times 7{,}200$ Hz, $8/7 \times 9{,}000$ Hz, and $8/7 \times 12{,}000$ Hz

For native modem applications, all modem processing is handled by the host and all data is transferred by PIO over the ISA interface through a 4 deep FIFO.

For modem applications using a dedicated data pump, a bi-directional DSP serial port interfaces directly to the data pump.

WSS & SoundBlaster Compatibility

Windows Sound System software audio compatibility is built into the AD1815.

SoundBlaster emulation is provided through the SoundBlaster register set and the internal music synthesizer. SoundBlaster Pro version 2.01 functions are supported including record and Creative SoundBlaster ADPCM.

Virtually all applications developed for SoundBlaster, Windows Sound System, AdLib, and MIDI MPU-401 platforms run on the AD1815 SoundComm Controller. Follow the same development process for the controller as you would use for these other devices. This section provides information on related development kits, hardware/software specifications, and reference texts.

As the AD1815 contains SoundBlaster (compatible) and Windows Sound System logical devices. You may find the following related development kits useful when developing AD1815 applications.

Developer Kit for SoundBlaster Series, 2nd ed. © 1993, Creative Labs, Inc., 1901 McCarthy Blvd., Milpitas, CA 95035

Microsoft Windows Sound System Driver Development Kit (*CD*), Version 2.0, © 1993, Microsoft Corp., One Microsoft Way, Redmond, WA 98052

Because the AD1815 complies with the following related specifications, you can use them as an additional reference to AD1815 operations beyond the material in this data sheet.

Plug & Play ISA Specification, Version 1.0a, © 1993, 1994, Intel Corp. & Microsoft Corp., One Microsoft Way, Redmond, WA 98052

Multimedia PC Level 2 Specification, © 1993, Multimedia PC Marketing Council, 1730 M St. NW, Suite 707, Washington, DC 20036

MIDI 1.0 Detailed Specification & Standard MIDI Files 1.0, © 1994, MIDI Manufacturers Association, PO Box 3173 La Habra, CA 90632-3173

Recommendation G.711-Pulse Code Modulation (PCM) Of Voice Frequencies (μ-Law & A-Law Companding), The International Telegraph and Telephone Consultative Committee IX Plenary Assembly Blue Book, Volume III - Fascicle III.4, General Aspects Of Digital Transmission Systems; Terminal Equipment's, Recommendations G.700 - G.795, (Geneva, 1988), ISBN 92-61-03341-5

IMA Digital Audio Doc-Pac (IMA-ADPCM), © 1992, Interactive Multimedia Association, 48 Maryland Avenue, Suite 202, Annapolis, MD 21401-8011

The following reference texts can serve as additional sources of information on developing applications that run on the AD1815.

S. De Furia & J. Scacciaferro, *The MIDI Implementation Book*, (© 1986, Third Earth, Pompton Lake)

C. Petzold, *Programming Windows: the Microsoft guide to writing applications for Windows 3.1*, 3rd. ed., (© 1992, Microsoft Press, Redmond)

K. Pohlmann, *Principles of Digital Audio,* (© 1989, Sams, Indianapolis)

A. Stolz, *The SoundBlaster Book*, (© 1993, Abacaus, Grand Rapids)

J. Strawn, *Digital Audio Engineering, An Anthology*, (©1985, Kaufmann, Los Altos)

Yamamoto, *MIDI Guidebook*, 4th. ed., (© 1987, 1989, Roland Corp.)

Multimedia PC Capabilities

The AD1815 is MPC-2 and MPC-3 compliant. This compliance is achieved through the AD1815's flexible mixer and the embedded chip resources.

Music Synthesis

The AD1815 includes an embedded music synthesizer that emulates industry standard OPL3 FM synthesizer chips and deliver 20 voice polyphony. The internal synthesizer generates digital music data at 22.05 kHz and is summed into the DACs digital data stream prior to conversion. To sum synthesizer data with the ADC output, the ADC must be programmed for a 22.05 kHz sample rate.

EuSynth-1+

The synthesizer is a hardware implementation of Eusyhth-1 + code that was developed by Euphonics, a research and development company that specializes in audio processing and electronic music synthesis.

Wavetable MIDI Inputs

The AD1815 has a dedicated analog input for receiving an analog wavetable synthesizer output. Alternatively, a wavetable synthesizer's I^2S formatted digital output can be directly connected to one of the AD1815's I^2S serial ports. Digital wavetable data from the AD1815's I^2S port can be summed with other digital data streams being handled by the AD1815 and then sent to the 16-bit ΣΔ DAC.

MIDI

The primary interface for communicating MIDI data to and from the host PC is the compatible MPU-401 interface that operates in UART mode. The MPU-401 interface has two built-in FIFOs: a 64 byte receive FIFO and a 16 byte transmit FIFO.

Game Port

An IBM-compatible game port interface is provided on chip. The game port supports up to two joysticks via a 15-pin D-sub connector. Joystick registers supporting the Microsoft Direct Input standard are included as part of the register map. The AD1815 may be programmed to automatically sample the game port and save the value in the Joystick Position Data Register. When enabled, this feature saves up to 10% CPU MIPS by off-loading the host from constantly polling the joystick port.

Volume Control

The registers that control the Master Volume output stage are accessible through the parallel port. Master Volume output can also be controlled through a 2-pin hardware interface. One pin is used to increase the gain, the other pin attenuates the output, and both pins together mute the output entirely. Once muted, any further activity of these pins will unmute the AD1815's output.

Plug & Play

The AD1815 is fully Plug and Play configurable. For motherboard applications, the built-in Plug and Play protocol can be disabled with a software key providing a back door for the BIOS to configure the AD1815's logical devices. For information on the Plug & Play mode configuration process, see the *Plug & Play ISA Specification Version 1.0a (May 5, 1994)*. All the AD1815's logical devices comply with Plug & Play resource definitions described in the specification.

SERIAL INTERFACES

I²S Serial Ports

The two I²S serial ports on the AD1815 accept serial data in the following formats: Right-Justified, I²S-Justified, and Left-Justified.

The following figure shows the right-justified mode. LRCLK is HI for the left channel, and LO for the right channel. Data is valid on the rising edge of the BCLK. The MSB is delayed 16-bit clock periods from an LRCLK transition, so that when there are 64 BCLK periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

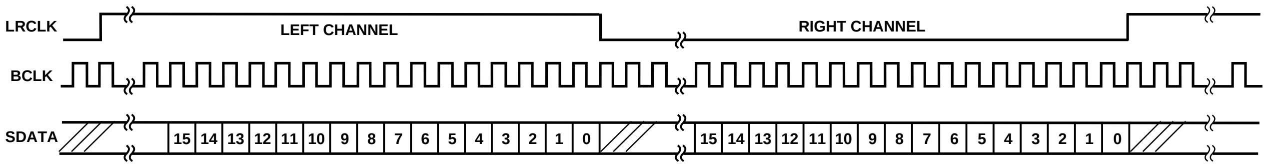


Figure 9. Serial Interface Right-Justified Mode

The following figure shows the I²S-justified mode. LRCLK is LO for the left channel, and HI for the right channel. Data is valid on the rising edge of BCLK. The MSB is left-justified to an LRCLK transition, but with a single BCLK period delay.

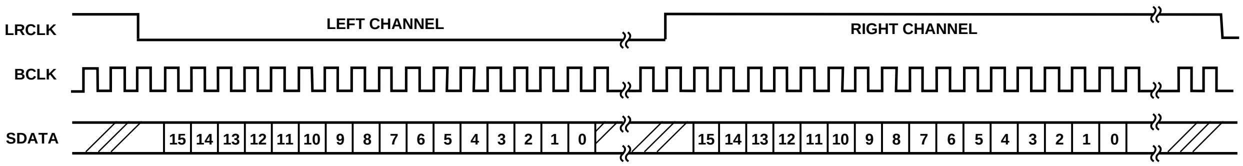


Figure 10. Serial Interface I²S-Justified Mode

The following figure shows the left-justified mode. LRCLK is HI for the left channel, and LO for the right channel. Data is valid on the rising edge of BCLK. The MSB is left-justified to an LRCLK transition, with no MSB delay.

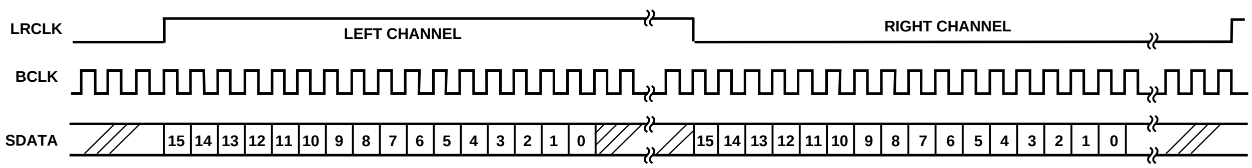


Figure 11. Serial Interface Left-Justified Mode

Bidirectional DSP Serial Interface

The AD1815 SoundComm Controller transmits and receives both data and control/status information through its DSP serial interface port (SPORT). The AD1815 is always the bus master and supplies the frame sync and the serial clock. The AD1815 has four pins assigned to the SPORT: SDI, SDO, SDFS, and SCLK. The SPORT has two operating modes: monitor and intercept. The SPORT always monitors the various data streams being processed by the AD1815. In intercept mode, any of the digital data streams can be manipulated by the DSP before reaching the final ADC or DAC stages.

The SDI and SDO pins handle the serial data input and output of the AD1815. Communication in and out of the AD1815 requires that bits of data are transmitted after a rising edge of SCLK, and sampled on the falling edge of SCLK. The SCLK frequency is always 11 MHz (or 1/3 or XTALI).

When the modem channel is not enabled, these time slots are mapped as shown in Table I.

Table I. Modem Disabled Time Slot Map

Time Slot	SDI Pin	SDO Pin
0	Control Word Input	Status Word Output
1	Control Register Data Input	Control Register Data Output
2	* SS/SB ADC Right Input (to ISA)	SS/SB ADC Right Output (from Codec)
3	* SS/SB ADC Left Input (to ISA)	SS/SB ADC Left Output (from Codec)
4	* SS/SB DAC Right Input (to Codec)	SS/SB DAC Right Output (from ISA)
5	* SS/SB DAC Left Input (to Codec)	SS/SB DAC Left Output (from ISA)
6	* FM DAC Right Input (to Codec)	FM DAC Right Output (from FM Synth Block)
7	* FM DAC Left Input (to Codec)	FM DAC Left Output (from FM Synth Block)
8	* I^{2}S 1 DAC Right Input (to Codec)	I^{2}S 1 DAC Right Output (from I^{2}S Port 1)
9	* I^{2}S 1 DAC Left Input (to Codec)	I^{2}S 1 DAC Left Output (from I^{2}S Port 1)
10	* I^{2}S 0 DAC Right Input (to Codec)	I^{2}S 0 DAC Right Output (from I^{2}S Port 0)
11	* I^{2}S 0 DAC Left Input (to Codec)	I^{2}S 0 DAC Left Output (from I^{2}S Port 0)

*This data is ignored by the AD1815 unless the channel pair is in intercept mode (see below).
SS - Sound System Mode
SB = Sound Blaster Mode

When the modem channel is enabled (DSP modem mode), time slots are mapped as above except for time Slot 2, which is as follows:

2	Modem DAC Input (to Codec)	Modem ADC Output (from Codec)

When the modem channel is enabled, stereo SB or SS capture is not possible and SB and SS fall back to mono capture. The right capture channel then gets the left channel capture data.

At startup (after pin reset), there are exactly 12 time slots per frame. The frame rate will be 57,291 and 2/3 Hz (11 MHz sclk/(16 bits × 12 slots)). Interfacing with an Analog Devices 21xx family DSP can be achieved by putting the ADSP-21xx in 24 slot per frame mode, where the first 12 and second 12 slots in the ADSP-21xx frame are identical.

The frame rate can be changed from its default by a write to the DFS(2:0) bits in register 33. Rate choices are: Maximum (57,291 and 2/3 Hz default), Modem rate, SS capture rate, SS playback rate, FM rate, I^{2}S Port (1) rate, or I^{2}S Port (0) rate. When the frame rate is less than 57,261 and 2/3 Hz, extra SCLK periods are added to fill up the time. The number of SCLK periods added will vary somewhat from frame to frame.

Similar to the AD1843, Valid out, Request in, and Valid in bits located in the control and status words are used to control sample data flow. If a channel's sample rate is equal to the frame rate, these bits can be ignored since they will predictably always be 1s.

By default, the DSP serial port only allows codec sample data I/O to be monitored. Intercept modes must be enabled to make substitutions in sample data flow to and from the codec. There are five bits in SS register 33 which enable intercept mode for SS capture, SS playback, FM playback, I^{2}S Port (1) playback, and I^{2}S Port (0) playback.

Control Word Input (Slot 0 SDI)

15	14	13	12	11	10	9	8
FCLR	RES	MODVI	SSCVI	SSPVI	FMVI	IS1VI	IS0VI

7	6	5	4	3	2	1	0
ALIVE	R/W	IA[5:0]					

IA [5:0] Indirect Register Address. Sound System Indirect Register Address defines the address of indirect registers shown in Table VI.

R/W Read/Write request. Either a read from or a write to a SS indirect register occurs every frame. Setting this bit initiates a SS indirect register read while clearing this bit initiates a SS indirect register write.

ALIVE DSP port alive bit. When set, this bit indicates to the powerdown timer that the DSP port is active. When cleared, this bit indicates that the DSP port is inactive.

IS0VI I^{2}S Port 0 Substitution Data Input Valid Flag. This bit is ignored if: (1) Intercept mode is not enabled for the I^{2}S port 0 channel pair, or (2) The AD1815 did not request data from the I^{2}S port 0 channel pair in the previous frame. Otherwise, setting this bit indicates that slots 10 and 11 contain valid right and left I^{2}S Port 0 substitution data. When this bit is cleared, data in slots 10 and 11 is ignored.

IS1VI I^{2}S Port 1 Substitution Data Input Valid Flag. This bit is ignored if: (1) Intercept mode is not enabled for I^{2}S port 1 channel pair, or (2) The AD1815 did not request data from the I^{2}S port channel pair in the previous frame. Otherwise, setting this bit indicates that Slots 8 and 9 contain valid right and left I^{2}S Port 1 substitution data. When this bit is cleared, data in slots 8 and 9 is ignored.

FMVI — FM Synthesis Substitution Data Input Valid Flag. This bit is ignored if: (1) Intercept mode is not enabled for the FM synthesis channel pair, or (2) The AD1815 did not request data from the FM synthesis channel pair in the previous frame (see the FMRQ Bit 9 in the status word output). Otherwise, setting this bit to 1 indicates that slots 6 and 7 contain valid right and left FM synthesis channel substitution data. When this bit is reset to 0, data in slots 6 and 7 is ignored.

SSPVI — SS/SB Playback Substitution Data Input Valid Flag. This bit is ignored if: (1) Intercept mode is not enabled for SS/SB playback, or (2) The AD1815 did not request data for SS/SB playback in the previous frame (see the SSPRQ bit in the Status Word Output). Otherwise, setting this bit indicates that Slots 4 and 5 contain valid right and left SS/SB playback substitution data. If in “capture rate equal to playback rate” mode, setting this bit also indicates that valid capture substitution data is being sent to the AD1815. If not in modem mode, right and left channel capture substitution data is accepted in Slots 2 and 3 respectively. If in modem mode, only mono capture substitution data is accepted in slots 2 and 3. When this bit is cleared, data in all slots controlled by this bit, as defined above, is ignored.

SSCVI — SS/SB Capture Substitution Data Input Valid Flag. This bit is ignored if: (1) Intercept mode is not enabled for SS/SB capture, or (2) The AD1815 did not request data for SS/SB capture in the previous frame (see the SSCRQ bit in the Status Word Output). Otherwise, setting this bit indicates that valid SS/SB capture substitution data is being sent to the AD1815. If not in modem mode, or DSP port or ISA bus based, right and left channel capture data is accepted in Slots 2 and 3 respectively. If in modem mode, only mono capture substitution data is accepted in Slot 3, because Slot 2, which is mapped to the right capture channel, is being used for modem. This mono data will, however, be sent to both left and right ISA SS/SB capture channels. When this bit is cleared, data in Slots 3 and 2 is ignored.

MODVI — Modem Input Valid flag. This bit is ignored if: (1) The AD1815 is in DSP modem mode, or (2) If the AD1815 did not request data for the modem in the previous frame (see the MODRQ bit in the Status Word Output). When in DSP modem mode, setting this bit indicates that Slot 2 contains valid modem data to be transmitted. When this bit is cleared, data in Slot 2 is ignored.

RES — Reserved: To insure future compatibility write “0” to all reserved bits.

FCLR — DSP Port Clear Status Flag. When you set this bit, (write 1), the PNPR and PDN flag bits in the status word (Bits 15 and 14 of slots 0 SDO) are cleared. When you clear this bit, (writing a 0), it has no effect on PNPR and PDN and preserves them in the previous states.

Status Word Output (Slot 0 SDO)

15	14	13	12	11	10	9	8
PDN	PNPR	MODVO	SSCVO	SSPVO	FMVO	IS1VO	IS0VO
7	6	5	4	3	2	1	0
MB1	MB0	MODRQ	SSCRQ	SSPRQ	FMRQ	IS1RQ	IS0RQ

IS0RQ — I^2S Port (0) Input Request Flag. This bit is set if intercept mode is enabled for I^2S Port (0) and its four-word stereo input buffer is not full.

IS1RQ — I^2S Port (1) Input Request Flag. This bit is set if intercept mode is enabled for I^2S Port (1) and its four-word stereo input buffer is not full.

FMRQ — FM Synthesis Input Request Flag. This bit is set if intercept mode is enabled for FM synthesis and its four-word stereo input buffer is not full.

SSPRQ — SS/SB Capture Input Request Flag. This bit is set if intercept mode is enabled for SS/SB playback and its four-word stereo input buffer is not full.

SSCRQ — SS/SB Capture Input Request Flag. This bit is set if intercept mode is enabled for SS/SB capture and its four-word stereo input buffer is not full.

MODRQ — Modem Input Request Flag. This bit is set if the modem is enabled and its four-word stereo input buffer is not full.

MB0 — Mailbox 0 Status Flag. This bit is set if the most recent action to SS indirect register 42 (DSP port Mail Box 1) was a write, and is cleared if the most recent action was a read. The status of this bit is also reflected in SS indirect register 33. It may be used as a handshake bit to facilitate communication between a DSP on the DSP port and a host CPU on the ISA bus.

MB1 — Mailbox 1 Status Flag. This bit is set if the most recent action to SS indirect register 43 (DSP port Mail Box 1) was a write and is cleared if the most recent action was a read. The status of this bit is also reflected in SS indirect register 33. It may be used as a handshake bit to facilitate communication between a DSP on the DSP port and a host CPU on the ISA bus.

IS0VO — I^2S Port 0 Valid Out. This bit is set if Slots 10 and 11 contain valid right and left I^2S Port 0 data.

IS1V1 — I^2S Port 1 Valid Out. This bit is set if Slots 8 and 9 contain valid right and left I^2S Port 1 data.

FMVO FM Synthesis Valid Out. This bit is set if Slots 6 and 7 contain valid left and right FM synthesis data.

SSPVO SS/SB Playback Valid Out. This bit is set if Slots 4 and 5 contain valid right and left SS/SB playback data.

SSCVO SS/SB Capture Valid Out. This bit is set if valid SS/SB capture data is being transmitted. If not in a modem mode, Slots 2 and 3 will contain valid right and left SS/SB capture data. If in modem mode, only Slot 3 will contain valid left SS/SB capture data as Slot 2 and the ADC right channel are used by the modem.

MODVO Modem Valid Out. This bit is set if Slot 2 contains valid modem capture data.

PNPR Plug and Play Reset flag. This bit is set by an AD1815 reset (RESETB pin asserted LOW), or by a Plug and Play reset command. This bit is cleared by the assertion of the FCLR bit in the control word. While this bit is set, all attempts to write a SS indirect register via the DSP port will be ignored and fail. This is to insure that Plug and Play resets are immediately applied to the application running on the DSP, without requiring them to continuously poll the Plug and Play reset status bit. During the frame that this bit is cleared (by asserting FCLR), an attempt to write a SS indirect register will succeed. If the FCLR bit is asserted continuously, writes to indirect registers via the DSP port will always be enabled. A Plug and Play reset command will set this PNPR bit HIGH during at least one frame.

PDN Powerdown flag. This bit is set by an AD1815 reset (RESETB pin asserted LOW), or by an AD1815 powerdown. Before an AD1815 powerdown sequence shuts down the DSP port, at least one frame will be sent with this bit set. This bit can be cleared by the assertion of the FCLR (DSP port status clear) bit in the control word, providing the AD1815 is no longer in powerdown.

The SDFS pin is used for the serial interface frame synchronization. New frames are marked by a one SCLK duration HI pulse driven out on SDFS one serial clock period before the frame begins. Upon initializing, there are exactly 12 time slots per frame, and 16 bits per time slot. The frame rate is 57,291 and 2/3 Hz (11 MHz SCLK / (16 bits * 12 slots). The frame rate can also be changed from the default value by reprogramming the rate in registers. The frame rate can run at the default rate or programmed to match the modem sample rate, ADC capture rate, DAC playback rate, music sample rate, $I^2S(1)$ sample rate, or $I^2S(0)$ sample rate. When the frame rate is not equivalent to the sample rate, Valid Out, Request In, and Valid In bits are used to control the sample data flow. When the frame rate is equivalent to the sample rate, Valid and Request bits can be ignored.

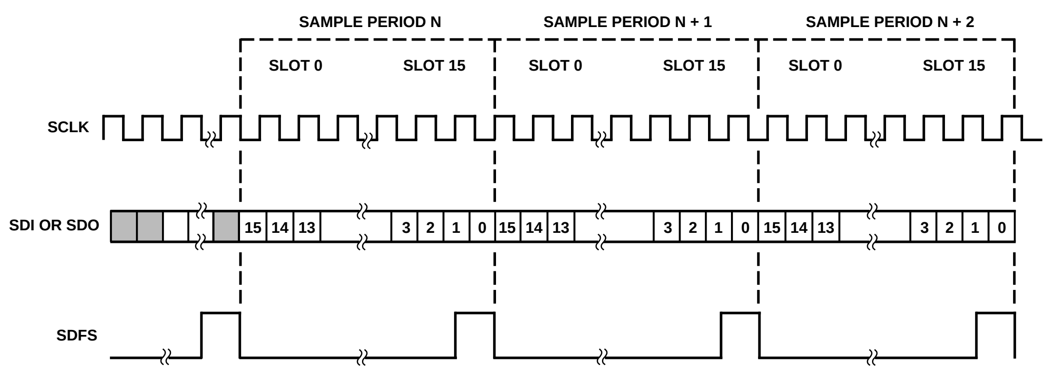


Figure 12. DSP Serial Interface (Default Frame Rate)

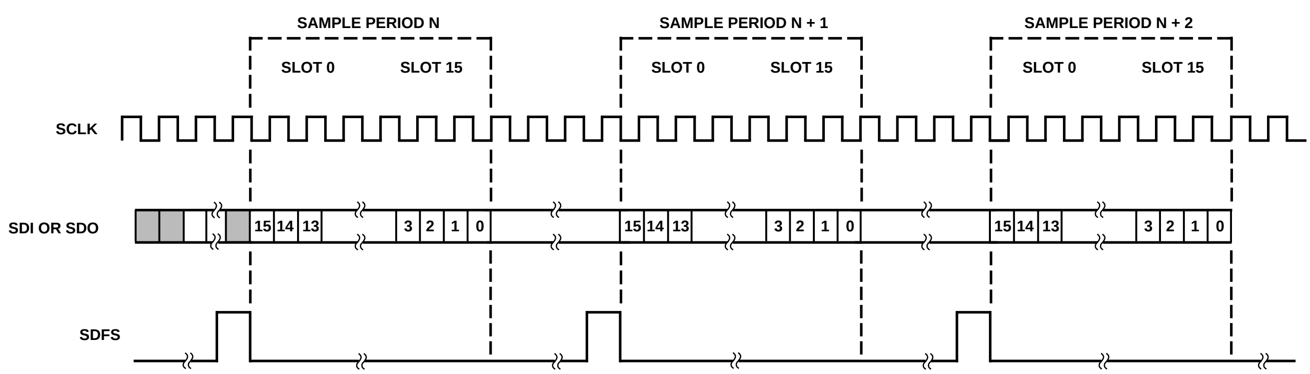


Figure 13. DSP Serial Interface (User Programmed Frame Rate)

The following figure illustrates the flexibility of the DSP Serial Port interface. This port can monitor or intercept any of the digital streams managed by the AD1815. Any ADC or DAC data stream can be intercepted by the port, shipped to an external DSP or ASIC, manipulated, and returned to any DAC summing path or the ADC.

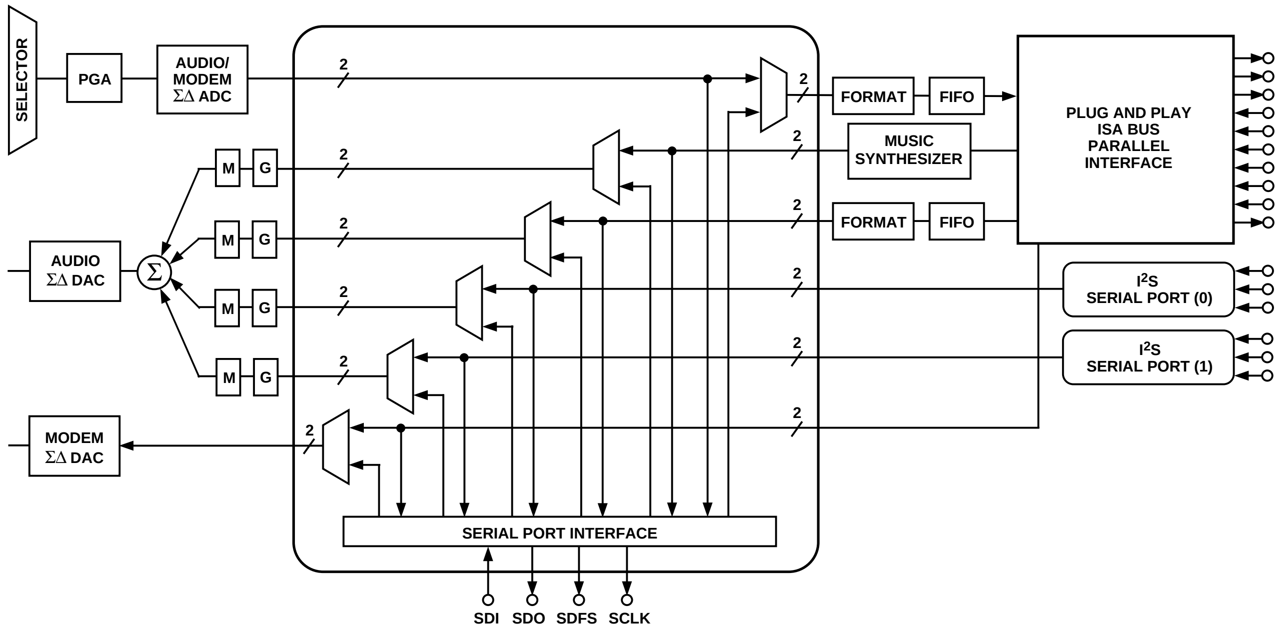


Figure 14. DSP Serial Port

ISA INTERFACE

AD1815 Chip Registers

Table II, Chip Register Diagram, details the AD1815 direct register set available from the ISA Bus. The PC I/O addressable ports must be configured using the Plug and Play Resources prior to any accesses by the host.

Table II. Chip Register Diagram

Register Type-Register Name	Register PC I/O Address
Plug and Play	
ADDRESS	0x279
WRITE_DATA	0xA79
READ_DATA	Relocatable in Range 0x203 – 0x3FF
Sound System Codec	
CODEC REGISTERS	0x(SS Base+0 – SS Base+15) Relocatable in Range 0x100 – 0x3FF See Table V
Sound Blaster Pro	
Music0: Address (w), Status (r)	0x(SB Base) Relocatable in Range 0x010 – 0x3F0
Music0: Data (w)	0x(SB Base+1)
Music1: Address (w)	0x(SB Base+2)
Music1: Data (w)	0x(SB Base+3)
Mixer Address (w)	0x(SB Base+4)
Mixer Data (w)	0x(SB Base+5)
Reset (w)	0x(SB Base+6 or 7)
Music0: Address (w)	0x(SB Base+8)
Music0: Data (w)	0x(SB Base+9)
Input Data (r)	0x(SB Base+A or +B)
Status (r), Output Data (w)	0x(SB Base+C or +D)
Status (r)	0x(SB Base+E or +F)

Register Type-Register Name	Register PC I/O Address
AdLib	
Music0: Address (w), Status (r)	0x(Adlib Base) Relocatable in Range 0x100 – 0x3F8
Music0: Data (w)	0x(Adlib Base+1)
Music1: Address (w)	0x(Adlib Base+2)
Music1: Data (w)	0x(Adlib Base+3)
MIDI MPU-401	
MIDI Data (r/w)	0x(MIDI Base) Relocatable in Range 0x100 – 0x3F8
MIDI Status (r), Command (w)	0x(MIDI Base+1)
Game Port	
Game Port I/O	0x(Game Base +0 to Game Base +7) Relocatable in Range 0x100 – 0x3F8

AD1815 Plug and Play Device Configuration Registers

The AD1815 may be configured according to the Intel/Microsoft Plug and Play Specification using the internal ROM. Alternatively, the PnP configuration sequence may be bypassed using the "Alternate Key Sequence" described in Appendix A.

The operating system configures/reconfigures AD1815 Plug and Play Logical Devices after system boot. There are no "boot-devices" among the Plug and Play Logical Devices in the AD1815. Non-Plug and Play BIOS systems configure the AD1815's Logical Devices after boot using drivers. Depending on BIOS implementations, Plug and Play BIOS systems may configure the AD1815's Logical Devices before POST or after Boot. See the *Plug and Play ISA Specification Version 1.0a* for more information on configuration control. To complete this configuration, the system reads resource data from the AD1815's on-chip resource ROM and from any other Plug and Play cards in the system, then arbitrates the configuration of system resources with a heuristic algorithm. The algorithm maximizes the number of *active* devices and the *acceptability* of their configurations.

The system considers all Plug and Play logical device resource data at the same time and makes a conflict-free assignment of resources to the devices. If the system cannot assign a conflict-free resource to a device, the system does not configure or activate the device. All configured devices are activated.

The system's Plug and Play support selects all necessary drivers, starts them, and maintains a list of system resources allocated to each logical device. Optionally, you can reassign system resources at runtime with a Plug and Play Resource Manager. The custom setup created using the manager can be saved and used automatically on subsequent system boots.

Plug and Play Device IDs (embedded in the logical device's resource data) provide the system with the information required to find and load the correct device drivers. One custom driver, the AD1815 Sound System driver from Analog Devices, is required for correct operation. In the other cases (MIDI, Game Port), the system can use generic drivers. Table III lists the AD1815's logical devices and compatible Plug and Play device drivers.

Table III. Logical Devices and Compatible Plug and Play Device Drivers

Logical Device Number	Emulated Device	Compatible (Device ID)	Device ID
0	Sound System	—	ADS7150
1	MIDI MPU401 compatible	PNPB006	ADS7151
2	Game/Joystick port	PNPB02F	ADS7152

The configuration process for the logical devices on the AD1815 is described in the *Plug and Play ISA Specification Version 1.0a (May 5, 1994*). The specification describes how to transfer the logical devices from their start-up *Wait For Key* state to the *Config* state and how to assign I/O ranges, interrupt channels, and DMA channels. See Appendix A for an example setup program and specific Plug and Play resource data.

Table IV describes in detail the I/O Port Address Descriptors, DMA Channels, Interrupts for the functions required for the AD1815 Logical Device groups.

Table IV. Logical Device Configuration

LDN	PnP Function	Description
0	I/O Port Address Descriptor (0x60-0x61)	The Sound Blaster Pro address range is from 0x100 to 0x3F0. The typical address is 0x220. The range is 16 bytes long and must be aligned to a 16 byte memory boundary.
0	I/O Port Address Descriptor (0x62-0x63)	The Adlib address range is from 0x100 to 0x3F8. The typical address is 0x388. The range is 4 bytes long and must be aligned to a 8 byte memory boundary.
0	I/O Port Address Descriptor (0x64-0x65)	The Codec address range is from 0x100 to 0x3F8. The range is 16 bytes long and must be aligned to a 16 byte memory boundary.
0	Interrupt Request Level Select (0x70-0x71)	This IRQ is shared between the SB Pro device and the Codec. These devices require one of the following IRQ channels: 5, 7, 9, 11, 12, or 15. Typically, the IRQ is set to 5 or 7 for this device.
0	DMA Playback Channel Select (0x74)	This 8-bit channel is shared between the SB Pro device and the Codec for playback. These devices require one of the following DMA channels; 0, 1, 3. Typically, DMA channel 1 is set.
0	DMA Capture Channel Select (0x75)	This the DMA channel used for capturing Codec data. The Codec operates in single channel mode if a separate DMA channel for capture and playback is not assigned. The following DMA channels may be programmed; 0, 1, 3. DMA Channel 4 indicates single channel mode.
1	I/O Port Address Descriptor (0x60-0x61)	The MPU-401 compatible device address range is 0x100 to 0x3FE. Typical configurations use 0x330. The range is 2 bytes long and must be aligned to a 2 byte memory boundary.
1	Interrupt Request Level Select (0x70-0x71)	The MIDI device requires one of the following IRQ channels: 5, 7, 9, 11, 12, or 15.
2	I/O Port Address Descriptor (0x60-0x61)	The Game Port address range is from 0x100 to 0x3F8. The typical address is 0x200. The range is 8 bytes long and must be aligned to a 8 byte memory boundary.

NOTE
DMA channel 4 indicates single-channel mode.

Sound System Direct Registers

The AD1815 has a set of 16 programmable Sound System Direct Registers and 36 Indirect Registers. This section describes all the AD1815 registers and gives their address, name, and initialization state/reset value. Following each register table is a list (in ascending order) of the full register name, its usage, and its type: (RO) Read Only, (WO) Write Only, (STKY) Sticky, (RW) Read Write, and Reserved (res). Table V is a map of the AD1815 direct registers.

Table V. Sound System Direct Registers

Direct Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BASE + 0	CRDY	IMRDY	INADR[5:0]					
BASE + 1	PI	CI	TI	VI	DI	RI	GI	SI
BASE + 2	Indirect SS Data [7:0]							
BASE + 3	Indirect SS Data [15:8]							
BASE + 4	RES	MOF	PUR	COR	ORR [1:0]		ORL [1:0]	
BASE + 5	PFH	PDR	PLR	PUL	CFH	CDR	CLR	CUL
BASE + 6	PIO Playback/Capture [7:0]							
BASE + 7	RESERVED							
BASE + 8	TRD	DAZ	PFMT [1:0]		PC/L	PST	PIO	PEN
BASE + 9	RES		CFMT [1:0]		PC/L	CST	CIO	CEN
BASE + 10	PIO MODEM OUT / IN [7:0]							
BASE + 11	PIO MODEM OUT / IN [15:8]							
BASE + 12	JOYSTICK DATA [7:0]							
BASE + 13	JRDY	JWRP	JSEL [1:0]		JMSK [3:0]			
BASE + 14	JAXIS [7:0]							
BASE + 15	JAXIS [15:8]							

[Base+0] **Chip/Modem Status/Indirect Address**

7	6	5	4	3	2	1	0
CRDY	IMRDY	INADR[5:0]					

RESET = [0x00]

INADR [5:0] (RW) Indirect Address for Sound System (SS). These bits are used to access the Indirect Registers shown in Table VIII. All registers data must be written in pairs, low byte followed by high byte, by loading the Indirect SS Data Registers, (Base +2) and (Base +3).

IMRDY (RO) ISA Modem Ready. The AD1815 asserts this bit when the modem can accept data.
- 0 Modem not ready.
- 1 Modem ready.

CRDY (RO) AD1815 Ready. The AD1815 asserts this bit when AD1815 can accept data.
- 0 AD1815 not ready.
- 1 AD1815 ready.

[Base+1] **Interrupt Status**

7	6	5	4	3	2	1	0
PI	CI	TI	VI	DI	RI	GI	SI

RESET = [0x00]

SI (RO) SoundBlaster generated Interrupt.
- 0 No interrupt.
- 1 SoundBlaster interrupt pending.

GI (RW) Game Interrupt (Sticky, Write "0" to Clear).
- 0 No interrupt.
- 1 An interrupt is pending due to Digital Game Port data ready.

RI (RW) Ring Interrupt (Sticky, Write "0" to Clear).
- 0 No interrupt.
- 1 An interrupt is pending due to a Hardware Ring pin being asserted.

DI (RW) DSP Interrupt (Sticky, Write "0" to Clear).
- 0 No interrupt.
- 1 An interrupt is pending due to a write to the DIT bit in indirect register [33] bit <13>.

VI (RW) Volume Interrupt (Sticky, Write "0" to Clear).
- 0 No interrupt.
- 1 An interrupt is pending due to Hardware Volume Button being pressed.

TI (RW) Timer Interrupt. This bit indicates there is an interrupt pending from the timer count registers. (Sticky, Write "0" to Clear).
- 0 No interrupt.
- 1 Interrupt is pending from the timer count register.

CI (RW) Capture Interrupt. This bit indicates that there is an interrupt pending from the capture DMA count register. (Sticky, Write "0" to Clear).
- 0 No interrupt.
- 1 Interrupt is pending from the capture DMA count register.

PI (RW) Playback Interrupt. This bit indicates that there is an interrupt pending from the playback DMA count register. (Sticky, Write "0" to Clear).
- 0 No interrupt.
- 1 Interrupt is pending from the playback DMA count register.

[Base+2] **Indirect SS Data Low Byte**

7	6	5	4	3	2	1	0
Indirect SS Data [7:0]							

RESET = [0xXX]

[Base+3] **Indirect SS Data High Byte**

7	6	5	4	3	2	1	0
Indirect SS Data [15:8]							

RESET = [0xXX]

Indirect SS Data [15:0] Indirect Sound System Data. Data in this register is written to the Sound System Indirect Register specified by the address contained in INDAR [5:0], Sound System Direct Register [Base +0]. Data is written when the Indirect SS Data High Byte value is loaded.

[Base+4] PIO Debug

7	6	5	4	3	2	1	0
RES	MOF	PUR	COR	ORR[1:0]		ORL[1:0]	

RESET = [0x00]

All bits in this register are sticky until any write which clears all bits to 0.

ORL/ORR [1:0] (RO) Overrange Left/Right detect. These bits record the largest output magnitude on the ADC right and left channels and are cleared to 00 after any write to this register. The peak amplitude as recorded by these bits is "sticky," i.e., the largest output magnitude recorded by these bits will persist until these bits are explicitly cleared. They are also cleared by powering down the ADC right channel.

ORL/ORR	Over/Under Range Detection
00	Less than –1 dB Underrange
01	Between –1 dB and 0 dB Underrange
10	Between 0 dB and 1 dB Overrange
11	Greater than 1 dB Overrange

COR (RO) Capture Over Run. The codec sets (1) this bit when capture data is not read within one sample period after the capture FIFO fills. When COR is set, the FIFO is full and the codec discards any new data generated. The codec clears this bit immediately after a four byte capture sample is read.

PUR (RO) Playback Under Run. The codec sets (1) this bit when playback data is not written within one sample period after the playback FIFO empties. The codec clears (0) this bit immediately after a four byte playback sample is written. When PUR is set the playback channel has "run out" of data and either plays back a mid-scale value or repeats the last sample.

MOF (RO) Modem Fail ("Sticky "). The modem sets (1) this bit if in ISA modem mode (see Sound System Indirect Register 32, bit IME) and the four deep transmit/receive FIFO underruns.

[Base+5] PIO Status

7	6	5	4	3	2	1	0
PFH	PDR	PLR	PUL	CFH	CDR	CLR	CUL

RESET = [0x00]

CUL (RO) Capture Upper/Lower Sample. This bit indicates whether the PIO capture data ready is for the upper or lower byte of the channel.
- 0 Lower byte ready.
- 1 Upper byte ready or any 8-bit mode.

CLR (RO) Capture Left/Right Sample. This bit indicates whether the PIO capture data waiting is for the left channel ADC or the right channel ADC.
- 0 Right channel.
- 1 Left channel or mono.

CDR (RO) Capture Data Ready. The PIO Capture Data register contains data ready for reading by the host. This bit should be used only when direct programmed I/O data transfers are desired (FIFO has at least 4 bytes before full).
- 0 ADC is stale. Do not reread the information.
- 1 ADC data is fresh. Ready for next host data read.

CFH (RO) Capture FIFO Half Full. (FIFO has at least 32 bytes before full.)

PUL (RO) Playback Upper/Lower Sample. This bit indicates whether the PIO playback data needed is for the upper or lower byte of the channel.
- 0 Lower byte needed.
- 1 Upper byte needed or any 8-bit mode.

PLR (RO) Playback Left/Right Sample. This bit indicates whether the PIO playback data needed is or the left channel DAC or the right channel DAC.
- 0 Right channel needed.
- 1 Left channel or mono.

PDR (RO) Playback Data Ready. The PIO Playback data register is ready for more data. This bit should only be used when direct programmed I/O data transfers are desired (FIFO can take at least 4 bytes).
- 0 DAC data is still valid. Do not overwrite.
- 1 DAC data is stale. Ready for next host data write value.

PFH (RO) Playback FIFO Half Empty. FIFO can take at least 32-bytes, 8 groups of 4-bytes.

[Base+6] PIO Data

7	6	5	4	3	2	1	0	
PIO Playback/Capture [7:0]								RESET = [0x00]

PIO Playback/ Capture [7:0] — The Programmed I/O (PIO) Data Registers for capture and playback are mapped to the same address. Writes send data to the Playback Register and reads will receive data from the Capture Register.

Reading this register will increment the capture byte state machine so that the following read will be from the next appropriate byte in the sample. The exact byte may be determined by reading the PIO Status Register. Once all relevant bytes have been read, the state machine will stay pointed to the last byte of the sample until a new sample is received.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes have been written, subsequent byte writes will be ignored. The state machine is reset when the current sample is transferred.

Note: All writes to the FIFO "MUST" contain 4 bytes of data.
* 1 sample of 16-bit stereo
* 2 samples of 16-bit mono
* 2 samples of 8-bit stereo (Linear PCM, U-law PCM, A-Law PCM)
* 4 samples of 8-bit mono (Linear PCM, U-law PCM, A-Law PCM)

[Base+7] Reserved

7	6	5	4	3	2	1	0	
Reserved [7:0]								RESET = [0xXX]

[Base+8] Playback Config

7	6	5	4	3	2	1	0	
TRD	DAZ	PFMT [1:0]		PC/L	PST	PIO	PEN	RESET = [0x00]

PEN (RW) Playback Enable. This bit enables or disables programmed I/O data playback.
0 Disable
1 Enable

PIO (RW) Programmed Input/Output. This bit determines whether the playback data is transferred via DMA or PIO.
0 DMA transfers only.
1 PIO transfers only.

PST (RW) Playback Stereo/Mono select. These bits select stereo or mono formatting for the input audio data streams. In stereo, the Codec alternates samples between channels to provide left and right channel input. For mono, the Codec captures samples on the left channel stereo.
0 Mono
1 Stereo

PC/L (RW) Playback Companded/Linear Select. This bit selects between a linear digital representation of the audio signal or a nonlinear, companded format for all output data. The type of linear PCM or the type of companded format is defined by PFMT [1:0].
0 Linear PCM
1 Companded

PFMT [1:0] (RW) Playback Format. Use these bits to select the playback data format for output data according to Table VI and Figure 15.

DAZ (RW) DAC zero. This bit forces the DAC to zero.
0 Repeat last sample.
1 Force DAC to ZERO.

TRD (RW) Transfer Request Disable. This bit enables or disables Codec DMA transfers during a Codec interrupt (indicated by the SS Codec Status register's INT bit being set (1)). This assumes Codec DMA transfers were enabled and the SS Codec Indexed (0x09) Interface Configuration register's PEN or CEN bits are set.
0 Transfer Request Enable.
1 Transfer Request Disable.

After setting format bits, sample data into the AD1815 must be ordered according to Figure 15, Table VI.

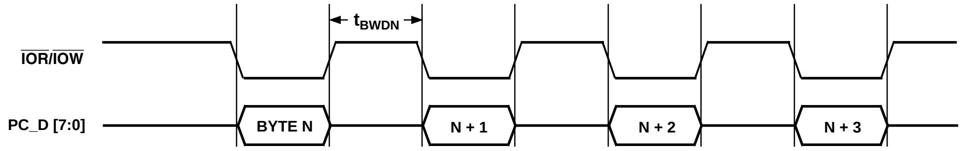


Figure 15. Codec Transfers

Table VI. Codec Transfers

ST	FMT1 FMT0 C/L	Format	Byte 3 MSB LSB	Byte 2 MSB LSB	Byte 1 MSB LSB	Byte 0 MSB LSB
0	000	Mono Linear, 8-Bit Unsigned	Sample 3 8-Bits Left Channel	Sample 2 8-Bits Left Channel	Sample 1 8-Bits Left Channel	Sample 0 8-Bits Left Channel
1	000	Stereo Linear, 8-Bit Unsigned	Sample 1 8-Bits Right Channel	Sample 1 8-Bits Left Channel	Sample 0 8-Bits Right Channel	Sample 0 8-Bits Left Channel
0	001	Mono µ-Law, 8-Bit Companded	Sample 3 8-Bits Left Channel	Sample 2 8-Bits Left Channel	Sample 1 8-Bits Left Channel	Sample 0 8 Bits Left Channel
1	001	Stereo µ-Law, 8-Bit Companded	Sample 1 8-Bits Right Channel	Sample 1 8-Bits Left Channel	Sample 0 8-Bits Right Channel	Sample 0 8 Bits Left Channel
0	010	Mono Linear 16-Bit Little Endian	Sample 1 Upper 8-Bits Left Channel	Sample 1 Lower 8-Bits Left Channel	Sample 0 Upper 8-Bits Left Channel	Sample 0 Lower 8-Bits Left Channel
1	010	Stero Linear 16-Bit Little Endian	Sample 0 Upper 8-Bits Right Channel	Sample 0 Lower 8-Bits Right Channel	Sample 0 Upper 8-Bits Left Channel	Sample 0 Lower 8-Bits Left Channel
0	011	Mono A-Law, 8-Bit Companded	Sample 3 8-Bits Left Channel	Sample 2 8-Bits Left Channel	Sample 1 8-Bits Left Channel	Sample 0 8-Bits Left Channel
1	011	Stereo A-Law, 8-Bit Companded	Sample 1 8-Bits Right Channel	Sample 1 8-Bits Left Channel	Sample 0 8-Bits Right Channel	Sample 0 8-Bits Left Channel
0	100	Reserved				
1	100	Reserved				
0	101	Reserved				
1	101	Reserved				
0	110	Mono Linear, 16-Bit Big Endian	Sample 1 Lower 8-Bits Left Channel	Sample 1 Upper 8-Bits Left Channel	Sample 0 Lower 8-Bits Left Channel	Sample 0 Upper 8-Bits Left Channel
0	110	Stereo Linear, 16-Bit Big Endian	Sample 0 Lower 8-Bits Right+ Channel	Sample 0 Upper 8-Bits Left Channel	Sample 0 Lower 8-Bits Left Channel	Sample 0 Upper 8-Bits Left Channel
0	111	Reserved				
1	111	Reserved				

[Base+9] **(Capture Config)**

7	6	5	4	3	2	1	0
RES		CFMT [1:0]		CC/L	CST	CIO	CEN

RESET = [0x00]

CEN	(RW)	Capture Enable. This bit enables or disables data capture. 0 Disable 1 Enable
CIO	(RW)	Capture Programmed I/O. This bit determines whether the capture data is transferred via DMA or PIO. 0 DMA 1 PIO
CST	(RW)	Capture Stereo/Mono Select. This bit selects stereo or mono formatting for the input audio data streams. In stereo, the Codec alternates samples between channels to provide left and right channel input. For mono, the Codec captures samples on the left channel. 0 Mono 1 Stereo
CC/L	(RW)	Capture Companded/Linear Select. This bit selects between a linear digital representation of the audio signal or a nonlinear, companded format for all output data. The type of linear PCM or the type of companded format is defined by CFMT [1:0]. 0 Linear PCM 1 Companded
CFMT [1:0]	(RW)	Capture Format. Use these bits to select the format for capture data according to the following Table VI and Figure 15.

[Base+10] PIO Modem Data Low Byte

7	6	5	4	3	2	1	0	
PIO Modem Out/Modem In [7:0]								RESET = [0xXX]

[Base+11] PIO Modem Data High Byte

7	6	5	4	3	2	1	0	
PIO Modem Out/Modem In [15:8]								RESET = [0xXX]

[Base+12] Joystick RAW DATA

7	6	5	4	3	2	1	0	
Joystick Data [7:0]								RESET = [0xF0]

DATA (RO) Joystick Data. Joystick Data (identical to 0x201): Writes to this register are ignored.

[Base+13] Joystick Control

7	6	5	4	3	2	1	0	
JRDY	JWRP	JSEL [1:0]		JMSK [3:0]				RESET = [0x8F]

JMSK [3:0] (RW) Joystick Axis Mask. JRDY bit calculated based on axes selected by JMSK only.

xxx1	Enable AX
xx1x	Enable AY
x1xx	Enable BX
1xxx	Enable BY

JSEL [1:0] (RW) Joystick Select. Selects one of four joystick axis register sets according to the following table:

00	Read AX (16 Bits) from [Base+14] & [Base+15]
01	Read AY (16 Bits) from [Base+14] & [Base+15]
10	Read BX (16 Bits) from [Base+14] & [Base+15]
11	Read BY (16 Bits) from [Base+14] & [Base+15]

JWRP (RW) Joystick Wrapmode. Continuous Joystick sampling mode—sampling automatically restarted every ~16 ms.

JRDY (RO) Joystick Ready. Sampling complete, joystick data ready for reading.

Note: Sampling must be started manually if JWRP is set before any sampling cycles are run. To start sampling AFTER setting the WRP bit, write to the joystick port [Base+14].

[Base+14] Joystick Position Data Low Byte

7	6	5	4	3	2	1	0	
JAXIS [7:0]								RESET = [0xFF]

JAXIS [7:0] (RO) Joystick Axis Low Byte.

Note: Axis to be read through this register is selected by the JSEL bits in the control register. A write to this register starts a sampling cycle.

[Base+15] Joystick Position Data High Byte

7	6	5	4	3	2	1	0	
JAXIS [15:8]								RESET = [0xFF]

JAXIS [15:8] (RO) Joystick Axis High Byte.

Note: Axis to be read through this register is selected by the JSEL bits in the control register. A write to this register starts a sampling cycle.

Sound System Indirect Registers

Writing Indirect Registers

All Indirect Registers "MUST" be written in pairs: low byte followed by high byte. The Indirect Address Register [SSBASE+0] holds the address for a register pair, the Indirect Low Data Byte [SSBASE+2] is used to write low data byte and Indirect High Data Byte [SSBASE+3] is used to write the High data byte. The Low data byte is held in in the temporary register until the upper byte is written.

Programming Example

"Write Sample Rate for Playback to 11,000 (2AF8hex)"

1) Write [SSBASE+0] with 0x08; indirect register for playback sample rate
2) Write [SSBASE+2] with 0xF8; low byte of 16-bit sample rate register
3) Write [SSBASE+3] with 0x2A; high byte of 16-bit sample rate register

Reading Indirect Registers

All indirect registers can be read individually. The Sound System Indirect Address Register [SSBASE+0] holds the address for a register pair, the Indirect Low Data Byte [SSBASE+2] is used to read low data byte and Indirect High Data Byte[SSBASE+3] is used to read the High data byte.

Programming Example

"Read Sample Rate for Playback to 11,000 (2AF8hex)"

```
1) Write [SSBASE+0] with 0x08    ; Indirect register for Playback Sample Rate
2) Read [SSBASE+2]               ; Low byte of 16-bit sample rate register
3) Read  [SSBASE+3]              ; High byte of 16-bit sample rate register
```

ISR Saves and Restores

For Interrupt Service Routines, ISRs, it is necessary to save and restore the Indirect Address and the Low Byte Temp Data registers inside the ISR.

Programming Example

"Save/Restore during an ISR"

Beginning of ISR:

```
1) Read  [SSBASE+0]               ; Save Indirect Address register to TMP_IA
2) Write [SSBASE+0] with 0x00;    ; Indirect Register for Low Byte Temp Data
3) Read  [SSBASE+2]               ; Save Low Byte Temp data to TMP_LBT
4) ISR Code                       ; ISR routine
5) Write [SSBASE+2] with TMP_LBT  ; Restore Low Byte Temp data TMP_LBT
6) Write [SSBASE+0] with TMP_IA   ; Restore Indirect Address TMP_IA
7) Return from Interrupt          ; Return from ISR
```

Table VII. Indirect Register Map and Reset/Default States

Index	Register Name	Reset/ Default State
0	Low Byte TMP	0xXX
1	Interrupt Enable and External Control	0x0102
2	Voice Playback Sample Rate	0x1F40
3	Voice Capture Sample Rate	0x1F40
4	Voice Attenuation	0x8080
5	FM Attenuation	0x8080
6	$I^2S(1)$ Attenuation	0x8080
7	$I^2S(0)$ Attenuation	0x8080
8	Playback Base Count	0x0000
9	Playback Current Count	0x0000
10	Capture Base Count	0x0000
11	Capture Current Count	0x0000
12	Timer Base Count	0x0000
13	Timer Current Count	0x0000
14	Master Volume Attenuation	0x0000
15	CD Gain/Attenuation	0x8888
16	Synth Gain/Attenuation	0x8888
17	Video Gain/Attenuation	0x8888
18	Line Gain/Attenuation	0x8888
19	Mic/Mono-In Gain Attenuation	0x8888
20	ADC Source Select and ADC PGA	0x0000
32	Chip Configuration	0x00F0
33	DSP Configuration	0x0000
34	FM Sample Rate	0x5622
35	$I^2S(1)$ Sample Rate	0xAC44
36	$I^2S(0)$ Sample Rate	0xAC44
37	Modem Sample Rate	0x1C20
38	Programmable Clock Rate	0xAC44
39	Modem DAC and ADC Attenuation	0x8000
40	Modem Mix Attenuation	0x80XX
41	Hardware Volume Button Modifier and Status	0xXX1B
42	DSP Mailbox 0	0x0000
43	DSP Mailbox 1	0x0000
44	Powerdown and Timer Control	0x0000
45	Version ID	0x0000
46	Reserved	0x0000

Table VIII. Sound System Indirect Registers

	(High Byte)								(Low Byte)							
ADDRESS	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
00 (0x00)	RES								LBTD [7:0]							
01 (0x01)	PIE	CIE	TIE	VIE	DIE	RIE	JIE	SIE	RES						XC1	XC0
02 (0x02)	VPSR [15.8]								VPSR [7:0]							
03 (0x03)	VCSR [15:8]								VCSR [7:0]							
04 (0x04)	LVM	RES	LVA [5:0]						RVM	RES	RVA [5:0]					
05 (0x05)	LFMM	RES	LFMA [5:0]						LFMM	RES	RFMA [5:0]					
06 (0x06)	LS1M	RES	LS1A [5:0]						RS1M	RES	RS1A [5:0]					
07 (0x07)	LS0M	RES	LS0A [5:0]						RS0M	RES	RS0A [5:0]					
08 (0x08)	PBC [15:8]								PBC [7:0]							
09 (0x09)	PCC [15:8]								PCC [7:0]							
10 (0x0A)	CBC [15:8]								CBC [7:0]							
11 (0x0B)	CCC [15:8]								CCC [7:0]							
12 (0x0C)	TBC [15:8]								TBC [7:0]							
13 (0x0D)	TCC [15:8]								TCC [7:0]							
14 (0x0E)	LMVM	RES		LMVA [4:0]					RMVM	RES		RMVA [4:0]				
15 (0x0F)	LCDM	RES		LCDA [4:0]					RCDM	RES		RCDA [4:0]				
16 (0x10)	LSYM	RES		LSYA [4:0]					RSYM	RES		RSYA [4:0]				
17 (0x11)	LVDM	RES		LVDA [4:0]					RVDM	RES		RVDA [4:0]				
18 (0x12)	LLM	RES		LLA [4:0]					RLM	RES		RLA [4:0]				
19 (0x13)	MCM	M20	RES	MCA [4:0]					MM	RES		MA [4:0]				
20 (0x14)	LAGC	LAS [2:0]			LAG [3:0]				RAGC	RAS [2:0]			RAG [3:0]			
32 (0x20)	WSE	CDE	RES	CNP	RES		IME	IMR	COF [3:0]				I2SF1 [1:0]		I2SF0 [1:0]	
33 (0x21)	DS1	DS0	DIT	DME	DMR	ADR	I1T	I0T	CPI	PBI	FMI	I1I	I01	DFS [2:0]		
34 (0x22)	FSMR [15:8]								FMSR [7:0]							
35 (0x23)	S1SR [15:8]								S1SR [7:0]							
36 (0x24)	S0SR [15:8]								S0SR [7:0]							
37 (0x25)	MSR [15:8]								MSR [7:0]							
38 (0x26)	PCR [15:8]								PCR [7:0]							
39 (0x27)	MDM	RES		MDA [4:0]					RES				MAG [3:0]			
40 (0x28)	MMM	RES		MMA [4:0]					RES							
41 (0x29)	RES								VMU	VUP	VDN	BM [4:0]				
42 (0x2A)	MB0R [15:8]								MB0R [7:0]							
43 (0x2B)	MB1R [15:8]								MB1R [7:0]							
44 (0x2C)	CPD	RES	PIW	PIR	PAA	PDA	PDP	PTB	RES							
45 (0x2D)	VER [15:8]								VER [7:0]							
46 (0x2E)	RES								RES							

[00] INDIRECT LOW BYTE TMP **DEFAULT = [0xXX]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RES								LBTD [7:0]							

LBTD [7:0] Low Byte Temporary Data holding latch for register pair writes
Written on any write to [SSBase + 2]
Read from [SSBase + 2] when the indirect address is 0x00

[01] INTERRUPT ENABLE AND EXTERNAL CONTROL **DEFAULT = [0x0102]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
PIE	CIE	TIE	VIE	DIE	RIE	JIE	SIE	RES						XC1	XC0

XC0 (R/W) External Control 0. The state of this bit is reflected on the XCTLO pin. This pin is also muxed with PCLKO. COF must be greater than 11 for PCLKO to be disabled, SS [32].

XC1 (R/W) External Control 1. The state of this bit is reflected on the XCTL1 pin. XCTL1 may also be used for Ring-In Interrupt.

SIE (R/W) Sound Blaster Interrupt Enable;
0 Sound Blaster Interrupt disabled
1 Sound Blaster Interrupt enabled

JIE (R/W) Joystick Interrupt Enable;
0 Joystick Interrupt disabled
1 Joystick Interrupt enabled

RIE	(R/W)	Ring Interrupt Enable; 0 Ring Interrupt disabled 1 Ring Interrupt enabled
DIE	(R/W)	DSP Interrupt Enable; 0 DSP Interrupt disabled 1 DSP Interrupt enabled
VIE	(R/W)	Volume Interrupt Enable. If enabled, software increments/decrements BUTTON MODIFIER via interrupt routine and pushing buttons only sets VUP, VDN, VMU bits. It does not change the volume. 0 Volume Interrupt disabled 1 Volume Interrupt enabled
TIE	(R/W)	Timer Interrupt Enable; 0 Timer Interrupt disabled 1 Timer Interrupt enabled
CIE	(R/W)	Capture Interrupt Enable; 0 Capture Interrupt disabled 1 Capture Interrupt enabled
PIE	(R/W)	Playback Interrupt Enable; 0 Playback Interrupt disabled 1 Playback Interrupt enabled

[02] VOICE PLAYBACK SAMPLE RATE **DEFAULT = [0x1F40]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	
VPSR [15:8]								VPSR [7:0]							

VPSR [15:0] Voice Playback Sample Rate. The sample rate can be programmed from 4 kHz to 55.2 kHz in 1 hertz increments. The default playback sample rate is 8 kHz.

[03] VOICE CAPTURE SAMPLE RATE **DEFAULT = [0x1F40]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
VCSR [15:8]								VCSR [7:0]							

VCSR [15:0] Voice Capture Sample Rate. The sample rate can be programmed from 4 kHz to 55.2 kHz in 1 hertz increments. Ignored if CNP bit in SS [32] = 0 in which case VPSR [15:0] controls capture rate. The default capture sample rate is 8 kHz.

[04] VOICE ATTENUATION **DEFAULT = [0x8080]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LVM	RES	LVA [5:0]						RVM	RES	RVA [5:0]					

RVA [5:0] Right Voice Attenuation for Playback channel. The LSB represents –1.5 dB, 000000 = 0 dB and the range is 0 dB to –94.5 dB.

RVM Right Voice Mute. 0 = Unmuted, 1 = Muted.

LVA [5:0] Left Voice Attenuation for Playback channel. The LSB represents –1.5 dB, 000000 = 0 dB and the range is 0 dB to –94.5 dB

LVM Left Voice Mute. 0 = Unmuted, 1 = Muted.

[05] FM ATTENUATION **DEFAULT = [0x8080]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LFMM	RES	LFMA [5:0]						RFMM	RES	RFMA [5:0]					

RFMA [5:0] Right F Music Attenuation for the internal Music Synthesizer. The LSB represents –1.5 dB, 000000 = 0 dB and the range is 0 dB to –94.5 dB.

RFMM Right F Music Mute. 0 = Unmuted, 1 = Muted.

LFMA [5:0] Left F Music Attenuation for the internal Music Synthesizer. The LSB represents –1.5 dB, 000000 = 0 dB and the range is 0 dB to –94.5 dB.

LFMM Left F Music Mute. 0 = Unmuted, 1 = Muted.

[06] I^2S(1) ATTENUATION **DEFAULT = [0x8080]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LS1M	RES	LS1A [5:0]						RS1M	RES	RS1A [5:0]					

RS1A [5:0] Right I^2S(1) Attenuation register. The LSB represents –1.5 dB, 000000 = 0 dB and the range is 0 dB to –94.5 dB.

RS1M	Right I^{2}S(1) Mute. 0 = Unmuted, 1 = Muted.
LS1A [5:0]	Left I^{2}S(1) Attenuation register. The LSB represents –1.5 dB, 000000 = 0 dB and the range is 0 dB to –94.5 dB.
LS1M	Left I^{2}S(1) Mute. 0 = Unmuted, 1 = Muted.

[07] I^{2}S(0) ATTENUATION **DEFAULT = [0x8080]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LS0M	RES	LS0A [5:0]						RS0M	RES	RS0A [5:0]					

RS0A [5:0]	Right I^{2}S(0) Attenuation register. The LSB represents –1.5 dB, 000000 = 0 dB and the range is 0 dB to –94.5 dB.
RS0M	Right I^{2}S(0) Mute. 0 = Unmuted, 1 = Muted.
LS0A [5:0]	Left I^{2}S(0) Attenuation register. The LSB represents –1.5 dB, 000000 = 0 dB and the range is 0 dB to –94.5 dB.
LS0M	Left I^{2}S(0) Mute. 0 = Unmuted, 1 = Muted.

[08] PLAYBACK BASE COUNT **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
PBC [15:8]								PBC [7:0]							

PBC [15:0] Playback Base Count.This register is for loading the Playback DMA Count. Writing a value to this register also loads the same data into the Playback Current Count register. You must load this register when Playback Enable (PEN) is de-asserted. When PEN is asserted, the Playback Current Count decrements once for every four-bytes which are transferred via a DMA cycle. The next transfer, after zero is reached in the Playback Current Count. will generate an interrupt and will reload the Playback Current Count with the value in the Playback Base Count. The Playback Base Count should always be programmed to Number-Bytes divided by four, minus one ((Number-Bytes/4) –1). The circular software DMA buffer must be divisible by four to ensure proper operation.

[09] PLAYBACK CURRENT COUNT **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
PCC [15:8]								PCC [7:0]							

PCC [15:0] Playback Current Count register. Contains the current Playback DMA Count. Reads and Writes must be done when PEN is de-asserted.

[10] CAPTURE BASE COUNT **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CBC [15:8]								CBC [7:0]							

CBC [15:0] Capture Base Count. This register is for loading the Capture DMA Count. Writing a value to this register also loads the same data into the Capture Current Count register. Loading must be done when Capture Enable (CEN) is de-asserted. When CEN is asserted, the Capture Current Count decrements once for every four-bytes which are transferred via a DMA cycle. The next transfer, after zero is reached in the Capture Current Count, will generate an interrupt and will reload the Capture Current Count with the value in the Capture Base Count. The Capture Base Count should always be programmed to Number-Bytes divided by four, minus one ((Number-Bytes/4) –1). The circular software DMA buffer must be divisible by four to ensure proper operation.

[11] CAPTURE CURRENT COUNT **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CCC [15:8]								CCC [7:0]							

CCC [15:0] Capture Current Count register. Contains the current Capture DMA Count. Reading and Writing must be done when CEN is de-asserted.

[12] TIMER BASE COUNT **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TBC [15:8]								TBC [7:0]							

TBC [15:0] Timer Base Count. Register for loading the Timer Count. Writing a value to this register also loads the same data into the Timer Current Count register. Loading must be done when Timer Enable (TE) is de-asserted. When TE is asserted, the Timer Current Count register decrements once for every specified time period. The time period

(10 µs or 100 ms) is programmed via the PTB bit in WS[44]. When TE is asserted, the Timer Current Count decrements once every time period. The next count, after zero is reached in the Timer Current Count register, will generate an interrupt and will reload the Timer Current Count register with the value in the Timer Current Count register.

[13] TIMER CURRENT COUNT **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TCC [15:8]								TCC [7:0]							

TCC [15:0] Timer DMA Current Count register. Contains the current timer count. Reading and Writing must be done when TE is de-asserted.

[14] MASTER VOLUME ATTENUATION **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LMVM	RES		LMVA [4:0]					RMVM	RES		RMVA [4:0]				

RMVA [4:0] Right Master Volume Attenuation. The LSB represents –1.5 dB, 00000 = 0 dB and the range is 0 dB to –46.5 dB. This register is added with the HARDWARE VOLUME BUTTON MODIFIER to produce the final DAC Master Volume attenuation level. See HARDWARE VOLUME BUTTON MODIFIER description for more details.

RMVM Right Master Volume Mute. 0 = Unmuted, 1 = Muted.

LMVA [4:0] Left Master Volume Attenuation. The LSB represents –1.5 dB, 00000 = 0 dB and the range is 0 dB to –46.5 dB. This register is added with the HARDWARE VOLUME BUTTON MODIFIER to produce the final DAC Master Volume attenuation level. See HARDWARE VOLUME BUTTON MODIFIER description for more details.

LMVM Left Master Volume. Mute 0 = Unmuted, 1 = Muted.

[15] CD GAIN/ATTENUATION **DEFAULT = [0x8888]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LCDM	RES		LCDA [4:0]					RCDM	RES		RCDA [4:0]				

RCDA [4:0] Right CD Attenuation. The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB.

RCDM Right CD Mute. 0 = Unmuted, 1 = Muted.

LCDA [4:0] Left CD Attenuation. The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB.

LCDM Left CD Mute. 0 = Unmuted, 1 = Muted.

[16] SYNTH GAIN/ATTENUATION **DEFAULT = [0x8888]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LSYM	RES		LSYA [4:0]					RSYM	RES		RSYA [4:0]				

RSYA [4:0] Right SYNTH Attenuation.The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB.

RSYM Right SYNTH Mute. 0 = Unmuted, 1 = Muted.

LSYA [4:0] Left SYNTH Attenuation. The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB.

LSYM Left SYNTH Mute. 0 = Unmuted, 1 = Muted.

[17] VID GAIN/ATTENUATION **DEFAULT = [0x8888]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LVDM	RES		LVDA [4:0]					RVDM	RES		RVDA [4:0]				

RVDA [4:0] Right VID Attenuation. The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB.

RVDM Right VID Mute. 0 = Unmute, 1 = Muted.

LVDA [4:0] Left VID Attenuation. The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB.

LVDM Left VID Mute. 0 = Unmuted, 1 = Muted.

[18] LINE GAIN/ATTENUATION **DEFAULT = [0x8888]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LLM	RES		LLA [4:0]					RLM	RES		RLA [4:0]				

RLA [4:0] Right LINE Attenuation. The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB.

RLM Right Line Mute. 0 = Unmuted, 1 = Muted.

LLA [4:0] Left LINE Attenuation. The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB.

LLM Left Line Mute. 0 = Unmuted, 1 = Muted.

[19] MIC/MONO_IN GAIN/ATTENUATION **DEFAULT = [0x8888]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MCM	M20	RES	MCA [4:0]					MM	RES		MA [4:0]				

MA [4:0]	MONO_IN Attenuation. The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB.
MM	MONO_IN Mute.
MCA [4:0]	Microphone Attenuation. The LSB represents –1.5 dB, 0000 = +12 dB and the range is ±12 dB to –34.5 dB.
M20	Microphone 20 dB Gain. The M20-bit enables the Microphone +20 dB gain stage.
MCM	Microphone Mute.

[20] ADC SOURCE Select and ADC PGA **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
LAGC	LAS [2:0]			LAG [3:0]				RAGC	RAS [2:0]			RAG [3:0]			

RAG [3:0]	Right ADC Gain Control ADC source select and GAIN. For GAIN, LSB represents +1.5 dB, 0000 = 0 dB and the range is 0 dB to +22.5 dB.
RAGC	Right Automatic Gain Control (AGC) Enable, 0 = Enabled, 1 = Disabled.
LAG [3:0]	Left ADC Gain Control ADC source select and GAIN. For GAIN, LSB represents +1.5 dB, 0000 = 0 dB and the range is 0 dB to +22.5 dB.
LAGC	Left Automatic Gain Control (AGC) Enable, 0 = Enabled, 1 = Disabled.

RAS [2:0]	ADC Right Input Source	LAS [2:0]	ADC Left Input Source
000	R_LINE	000	L_LINE
001	R_OUT	001	L_OUT
010	R_CD	010	L_CD
011	R_SYNTH	011	L_SYNTH
100	R_VID	100	L_VID
101	Mono Mix	101	MIC
110	Reserved	110	MDM_IN
111	Reserved	111	Reserved

[32] CHIP CONFIGURATION **DEFAULT = [0x00F0]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
WSE	CDE	RES	CNP	RES		IME	IMR	COF [3:0]				I^2SF1 [1:0]		I^2SF0 [1:0]	

I^2SF0 [1:0] I^2S Port Configuration for serial data type.
I^2SF1 [1:0]

00	Disabled
01	Right Justified
10	I^2S Justified
11	Left Justified

COF [3:0]	Clock Output Frequency. Programmable clock output on PCLKO pin is determined using the following formula PCLKO = $256 \times SS[38]/2^{COF}$ where COF = 0:11. If COF > 11, then PCLKO is disabled.
IMR	ISA Modem Enable. Set to "1" for host based modem.
IME	ISA Moden Resync. Write "1" to resynchronize modem.
CNP	Capture not equal to Playback. 0 Capture = Playback. The capture sample rate is determined by the playback sample rate in SS Indirect Register [02]. 1 Capture not equal to Playback
CDE	CD Enable, Set to "1" when a CD player is connected to I^2S (0).
WSE	Sound System Enable. 0 = Sound Blaster Mode. 1 = Sound System Mode under Windows.

Note: When in Sound Blaster Mode, the Codec ADC and DAC channels will be used solely for converting Sound Blaster data.

[33] DSP CONFIGURATION **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
DS1	DS0	DIT	DME	DMR	ADR	I1T	I0T	CPI	PBI	FMI	I1I	I0I	DFS [2:0]		

DFS [2:0] DSP Frame Sync Source. Sets the DSP Port Frame Sync according to the following source.
000—Maximum Frame Rate
001—$I^2S(0)$ Sample Rate
010—$I^2S(1)$ Sample Rate
011—Music Synthesizer Sample Rate
100—Sound System Playback Sample Rate
101—Sound System Capture Sample Rate
111—Reserved

I0I $I^2S(0)$ Data Intercept. 0 = Disable, 1 = Intercept $I^2S(0)$ Data Enabled.

I1I $I^2S(1)$ Data Intercept. 0 = Disable, 1 = Intercept $I^2S(1)$ Data Enabled.

FMI FM Music Synthesizer Data Intercept. 0 = Disable, 1 = Intercept FM Music Data Enabled.

PBI Playback Data Intercept. 0 = Disable, 1 = Intercept Playback Data Enabled.

CPI Capture Data Intercept. 0 = Disable, 1 = Intercept Capture Data Enabled.

I0T $I^2S(0)$ Takeover Data. 0 = Disable, 1 = Enabled.

I1T $I^2S(1)$ Takeover Data. 0 = Disable, 1 = Enabled.

ADR Audio Resync. Writing “1” causes all FIFOs in the DSP port to be re-initialized.

DMR DSP Modem Resync. Write to “1” to re-synchronize modem.

DME DSP Modem Enable. Set to “1” for DSP modem.

DIT DSP Interrupt. A write to this bit causes an ISA interrupt if DIE is asserted.

DS0 DSP Mailbox 0 Status. 0 = last access indicates read, 1 = last access indicates write.

DS1 DSP Mailbox 1 Status. 0 = last access indicates read, 1 = last access indicates write.

[34] FM SAMPLE RATE **DEFAULT = [0x5622]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
FMSR [15:8]								FMSR [7:0]							

FMSR [15:0] F Music Sample Rate register. The sample rate can be programmed from 4 kHz to 27.6 kHz in 1 hertz increments.

[35] $I^2S(1)$ SAMPLE RATE **DEFAULT = [0xAC44]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
S1SR [15:8]								S1SR [7:0]							

S1SR [15:0] $I^2S(1)$ Sample Rate register. The sample rate can be programmed from 4 kHz to 55.2 kHz in 1 hertz increments. Programming this register has no effect unless I^2SF1 [1:0] is enabled.

[36] $I^2S(0)$ SAMPLE RATE **DEFAULT = [0xAC44]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
S0SR [15:8]								S0SR [7:0]							

S0SR [15:0] $I^2S(0)$ Sample Rate register. The sample rate can be programmed from 4 kHz to 55.2 kHz in 1 hertz increments. Programing this register has no effect unless I^2SF0 [1:0] is enabled.

[37] MODEM SAMPLE RATE **DEFAULT = [0x1C20]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MSR [15:8]								MSR [7:0]							

MSR [15:0] MODEM Sample Rate register. The sample rate can be programmed from 4 kHz to 13.8 kHz in 1 hertz increments. This register is only valid when IME(ISA MODEM ENABLE) or DME(DSP MODEM ENABLE) is asserted.

[38] PROGRAMMABLE CLOCK RATE **DEFAULT = [0xAC44]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
PCR [15:8]								PCR [7:0]							

PCR [15:0] Programmable Clock Rate register. The clock rate can be programmed from 25 kHz to 50 kHz in 1 hertz increments. This register is only valid when the COF bits in SS[32] are set for the multiplier factor. PCLKO = $256 \times SS[38]/2^{COF}$. See SS[32] for determining the value of COF.

[39] MODEM DAC and ADC Attenuation **DEFAULT = [0x8000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MDM		RES	MDA [4:0]					RES				MAG [3:0]			

MAG [3:0] Modem ADC Gain. The LSB represents +1.5 dB and the range is 0 dB to +22.5 dB.
MDA [4:0] Modem DAC Attenuation. The LSB represents 1 dB and the range is 0 dB to –31 dB.
MDM Modem DAC Mute.

[40] MODEM MIX Attenuation **DEFAULT = [0x80XX]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MMM		RES	MDA [4:0]					RES							

MDA [4:0] MODEM-IN Attenuation. The LSB represents –1.5 dB, 00000 = +12 dB and the range is +12 dB to –34.5 dB
MMM MODEM Mix Mute.

[41] HARDWARE VOLUME BUTTON MODIFIER and STATUS **DEFAULT = [0xXX1B]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RES								VMU	VUP	VDN	BM [4:0]				

BM [4:0] Button Modifier
VDM Volume Down
VUP Volume Up
VMU Volume Mute

This register contains a MASTER VOLUME attenuation offset that can be incremented or decremented via the Hardware Volume Pins. This Register is summed with the MASTER VOLUME attenuation to produce the actual MASTER VOLUME DAC attenuation. A momentary press of greater than 50 ms on the VOLUME-UP pin will cause a decrement (decrease in Attenuation) in this register. Holding the pin for greater than 200 ms will cause an auto-decrement every 200 ms. This is also true for a momentary press of the VOLUME-DOWN pin. A momentary press of both the VOLUME-UP and VOLUME-DOWN causes a mute and no increment or decrement to occur.

When Muted, an un-mute is possible by either a momentary press of both the VOLUME-UP and VOLUME-DOWN pins together, a momentary press of VOLUME-UP (this also causes a volume increase), a momentary press of VOLUME-DOWN (this also causes a volume decrease) or a write of “0” to the VI bit in SS[BASE+1].

[42] DSP MAILBOX 0 **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MB0R [15:8]								MB0R [7:0]							

MB0R [15:0] This register is used to send data and control information to and from the DSP.

[43] DSP MAILBOX 1 **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MB1R [15:8]								MB1R [7:0]							

MB1R [15:0] This register is used to send data and control information to and from the DSP.

[44] POWERDOWN and TIMER CONTROL **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CPD	RES	PIW	PIR	PAA	PDA	PDP	PTB	RES							

The AD1815 supports a time-out mechanism used in conjunction with the TIMER BASE COUNT/TIMER CURRENT COUNT registers to generate a powerdown interrupt. This interrupt allows software to powerdown the entire chip by setting the CPD bit. This powerdown control feature lets users program a time interval from 1 ms to approximately 1.8 hours in 1 ms increments. Five powerdown count reload enable bits are used to reload the TIMER CURRENT COUNT from the TIMER BASE COUNT when activity is seen on that particular channel.

Programming Example: Generate Interrupt if No ISA Reads or Writes occur within 15 Minutes.
1) Write [SSBASE+0] with 0x0C ; Write Indirect address for TIMER BASE COUNT “register 12”
2) Write [SSBASE+2] with 0x28 ; Write TIMER BASE COUNT with (15min * 60sec/min * 10) = 0x2328 mili-Seconds
3) Write [SSBASE+3] with 0x23 ; Write High byte of TIMER BASE COUNT
4) Write [SSBASE+0] with 0x2C ; Write Indirect address for POWERDOWN and TIMER CONTROL register
5) Write [SSBASE+2] with 0x00 ; Write Low byte of POWERDOWN and TIMER CONTROL register
6) Write [SSBASE+3] with 0x30 ; Set Enable bits for PIW & PIR
7) Write [SSBASE+0] with 0x01 ; Write Indirect address for INTERRUPT CONFIG register
8) Write [SSBASE+2] with 0x82 ; Set the TE (Timer Enable) bit
9) Write [SSBASE+3] with 0x20 ; Set the TIE (Timer Interrupt Enable) bit

PTB Powerdown Time Base. 1 = timer set to 100 ms, 0 = timer set to 10 µs.

PDP Powerdown count reload on DSP Port enabled; "1" = Reload count if DSP Port enabled DSP Port enabled defined as:

PDA Powerdown count reload on Digital Activity; "1" = Reload count on Digital Activity Digital Activity is defined as: Any activity on (I^2S0, I^2S1, FM or PLAYBACK).

PAA Powerdown count reload on Analog Activity; "1" = Reload count on Analog Activity; Analog Activity is defined as: Any analog input un-muted (LINE, CD, SYNTH, MIC, MONO) or MASTER VOLUME un-muted.

PIR Powerdown count reload on ISA Read; "1" = Reload count on ISA read; ISA Read is defined as: A read from any active logical device inside the AD1815

PIW Powerdown count reload on ISA Write; "1" = Reload count on ISA write; ISA Write defined as: A write to any active logical device inside the AD1815

CPD Chip Powerdown
1 Powerdown;
0 Powerup

For Powerup, software should POLL the [SSBASE+0] CRY bit for "1" before writing or reading any logical device.

[45] VERSION ID **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
VER [15:8]								VER [7:0]							

[46] RESERVED **DEFAULT = [0x0000]**

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RES								RES							

Test register. Should never be written or read under normal operation

SB Pro; Adlib Registers

The AD1815 contains sets of ISA Bus registers (ports) that correspond to those used by the Sound Blaster Pro audio card from Creative Labs and the AdLib audio card from AdLib Multimedia. Table IX lists the ISA Bus Sound Blaster Pro registers. Table X lists the ISA Bus AdLib registers. Because the AdLib registers are a subset of those in the Sound Blaster card, you can find complete information on using both of these registers in the *Developer Kit for Sound Blaster Series, 2nd ed. ©1993,* Creative Labs, Inc., 1901 McCarthy Blvd., Milpitas, CA 95035.

Table IX. Sound Blaster Pro ISA Bus Registers

Register Name	ISA Bus Address
Music0: Address (w), Status (r)	0x(SB Base) Relocatable in range 0x010 – 0x3F0
Music0: Data (w)	0x(SB Base+1)
Music1: Address (w)	0x(SB Base+2)
Music1: Data (w)	0x(SB Base+3)
Mixer Address (w)	0x(SB Base+4)
Mixer Data (w)	0x(SB Base+5)
Reset (w)	0x(SB Base+6)
Music0: Address (w)	0x(SB Base+8)
Music0: Data (w)	0x(SB Base+9)
Input Data (r)	0x(SB Base+A)
Status (r), Output Data (w)	0x(SB Base+C)
Status (r)	0x(SB Base+E)

Table X. Adlib ISA Bus Registers

Register Name	ISA Bus Address
Music0: Address (w), Status (r)	0x(Adlib Base) Relocatable in range 0x008 – 0x3F8
Music0: Data (w)	0x(Adlib Base+1)
Music1: Address (w)	0x(Adlib Base+2)
Music1: Data (w)	0x(Adlib Base+3)

MIDI and MPU-401 Registers

The AD1815 contains a set of ISA Bus registers (ports) that correspond to those used by the ISA bus MIDI audio interface cards. Table XI lists the ISA Bus MIDI registers. These registers support commands and data transfers described in *MIDI 1.0 Detailed Specification and Standard MIDI Files 1.0,* ©1994, MIDI Manufacturers Association, PO Box 3173 La Habra, CA 90632-3173.

Table XI. MIDI ISA Bus Registers

Register Name	Address
MIDI Data (r/w)	0x(MIDI Base) Relocatable in range 0x008 to 0x3F8
MIDI Status (r), Command (w)	0x(MIDI Base+1)

0x(MIDI Base+1)

BIT	7	6	5	4	3	2	1	0
STATE	1	0	0	0	0	0	0	0
NAME	DRR	DSR	RESERVED					

DSR (R)	Data Send Ready. When read, this bit indicates that you can (0) or cannot (1) write to the MIDI Data register. (Full = 1, Empty = 0)
DRR (R)	Data Receive Ready. When read, this bit indicates that you can (0) or cannot (1) read from the MIDI Data register. (Unreadable = 1, Readable = 0)
CMD [7:0] (W)	MIDI Command. Write MPU-401 commands to bits [7:0] of this register.

NOTES

The AD1815 *only* supports the MIDI 0xFF (reset) and 0x3F (pass-through mode) commands. The controller powers setup for intelligent MIDI mode, but must be put in pass-through mode. To start MIDI operations, send a reset command (0xFF) and then send a pass-through mode command (0x3F). The MIDI data register contains an acknowledge byte (0xFE) after each command transfer.

All commands return an ACK byte in “smart” mode.

Status commands (0xAx) return ACK and a data byte; all other commands return ACK.

All commands except reset (0xFF) are ignored in UART mode. No ACK bytes are returned.

“Smart” mode data transfers are not supported.

Game Port Registers

The AD1815 contains a Game Port ISA Bus Register that corresponds to the game port described in the PnP specification.

Table XII. Game Port ISA Bus Registers

Register Name	Address
Game Port I/O	0x(Game Port Base+0 to Game Port Base+7 Relocatable in the range 0x100 to 0x3F8

APPENDIX A

Additional Plug and Play Programming Information

The following is an example of the programming steps for a quick Plug and Play setup. This example is intended for use in evaluating the AD1815. The example PnP code may cause conflicts with other PnP devices.

↓\1815DIG\PAD_IORB
↓\1815DIG\PAD_IOWB
↓\1815DIG\XPC_AEN
↓\1815DIG\XPC_A<11:0> (x)
↓\1815DIG\XPC_DATA<7:0> (x)

1	0	0	279	00	Write the Plug and Play key to get the device into “SLEEP”
1	0	0	279	00	(Device starts in “Wait For Key” state)
1	0	0	279	00	
1	0	0	279	6A	
1	0	0	279	B5	
1	0	0	279	DA	
1	0	0	279	ED	
1	0	0	279	F6	
1	0	0	279	FB	
1	0	0	279	7D	
1	0	0	279	BE	
1	0	0	279	DF	
1	0	0	279	6F	
1	0	0	279	37	
1	0	0	279	1B	
1	0	0	279	0D	
1	0	0	279	86	↑
1	0	0	279	C3	Plug and Play Initiation Key
1	0	0	279	61	↓
1	0	0	279	B0	
1	0	0	279	58	
1	0	0	279	2C	
1	0	0	279	16	
1	0	0	279	8B	
1	0	0	279	45	
1	0	0	279	A2	
1	0	0	279	D1	
1	0	0	279	E8	
1	0	0	279	74	
1	0	0	279	3A	
1	0	0	279	9D	
1	0	0	279	CE	
1	0	0	279	E7	
1	0	0	279	73	
1	0	0	279	39	
1	0	0	279	03	WAKE CSN (Card Select Number) 0
1	0	0	A79	00	goes to “ISOLATION”
1	0	0	279	00	Program read port = 0x36B,
1	0	0	A79	DA	and go to “CONFIG” state
1	0	0	279	06	Program CSN = B4
1	0	0	A79	B4	
1	0	0	279	07	Set LDN = 0 to program SB/CODEC/OPL3
1	0	0	A79	00	
1	0	0	279	60	Program I/O range 0, Sound Blaster = 0x220
1	0	0	A79	02	MSB
1	0	0	279	61	
1	0	0	A79	20	LSB
1	0	0	279	62	Program I/O Range 0, OPL3 = 0x388
1	0	0	A79	03	MSB
1	0	0	279	63	
1	0	0	A79	88	LSB
1	0	0	279	64	Program I/O Range 0, CODEC = 0x130
1	0	0	A79	01	MSB
1	0	0	279	65	
1	0	0	A79	30	LSB

↓\1815DIG\PAD_IORB	↓\1815DIG\PAD_IOWB	↓\1815DIG\XPC_AEN	↓\1815DIG\XPC_A<11:0> (x)	↓\1815DIG\XPC_DATA<7:0> (x)	
1	0	0	279	74	Program SB/CODEC Playback DMA
1	0	0	A79	01	to DMA channel 1.
1	0	0	279	75	Program CODEC Capture DMA
1	0	0	A79	00	to DMA channel 0. Program to 4 for SDC mode
1	0	0	279	70	Program SB/CODEC interrupt
1	0	0	A79	07	to IRQ7.
1	0	0	279	30	Enable SB/CODEC/OPL3.
1	0	0	A79	01	
1	0	0	279	07	Set LDN = 1 to program MPU-401.
1	0	0	A79	01	
1	0	0	279	60	Program I/O range 0, MPU-401 = 0x330
1	0	0	A79	03	MSB
1	0	0	279	61	
1	0	0	A79	30	LSB
1	0	0	279	70	Program MPU-401 interrupt
1	0	0	A79	0F	to IRQ15.
1	0	0	279	30	Enable MPU-401.
1	0	0	A79	01	
1	0	0	279	07	Set LDN = 2 to program GAME
1	0	0	A79	02	
1	0	0	279	60	Program I/O range 0, GAME = 0x200
1	0	0	A79	02	MSB
1	0	0	279	61	
1	0	0	A79	00	LSB
1	0	0	279	30	Enable GAME.
1	0	0	A79	01	
1	0	0	226	01	Put SB in reset (good to do while running CODEC tests)

Plug and Play Key & "Alternate Key" Sequences

One additional feature of the AD1815 is an alternate programming method which is used, for example, if a BIOS wants to assume control of the AD1815 and present DEVNODES to the OS (rather than having the device participate in Plug and Play enumeration). The following technique can be used.

Instead of the normal 32 byte Plug and Play key sequence, an alternate 126 byte key is used. After the 126 byte key, the AD1815 device will transition to the Plug and Play "config" state. It can then be programmed as usual using the standard Plug and Play ports. After programming, the AD1815 should be sent to the Plug and Play "WFK" (wait for key) state. Once the AD1815 has seen the alternate key, it will no longer parse for the Plug and Play key (and therefore never participate in Plug and Play enumeration). It can be reprogrammed by reissuing the alternate key again.

Both the Plug and Play key and the alternate key are sequences of writes to the Plug and Play address register, 0x279. Below are the ISA data values of both keys.

This is the standard Plug and Play sequence:

6a b5 da ed f6 fb 7d be df 6f 37 1b 0d 86 c3 61
b0 58 2c 16 8b 45 a2 d1 e8 74 3a 9d ce e7 73 39

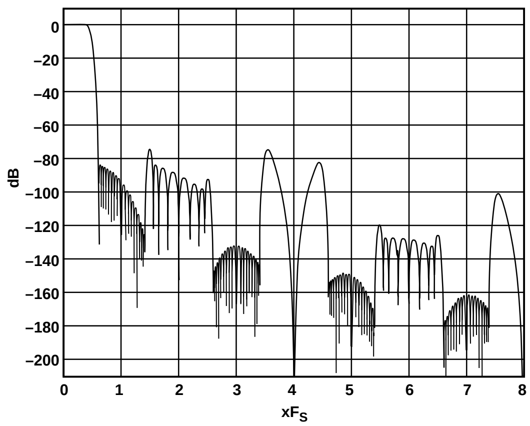
This is the longer, 126-byte alternate key. It is generated by the function:

f[n+1] = (f[n] >> 1) | (((f[n] ^ (f[n]>>1)) & 0x01) <<
6) f[0] = 0x01

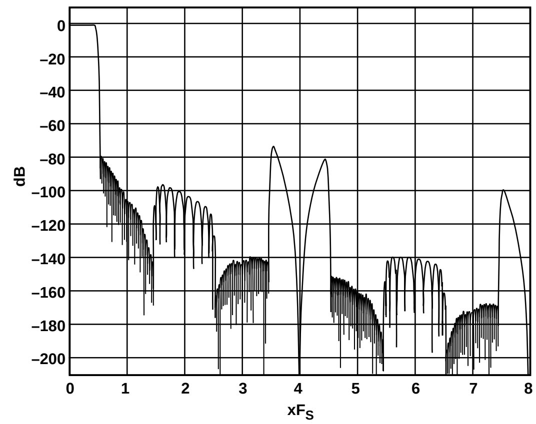
01 40 20 10 08 04 02 41 60 30 18 0c 06 43 21 50
28 14 0a 45 62 71 78 3c 1e 4f 27 13 09 44 22 51
68 34 1a 4d 66 73 39 5c 2e 57 2b 15 4a 65 72 79
7c 3e 5f 2f 17 0b 05 42 61 70 38 1c 0e 47 23 11
48 24 12 49 64 32 59 6c 36 5b 2d 56 6b 35 5a 6d
76 7b 3d 5e 6f 37 1b 0d 46 63 31 58 2c 16 4b 25
52 69 74 3a 5d 6e 77 3b 1d 4e 67 33 19 4c 26 53
29 54 2a 55 6a 75 7a 7d 7e 7f 3f 1f 0f 07

Reference Designs and Device Drivers

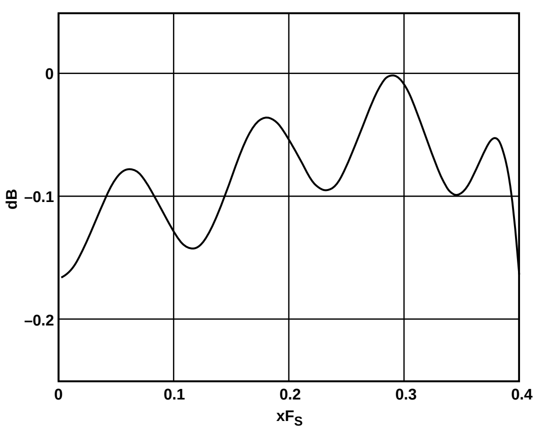
Reference designs and device drivers using the AD1815 are available via the Analog Devices Home Page on the World Wide Web at http://www.analog.com. Reference designs may also be obtained by contacting your local Analog Devices Sales representative or authorized distributor.



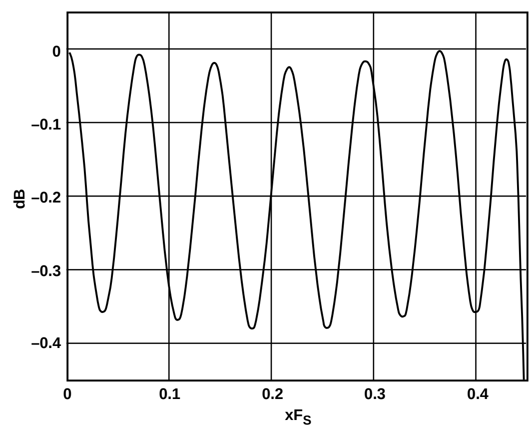
a. DAC Audio



c. DAC Modem

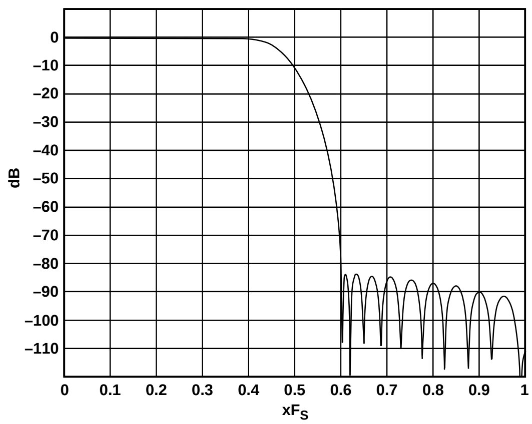


b. DAC Audio Passband

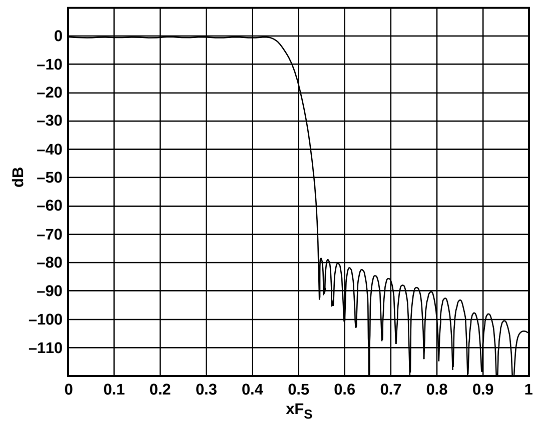


d. DAC Modem Passband

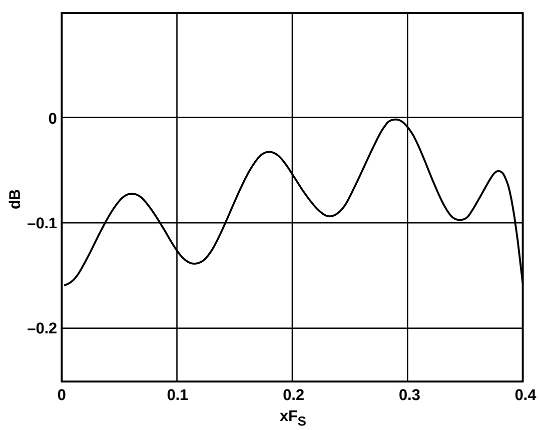
Figure 16. AD1815 Frequency Response Plots (Full-Scale Line-Level Input, 0 dB Gain). The Plots Do Not Reflect the Additional Benefits of the AD1815 Analog Filters. Out-of-Band Images Will Be Attenuated by an Additional 31.4 dB at 100 kHz.



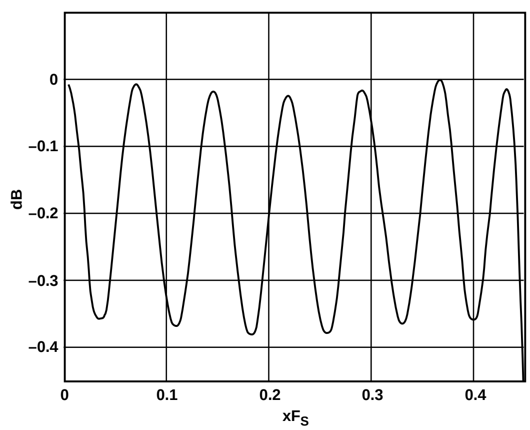
e. ADC Audio



g. ADC Modem



f. ADC Audio Passband



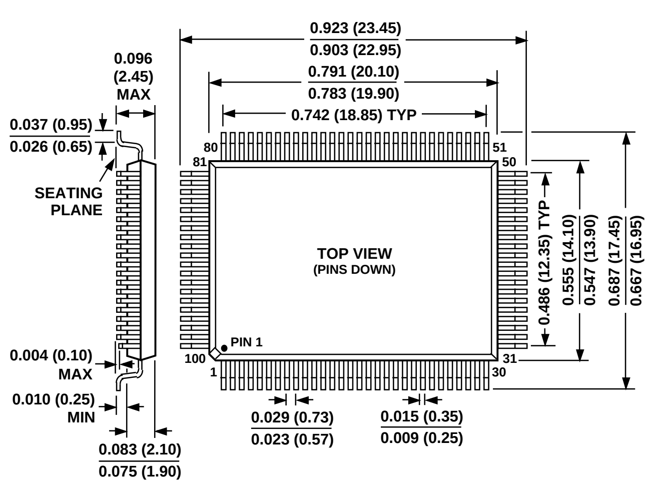
h. ADC Modem Passband

Figure 16. AD1815 Frequency Response Plots (Full-Scale Line-Level Input, 0 dB Gain). The Plots Do Not Reflect the Additional Benefits of the AD1815 Analog Filters. Out-of-Band Images Will Be Attenuated by an Additional 31.4 dB at 100 kHz.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

100-Lead PQFP (S-100)



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