Application Note 113
100 MHz Bus Design

APPLICATION NOTE 101

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Summary

At high bus frequencies, motherboard design becomes geometrically more difficult since a multiplicity of design factors interact to defeat the integrity of the design. Circuit traces become transmission lines, coupling occurs between traces, and power supplies require additional decoupling. Shorter lead length increases circuit density and produces greater thermal concerns. Clock generator location and clock-line layout becomes critical. Using circuit simulation and other sophisticated design techniques and by following the recommendations given here, high speed design can be made easier and more reliable.

This document applies to all Cyrix CPU unless otherwise specified.

Introduction

In recent years, the Cyrix x86 family of processors has gained increased performance due, in part, to higher bus speeds. This application note is intended to help motherboard designers properly design a motherboard to accommodate a Cyrix 6x86MX operating at 100 MHz bus. Background material presented in Cyrix Application Note 101 *75 MHz Board Design* also apply to 100 MHz bus designs.

In working with high frequencies special attention must be paid to:

- Trace to trace capacitance
- Transmission line effects
- Power supply decoupling
- Thermal constraints
- Clock distribution

Trace to Trace Capacitance

Capacitor impedance decreases frequency. For example, the impedance (Z) of 5 pf capacitance (C) between board traces goes from 1.6 Kohms at 20 MHz to 318 ohms at 100 MHz as shown in the equation below:

$$Z = \frac{1}{j\omega C} = \frac{1}{2j\pi fC'}$$

In higher speed designs effects of cross connection interference will be digital noise appearing at what seems to be at random. Setup and hold times are particularly aggravated and this may lead to unstable operation.

Long parallel bus runs between devices, can cause noise and cross-talk problems and can be largely prevented. These problems can be largely prevented by using short traces and avoiding long parallel bus runs. Twisted wire pairs can be simulated using vias and

jump-overs every one or two centimeters. Boards with lower dielectric coefficients have less lead-to-lead capacitance. Increasing the space between conductors, and increasing thickness of the board between planes decreases coupling.

Transmission Line Effects and Reflection

It is important to keep the source impedance, line impedance and load/receiver impedance the same to reduce line reflections. This is clearly seen when the voltage is source is a step function. However, when the source voltage changes so that there is a noticeable rise time associated with it, the reflections are not distinctly identifiable, since the source wave may still be rising during the reflections. This will cause the reflected waves to take on a more rounded shape, which gives rise to the phenomenon commonly known as overshoot, undershoot, and ringing.

Other line characteristics that affect clean signal transmission are turning radii of wires, and extraneous vias in a line. Ninety degree turns and vias in a path create discontinuities that result in transmission line impedance mismatches. To minimize these effects, use as few vias as possible, and use 45 degree turns instead of 90 degree turns.

Transmission Line Termination

Several common ways to reduce reflections on a transmission line include the use of diode clamping, series dampening resistors, balanced and unbalanced termination resistors, and resistive-capacitive termination.

Diode Clamping is a common technique where a pair of normally reverse biased diodes are connected from the end of a transmission line to either Vcc or ground. This method does not prevent the reflection, but limits the overshoot on the first reflection. Successive reflections back will not be suppressed since they won't fall above the diode's bias requirement.

Series resistive dampening is another technique used to limit ringing and reflections. By putting a small valued resistor (10 to 30 ohms) in series with the drivers, the rise time of the signal at the transmission line is increased due to the time

required to charge the line capacitance. The series resistors can limit the drive levels on a heavily loaded line to the point where a logical high level may not have the noise immunity headroom for the circuit being driven.

Another method of terminating a transmission line is by the use of unbalanced termination resistors. This technique involves placing resistors at the end of the transmission line to Vcc or more preferably the ground bus. The unbalanced termination resistor (Zt) is selected so that when it is connected in parallel across the receiver (load) impedance (Zr) the resulting impedance is equal to the transmission line impedance. Selecting a termination resistor based on the transmission line impedance will often not only create a mismatch, but will heavily load down the line driver, possibly holding the steady state level of the signal below the required high level voltage. It also has the effect of forcing a normally tri-stated bus into a logical one or zero state, and increasing the current requirements during steady state signaling.

Decoupling Capacitors

There are usually three values of decoupling capacitors used on motherboards, each addressing a different frequency spectrum required of the power supply. The large, bulk decoupling capacitors, which usually have a high ESR are placed on a board to compensate for voltage regulator recovery delays and long leads from the power supply. The next smaller valued capacitors, usually in the 0.1 pF range of value, is used to help decouple some of the higher frequency components that the self-inductance of the larger, bulk capacitors cannot deliver in microsecond times. At higher bus speeds, a third type of capacitor usually 0.01 μF with very low ESR (about 500 pH) is used.

Clock Distribution

As clock frequency goes up, clock-skew tolerance through the motherboard drops dramatically. Clock skew results from using different clock drivers and the existence of different clock path lengths. Since the chipsets, CPU, and peripheral components all use the same clock, it is critical that the clock signal be correctly distributed in a way that minimizes skew from chip-to-chip. By planning a clock distribution network early in the layout process the distance to each component can be designed to be equal and minimal. A small source resistor is also sometimes included in the clock line to help with transmission matching. In certain cases the clock line can be isolated and equalized by surrounding the clock trace by two ground traces.

100 MHz Bus AC Specifications and Analysis for the 6x86MX Processor

The 100 MHz Bus AC specifications are contained in *100 MHz Bus 6x86MX Data Book Addendum*. The following tables summarize the setup timing analysis of the 100 MHz components of6x86MX processor system operating with a 100 MHz bus.

The maximum valid delay values are taken from the *100 MHz Bus 6x86MX Data Book Addendum*.

The system delay value represents the worst case propagation delay. It is assumed that there is a:

- Maximum clock jitter of 250 ps
- Maximum clock skew of 500 ps
- 1.75 ns point to point trace delay or 2.5 ns muti-load trace delay

The cycle time is either one or two clock periods depending on path length.

The margin is the cycle time minus the sum of the maximum valid delay, the system delay and the minimum setup delay.

The load is the number of nodes including the driver.

TABLE 1. PROCESSOR TO NORTHBRIDGE TIMING ANALYSIS

SIGNAL	CPU MAX. VALID DELAY (NS)	SYSTEM DELAY (NS)	CYCLE TIME (NS)	MARGIN + NB SETUP (NS)	LOADS (INCLUDES SOURCE)	COMMENTS
A[31:3]	4.0	3.25	20	12.75	4	Note 1
ADS#	4.0	2.5	10	3.50	2	
BE[7:0]#	4.0	3.25	20	12.75	3	
CACHE#	4.0	2.5	20	13.50	2	
D/C#	4.0	2.5	10	3.5	2	
D[63:0]	4.0	2.5	10	2.25	3	
HITM#	4.0	2.5	20	13.5	2	
LOCK#	4.0	2.5	10	3.5	2	
M/IO#	4.0	2.5	10	3.5	2	
SMIACT#	4.0	2.5	20	13.5	2	
W/R#	4.0	2.5	10	3.5	2	

Note 1: The address bus bits not routed to PBSRAM chips are two load traces.

TABLE 2. PROCESSOR TO PBSRAM TIMING ANALYSIS

SIGNAL	CPU MAX. VALID DELAY (NS)	SYSTEM DELAY (NS)	CYCLE TIME (NS)	MARGIN + PBSRAM SETUP (NS)	LOADS (INCLUDES SOURCE)	COMMENTS
A[n:3]	4.0	3.25	10	2.75	4	Note 1
ADSC#	4.0	2.5	10	2.75	2	
BE[7:0]#	4.0	3.25	10	2.75	3	
D[63:0]	4.0	2.5	10	2.25	3	

Note 1: The address bus bits not routed to PBSRAM chips are two load traces.

TABLE 3. NORTHBRIDGE TO PROCESSOR TIMING ANALYSIS

SIGNAL	SYSTEM DELAY (NS)	CYCLE TIME (NS)	CPU SETUP TIME (NS)	MARGIN + NORTH BRIDGE DELAY (NS)	LOADS (INCLUDES SOURCE)	COMMENTS
A[31:3]	3.25	20	3.0	13.75	4	Note 1
AHOLD	2.50	10	3.5	4.0	2	
BOFF#	2.50	10	3.5	4.0	3	
BRDY#	2.50	10	3.0	4.5	2	
D[63:0]	3.25	10	1.7	5.0	3	
EADS#	2.50	10	3.0	4.5	2	
KEN#(INV)	3.25	10	1.7	5.0	2	
NA#	2.50	10	1.7	5.8	2	

Note 1: The address bus bits not routed to PBSRAM chips are two load traces.

TABLE 4. NORTHBRIDGE TO PB SRAM TIMING ANALYSIS

SIGNAL	SYSTEM DELAY (NS)	PBSRAM SETUP TIME (NS)	CYCLE TIME (NS)	MARGIN + NORTH BRIDGE DELAY (PS)	LOADS (INCLUDES SOURCE)	COMMENTS
BWE#	3.25	2.2	10	4.55	3	
CADS#	3.25	2.2	10	4.55	3	
CADV#	3.25	2.2	10	4.55	3	
CEI#	3.25	2.2	10	4.55	3	
COE#	3.25	2.2	10	4.55	3	
D[63:0]	3.25	2.2	10	4.55	3	
GWE#	3.25	2.2	10	4.55	3	

TABLE 5. NORTHBRIDGE TO SDRAM TIMING ANALYSIS

SIGNAL	SYSTEM DELAY (NS)	CYCLE TIME (NS)	SDRAM SETUP TIME (NS)	MARGIN + NB VALID DELAY (NS)	LOADS (INCLUDES SOURCE)	COMMENTS
MA	3.25	20	3.0	13.75	17	Note 1
MCS#	3.25	10	3.0	3.75	5	Note 1
MD[63:0]	3.25	10	3.0	3.75	5	Note 1
MDQMB[7:0]	3.25	10	3.0	3.75	5	Note 1
SCAS[1:0]	3.25	10	3.0	3.75	9	Note 1
SRAS[1:0]	3.25	10	3.0	3.75	9	Note 1
SWE[1:0]	3.25	10	3.0	3.75	9	Note 1

Note: Load depends on number of DIMMs and SDRAM chips/DIMM

TABLE 6. PBSRAM TO SDRAM DATA OUTPUT TIMING ANALYSIS

SIGNAL	MAX. VALID DELAY (NS)	SYSTEM DELAY (NS)	CYCLE TIME (NS)	MARGIN + SET UP TIME (NS)	LOADS (INCLUDES SOURCE)	COMMENTS
PBSRAM Data to Northbridge						
D[63:0]	5	3.25	10	1.75	3	Note 1
PBSRAM Data to Processor						
D[63:0]	5	3.25	10	1.75	3	Note 2
SDRAM Data to Northbridge						
MD[63:0]	TBD					

Note 1: Applies to L2 cache writeback cycles

Note 2: Applies to L2 cache read cycles.

Hold Time Analysis

Ensure that the minimum output delays of the driver are long enough to meet hold time of the associated receiver(s). The CPU minimum delay output times do not change for 100 MHz bus.

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