CYRIX 5X86 REGISTER ENHANCEMENTS REVEALED

Did you ever wonder how much improvement those 'special features' of the Cyrix 5x86 processor gave? Well, in this study we will investigate the performance enhancing effects of each user configurable register bit settings of the Cyrix 5x86 central processing unit. 36 different benchmark tests were employed to determine the average probable performance enhancement for each feature independently. Many of these register settings, or features, are disabled from the factory by default as a means to increase compatibility with a broad range of motherboards. As the Cyrix 5x86 is a partially downscaled 6x86, many of the conclusions made herein will likely hold true for the Cyrix 6x86 processor.

EXECUTIVE SUMMARY

For the overall performance gain, enabling BTB (branch prediction) showed an 8.5% improvement, LSSER (load/store reordering) showed an 8% improvement, FP FAST (fast floating-point unit) showed a 6% improvement, and MEM_BYP (memory read bypassing) showed a 1.5% improvement. The other features tested were IORT, LINBRST, RSTK, BWRT, LOOP, DTE, WT and showed little to no improvement.

INTRODUCTION

This study adopts the ensuite of benchmarking software utilised in the *Ultimate 486 Benchmark Comparison* as a means to estimate the performance gain per Cyrix feature. These features were enabled/disabled using the IBM M9 Register Utility Version V1.22 (20 May 1996), however other popular programs of the time were the Peter N. Moss Register Bit Enabler Version C2 (12 May 1996) and ET586 Version 1.1 (28 November 1995) by Evergreen Technologies. The IBM utility was chosen because of its graphical user interface in DOS and the ease of enabling bits. Since Windows 98SE was selected for performing Windows-

based benchmarks, a Cyrix NT driver was not needed; features were enabled in DOS prior to booting into Windows 98SE. If special Cyrix 5x86 features are desired in Windows NT and Windows 2000, Evergreen Technologies created ET586NT, which is an NT driver that runs as a device automatically at start-up. Below is a table containing a map of various Cyrix 5x86 register bits (CR0 is not included).

Register & Index	MAPEN	Idx	7	6	5	4	3	2	1	0
Performance Control [PCR0]	1h	20h	**LSSSER** 1	0	0	0	0	**LOOP_EN** 0	BTB_EN 0	**RSTK_EN** 0
Control 1 [CCR1]	xh	C1h	0	0	0	0	MMAC 0	SMAC 0	USE_SMI 1	0
Control 2 [CCR2]	xh	C2h	USE_SUSP 1	**BWRT** 0	0	WT1 1	SUSP_HALT 0	LOCK_NW 1	USE_WBAK 1	0
Control 3 [CCR3]	xh	C3h	MAPEN3 0	MAPEN2 0	MAPEN1 0	MAPEN0 1	SMM_MODE 1	LINBRST 1	NMI_EN 0	SMI_LOCK 0
Control 4 [CCR4]	1h	E8h	0	0	**FP_FAST** 0	DET_E 1	MEM_BYP 1	IORT2 0	IORT1 0	IORT0 0
SMM Address [SMAR0]	xh	CDh	A31 0	A30 0	A29 0	A28 0	A27 1	A26 1	A25 1	A24 0
SMM Address [SMAR1]	xh	CEh	A23 0	A22 0	A21 0	A20 0	A19 1	A18 0	A17 1	A16 0
SMM Address [SMAR2]	xh	CRh	A15 0	A14 0	A13 0	A12 0	SIZE3 0	SIZE2 1	SIZE1 0	SIZE0 1
Power Management [PMR]	1h	F0h	0	0	0	0	0	HLF_CLK 0	CLK1 0	CLK0 1
Device ID0 [DIR0]	xh	FEh	0	0	1	0	1	0	0	1
Device ID1 [DIR1]	xh	FFh	SID3 0	SID2 0	SID1 0	SID0 0	RID3 0	RID2 1	RID1 0	RID0 1

This table represents a snapshot of which Cyrix 5x86 features are set by the motherboard as default. The bolded entries are features which were later enabled using the IBM utility, that is, LSSER is to be changed to 0, LOOP_EN to 1, RSTK_EN to 1, BWRT to 1, and FP_FAST to 1. When enabled, the entirety of these settings constitute *My Default Settings* as noted on the chart in Appendix 2 (column *A*) and below. These settings are considered optimal/stable settings on the employed motherboard, a Biostar MB8433-UUD v3.0 with a Cyrix/IBM 5x86c-100HF running at 133 MHz (2 x 66 MHz) and 3.85 V. This voltage was selected as stable on this particular motherboard, CPU, and cooling environment, however other CPU/motherboard combinations may require a different core voltage for thermal/frequency stability. This stable voltage is typically in the 3.65 – 3.95 V range for 133 MHz operation.

Note that LSSER is optimal when it is set to 0, not 1. A feature is typically said to be enabled when it is set to 1, and disabled when it is set to 0 (except for LSSER, which is opposite). WT and IORT, when set to 0, are also theoretically the most optimal setting, however they exist mainly for reasons of cross-platform stability.

BIT ENABLING PROGRAMS

Since most motherboard manufacturers did not enable the special features of the Cyrix 5x86 in the BIOS, bit enabling software programs were generally required, however one manufacturer (PC Chips M919) allowed for two such features to be enabled in the BIOS (LINBRST and LSSER). While it is not well documented why more companies didn't follow suit, is likely due to time constraints and the fact that the 486 was considered a low-end, low-priority item by mid-1996. Unfortunately, even the latest BIOS update for the Biostar MB8433-UUD, dated May 1996, does not include a user adjustable enabler for Cyrix features.

While the IBM utility uses a GUI as a means to enable the special features, the Peter Moss utility uses on/off flags to enable features, for example, to enable BTB_EN and RSTK_EN type, `5x86.exe /BTB_EN=on /RSTK_EN=on`. The Evergreen utility is a little more cumbersome to use since you need to type in HEX values for an entire register (8 bits, or features, per register). For example, for the performance control register (PCR0), if you only want LOOP and RSTK enabled (and the other bits of this register disabled), you'd need to type, `ET586.exe /PCR0=5`, where 5 is hexadecimal digit. From the above chart, 00000101 in binary representation

is equal to 5 in hexadecimal. Even more confusing is that the Windows NT/2000 driver from Evergreen Technologies requires its units to be in decimal. It just so happens that, in this case, 5 in hexadecimal is also 5 in decimal, though this is not always the case. Screenshots of the various bit enabler programs are shown in Appendix 1.

There exists a fourth bit enabling program called CyrixGo, or Free5x86, however it is very limited in which features it can enable.

TEST METHODOLOGY

The testing scheme used herein is such that all features known to be stable with the employed CPU/motherboard combination were enabled (referred to as *DEFAULT SETTINGS* in column *A* of Appendix 2, and *My Test Settings* in the *Test Settings* section of this report). Then a specific feature was turned off (i.e. LSSER = 1, or LOOP = 0, or RSTK = 0, etc.), and the decrease in benchmark scores were tabulated in an adjacent column (column *B*, LSSER). Before testing the next feature (column *C*, LOOP), the previous feature was re-enabled (LSSER set back to 0).

The reason for testing this way, that is, always having all of the most optimal features enabled except for the one being tested, was because it is unknown whether one feature will greatly alter the performance of another. It is assumed that a user would want all optimal features enabled, unless one needs to be disabled for reasons of instability. Such a case was discovered with LOOP, in which LOOP only seems to have a noticeable performance enhancing effect when BTB was enabled. LOOP enabled on its own did not improve performance.

The charts in Appendices 2 & 3 list the effects each feature had on the indicated benchmark program, while the charts in Appendices 4 & 5 normalise the results to that of the optimal/stable default settings (column *A*). This is done so that a relative change in performance can be established. Columns *B* thru *I* are the most common known stable features and column *A* contains results when all these features are enabled. Conversely, column *J* shows the results when *B* thru *I* are all disabled. Columns *K**, *L**, and *M** are feature configurations which contain a performance boost from the chosen *DEFAULT SETTINGS*, however they are not likely to be long-term stable in Windows. IORT (column *N*), which controls the I/O recovery time, is generally a setting controlled by the BIOS, however the longest possible recovery time of 128 clock cycles was set to determine if this setting had any affect on performance.

While not a Cyrix-specific next generation feature, benchmark results were also tabulated for cases where the CPU's L1 cache was placed into write-through mode, and with L1 cache entirely off (columns *O* and *P*, respectively). For these latter two features, it is important to remember that the *DEFAULT SETTINGS* of column *A* were still employed. For this to occur, for example as with setting the CPU into write-through mode, the CPU must still be set to write-back mode in the BIOS initially, then later changed to write-through mode in software, otherwise the next generation features (column *A*) did not have the same enhancing effects. That is to say, if you set your BIOS to L1 write-through mode, it was determined that later enabling the special features had less performance improvement than when setting L1 to write-through mode in software. To set the cache to write-through mode in software, it is first necessary to set LOCK NW = 0 then set CD = 0 and NW = 0.

Once all test results were normalised to *DEFAULT SETTINGS*, they were averaged for ALU- and FPU-specific tasks in terms of percent increases/decreases in performance. Some tests did not show any performance boost, however those too were equally averaged in. This method of performance characterisation has been termed *Average probable boost* as indicated on the bar graphs to follow. Since some tests showed a very large increase in performance while others showed little or no increase, the percent boost of the best test case is also included separately on the graphs and is termed *Maximum observable boost*. This difference is due to the fact that some CPU features enhance only specific instructions in the software code, while others do not. The performance boosts in the charts are ordered, or ranked, by their average probable boost. Both Windows and DOS results were grouped together; however Appendices 6 & 7 contain a DOS only section for those who are interested primarily in DOS performance.

Chart entries **bolded** in Appendices 2 & 3 indicate a change of greater than 2% from *DEFAULT SETTINGS*.

TEST SETTINGS

Test System

Biostar MB8433-UUD v3.0 Motherboard - UMC 8881F/8886BF, [BIOS: UUD960326S, 03/26/1996]
IBM 5x86C - 100HF at 133 MHz (Step 0, Rev 5), FSB = 66 MHz, CLKMUL = 2X, V_{core} = 3.85 V, 1:1/2 FSB:PCI
64 MB Fast-page mode RAM (60 ns) [BIOS: 1WS/0WS]
512 KB Single-banked L2 SRAM Cache (15 ns), Write-back [BIOS: 3-2-2]
PCI Slot 1 = Adaptec 2940U2W PCI SCSI Controller w/Seagate ST373307LW Ultra320 Harddrive
PCI Slot 2 = 3Com 3c905C-TX-M, 10/100Base-TX (disabled in Windows)
PCI Slot 3 = Matrox Millennium G200 PCI Graphics Card, 16 MB SDRAM
ISA Slot 4 = Creative Labs AWE64 Gold, 28 MB RAM (CT4390)

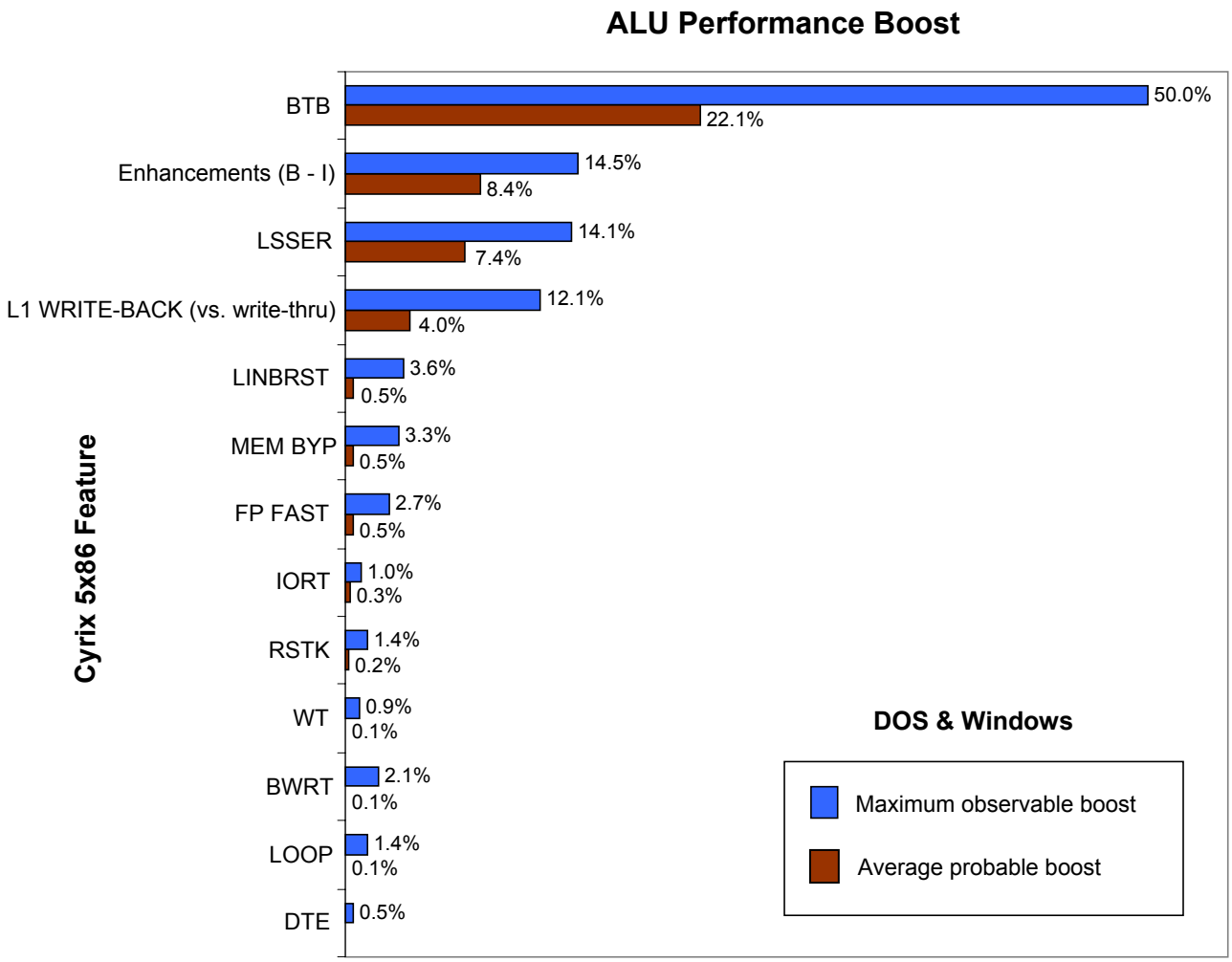
My Default Settings - Cyrix 5x86 Register Bits [PCR0=5h, CCR1=2h, CCR2=D6h, CCR3=1Ch, CCR4=38h, WBE (CD=0, NW=1)]

RSTK_EN = 1	Enables the return stack so that RET instructions will speculatively execute following a CALL. [1 is optimal]
BTB_EN = 0	Invokes the branch target buffer for instruction addresses, thereby inducing branch prediction. Not used. [1 is optimal]
LOOP_EN = 1	Enables the prefetch buffer loop for destination jumps still present in the prefetch buffer (prevents buffer flushing/reloading). [1 is optimal]
LSSER = 0	If set to 0, memory reads and writes to the load/store memory management unit can be reordered for optimum performance. [LSSER=0 is optimal]
WT1 = 1	Enables write-through in region 1 (640KB-1MB). Forces all writes to region 1 that hit the L1 cache to be sent to the external bus. [WT1=0 is optimal]
BWRT = 1	Enables the use of 16-byte burst write-back cycles. [1 is optimal]
LINBRST = 1	Enables a linear address sequence while performing burst cycles (as opposed to i486 "1+4" address sequencing). [1 is optimal]
FP_FAST = 1	Enables Fast FPU exception handling. [1 is optimal]
MEM_BYP = 1	Enables memory read bypassing so that data can be read from the write buffers prior to being written to external memory. [1 is optimal]
DTE_EN = 1	Enables the directory table entry cache. [1 is optimal]
IORT = 000	Specifies the minimum number of clock cycles between I/O accesses (I/O recovery time). [000 is optimal]
USE_WBAK = 1	Enables write-back L1 cache pins. [1 is optimal]
CD = 0, NW = 1	Enables write-back L1 cache. [01 is optimal]

CR0	***CCR1***	***CCR3***	***PCR0***	***PMR***
PG = 0	MMAC = 0	MAPEN[3-0] = 0001	LSSER = 0	HLF CLK = 0
CD = 0	SMAC = 0	SMM MODE = 1	LOOP EN = 1	CLK1 = 0
NW = 1	USE SMI = 1	LINBRST = 1	BTB EN = 0	CLK0 = 1
AM = 0		NMI EN = 0	RSTK EN = 1	
WP = 0	***CCR2***	SMI LOCK = 0		
NE = 0	USE SUSP = 1		***SMAR***	
1 = 1	BWRT = 1	***CCR4***	Address A31-A15 = 0000111000001010	
TS = 0	WT = 1	FP FAST = 1	A15-12 = 0000	
EM = 0	SUSP HLT = 0	DTE EN = 1	Size[3-0] = 0101	
MP = 0	LOCK NW = 1	MEM BYP = 1		
PE = 0	USE WBAK = 1	IORT[2-0] = 000		

For more information on how these features work and for what type of code they enhance, please refer to the *Cyrix 5x86 BIOS Writers Guide*, the *Cyrix 5x86 Microprocessor Guide*, the *Cyrix 6x86 BIOS Writers Guide*, the *Cyrix 6x86 Data Book*, the Peter Moss Utility's documentation, and register for an introductory course in computer architecture.

RESULTS - ALU



From the graph shown above, it is clear that BTB had the largest impact for ALU-focused processes, with a 22% boost. BTB, or branch prediction, on a Cyrix 5x86 is generally not considered a stable setting in Windows except possibly with Stepping 1, Revision 3 CPUs. To get BTB working on Stepping 1, Revision 3 CPUs, it is necessary to disable LOOP, and possibly RSTK, BWRT, and DTE. The CPU used in this study was Stepping 0, Revision 5. The noted Windows benchmark tests were run with LOOP, BWRT, and RSTK disabled, however to boot into Windows it was first necessary to boot into DOS, then type `win` at the command console to enter Windows. BTB appears stable in DOS with both revisions of the CPU. To date, no other CPU revisions have been encountered. The Cyrix 5x86-80 and 5x86-100 came in Stepping 1, Revision 3 editions, whereas Stepping 0, Revision 5 CPUs came in 100, 120, and 133 MHz flavours.

It was recently discovered that Windows NT4/98SE/2000 all initially appeared stable with a Stepping 0, Revision 5 CPU and all Cyrix features enabled (including BTB) except for LOOP, RSTK, BWRT, and DTE. Stability, however, had the tendency to decrease as the CPU was run longer (and began to heat up). This effect may be more of a consequence of running the CPU overclocked and above thermal spec for core voltage than with a broken feature. Some Cyrix features may be more frequency and/or thermal sensitive than others.

Referring to Appendix 6, we see that BTB did not have such a magnificent impact for DOS-only ALU tests; in DOS, performance boost dropped to only 5%. An interesting point to note from the DOS-only ALU chart is that

LOOP yielded a performance gain only when used in combination with BTB, thereby bumping the results up another 1%. Also surprising was that RSTK seemed to have no effect on its own accord. Unfortunately, LOOP and BTB together were not very stable. They may only work together in 16-bit mode since Windows would not boot with this setting and 3Dbench, Doom, Pcpbench, and Quake wouldn't run. It may be that BTB and LOOP work well together with Stepping 1, Revision 3 CPUs, however this configuration wasn't been tested.

Next in line for performance was LSSER at 7.4%. It was previously thought that LSSER needed to be disabled (set to 1) for motherboards which contained in-use PCI slots, however the author has had LSSER enabled (set to 0) for years with 3 filled PCI slots and hasn't had issues. From personal experience, the Biostar MB8433-UUD and PC Chips M919 both functioned with LSSER enabled.

Surprisingly, setting the L1 cache scheme to write-through mode instead of write-back only indicated a 4% improvement for ALU performance, though some tests showed as much as a 12% improvement. It should be noted that all other enhancements were still enabled. If write-back L1 cache is disabled in the BIOS instead of through software, it may not be possible to fully enable other Cyrix special features (although they may appear to be enabled).

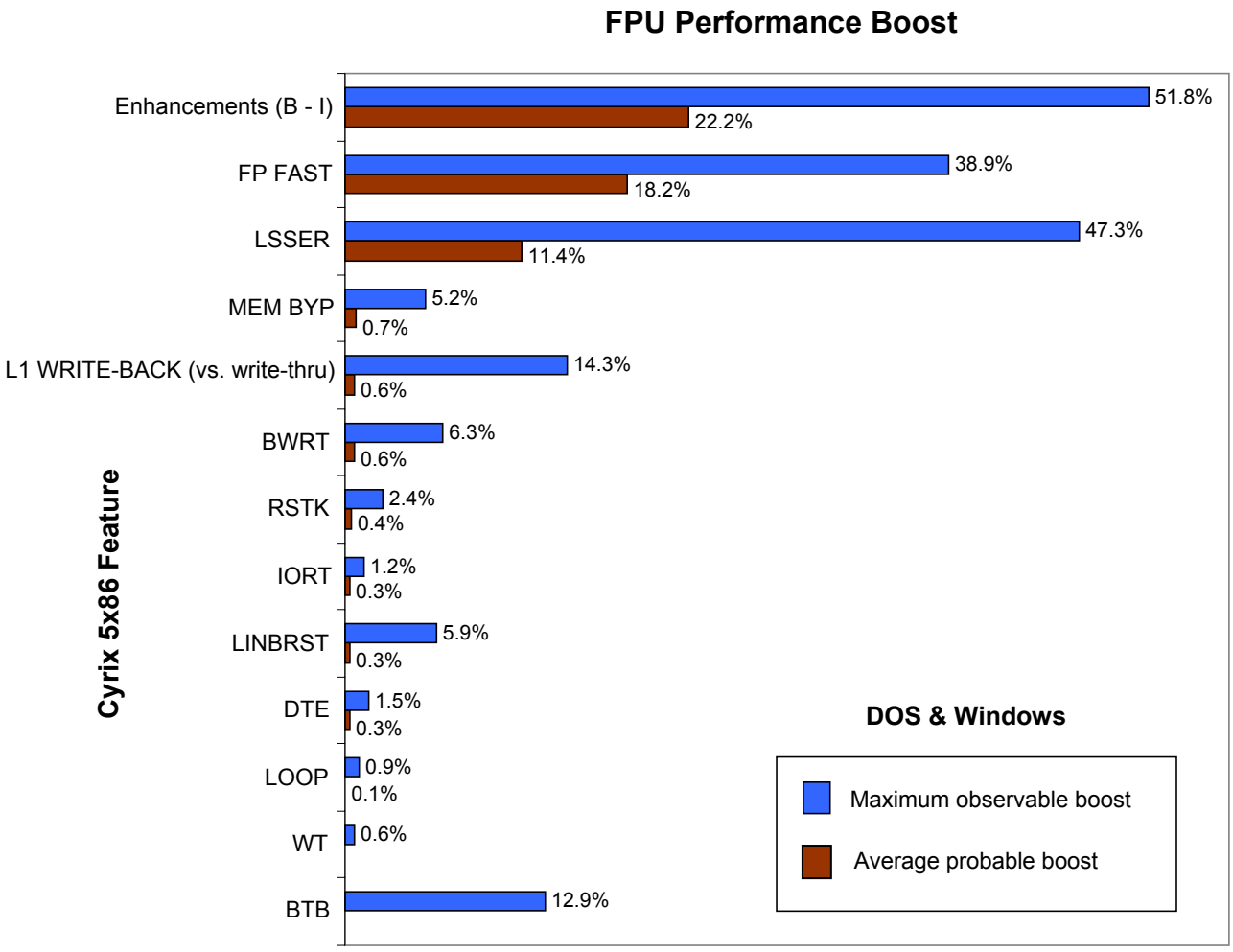
LINBRST, which is noted in the Cyrix literature as improving performance, only helped by an average of 0.5%. Your motherboard's chipset must support linear burst write cycles to enable this feature, otherwise your system will crash upon enabling it. While both the Biostar and M919 support LINBRST, there seemed to be no real performance boost, unless perhaps this feature cannot be disabled in software once the BIOS has enabled it. If this is the case, the only way to test for it would be to use a comparable motherboard which does not support this LINBRST, such as the Shuttle HOT-433. Only CPUMark32 in Windows caught the 4% improvement with LINBRST.

MEM BYP had the same ALU fate as LINBRST, with only a 0.5% improvement, however some tests weighed it in at 3.3%. FP FAST also didn't do much for ALU operations. Surprising is that IORT, which was set to 128 clock cycle delays, didn't seem to drop the performance much. It may be that the BIOS took over this setting without the possibility for intervention, however setting IORT to 128 clock cycles did drop the frame rate in DOOM by 5 fps.

WT, when enabled, sets only the memory region from 640 KB – 1000 KB into write-through mode (as opposed to write-back mode). When set to 0, you get write-back mode in this small region of memory, though doing so causes Quake not to run, and will yield an extra 2 fps in Doom. DTE and BWRT also had little to no effect on performance.

To summarise this section, if you can get BTB working, use it with a smile. LSSER is next in line for performance boost. Don't be too bummed if you cannot get the other features working, though if you can, adding up all the effects of the weak performers adds another 1% of boost on top of LSSER. If all stable/optimal enhancements are enabled, you should see a 13.5% ALU performance boost (*B* – *I*), though some applications may see up to a 50% boost. If you can get BTB working, you may see another 8.5% of ALU boost. From the *Ultimate 486 Benchmark Comparison*, the combined total boost of these Cyrix 5x86 register features weighs the ALU of a Cyrix 5x86-133 in at about the level of an AMD X5-160, or a Pentium 100 with pipeline burst cache enabled. Not too shabby for a low-cost, low-power 486.

RESULTS - FPU

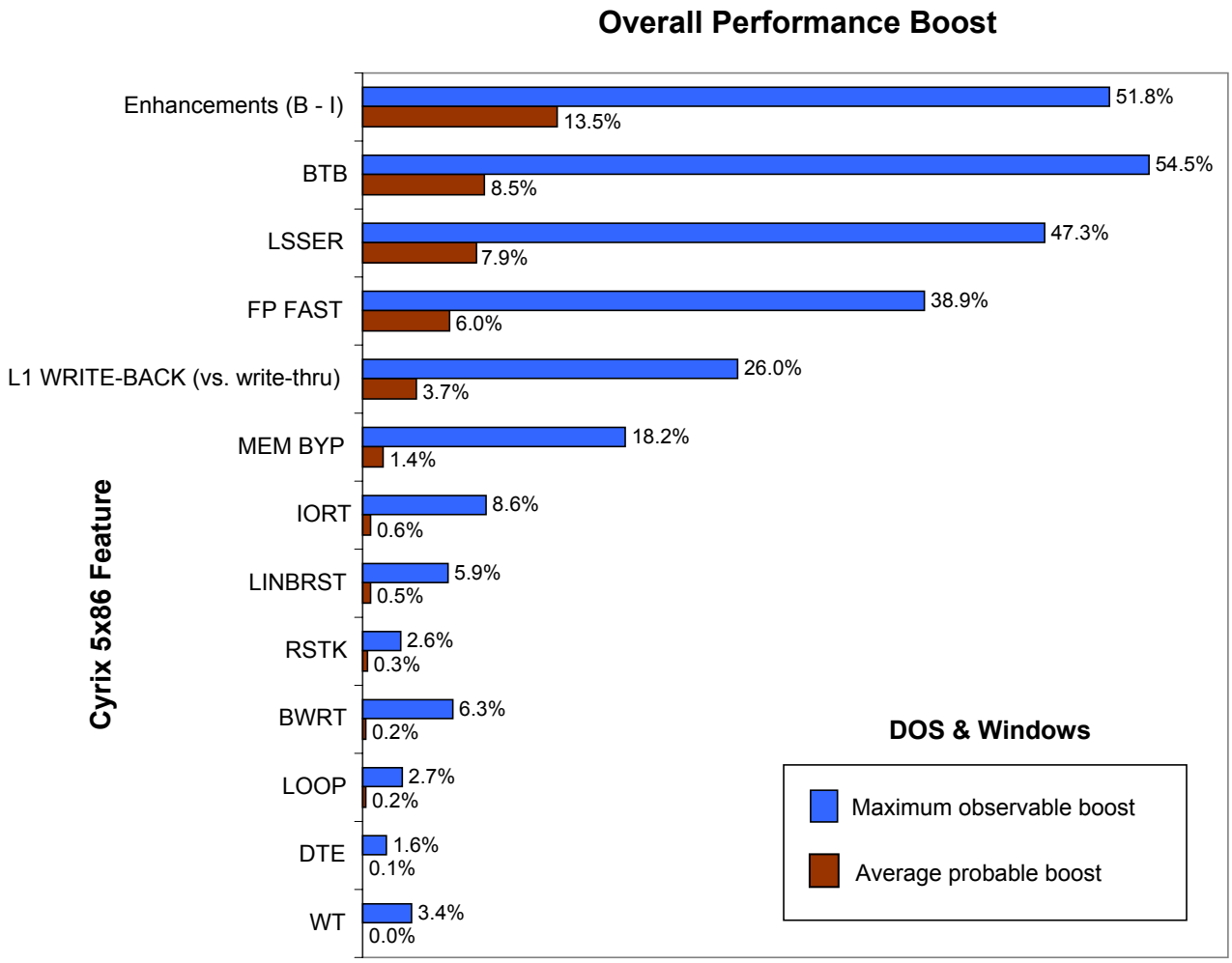


The floating-point units (FPU), or co-processors, of microprocessors are used extensively in high-performance games, simulation software, mp3 conversion, modeling, etc, so depending on your intended use of the processor, these results may be more (or less) important than the ALU results. Starting with BTB, we see that, on average, enabling this feature *decreased* ALU performance, but only in Windows. In DOS, it enhanced performance by about 2%. This performance drop wasn't an isolated case, since WinTune98, Sandra99, and PassMark all indicated a drop in performance.

The clear leader for FPU performance enhancement was FP FAST, which boosted the average FPU test results by 18%. Next in line was LSSER with 11.4%. MEM BYP helped by as much as 1%, while all other features had a relatively low average probable boost. It may be naive to entirely dismiss the other features since some tests indicated significant improvement. MEM BYP, BWRT, and LINBRST all had about a 5% improvement for the best case test. Even BTB, whose average is negative, improved performance by 13% in some tests.

The entire ensemble of stable/optimal features improved FPU performance by about 22%, and from the *Ultimate 486 Benchmark Comparison*, a Cyrix 5x86-133 rates in at about a Pentium 90. Even an AMD X5 overclocked to 200 MHz was about 4 Pentium ratings (PR points) below the Cyrix 5x86-133 in FPU-related tasks.

RESULTS - OVERALL



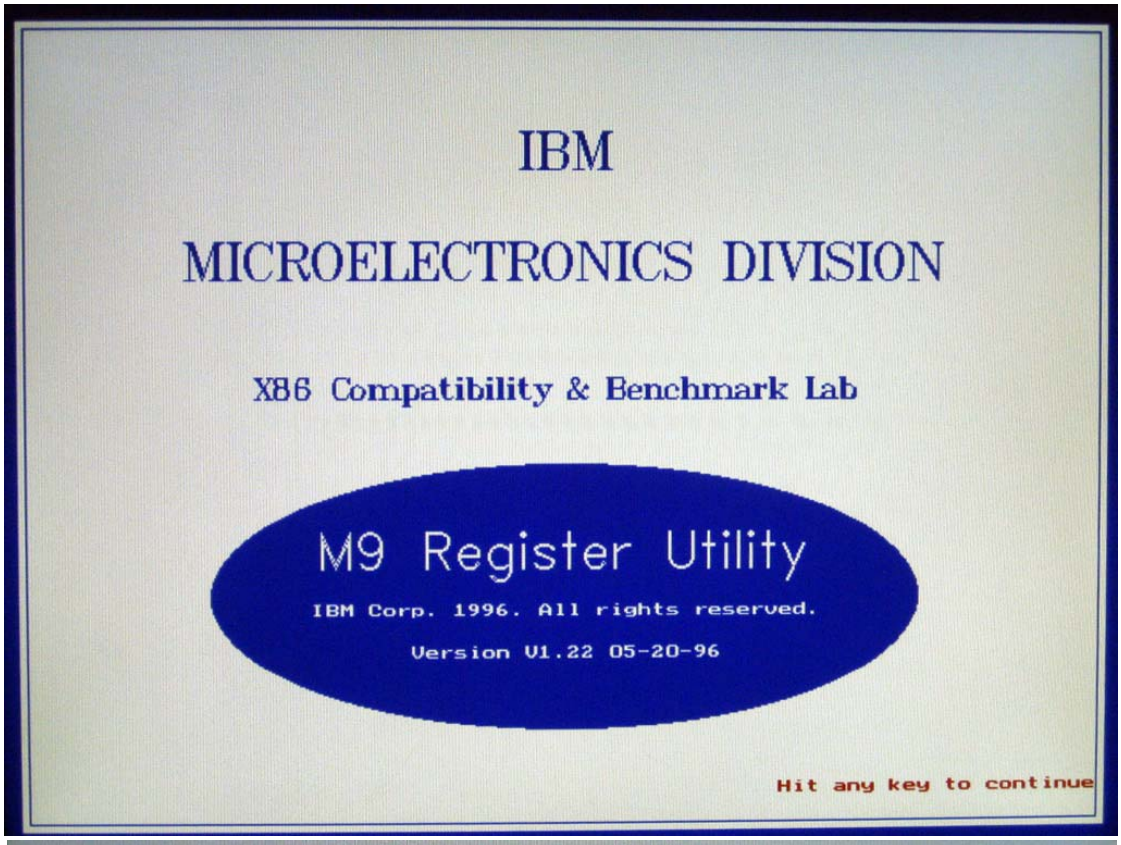
The overall performance graph encompasses a much larger number of tests than either the ALU- or FPU-specific graphs so the overall results are far more encompassing. The above graph can speak largely for itself. In line with the conclusions made in the ALU and FPU sections, BTB, LSSER, FP FAST, and perhaps MEM BYP are the most important of all the Cyrix 5x86's special features. The Symantec (Norton) Sysinfo benchmark program really seemed to think that MEM BYP hot stuff; it boosted the results of this test by 18%, however the average probable boost was a mere 1.4%

Considering that LSSER had a large impact on both ALU and FPU operations, it may be considered the most important Cyrix feature to enable. While BTB looks like a big contributor overall, it had less than half the performance of LSSER for DOS-only activities (not to mention its poor FPU performance). Rated second is a toss-up between BTB and FP FAST; it is hard to look past the whopping 18% improvement offered by FP FAST. In fourth place is MEM BYP, followed perhaps by LINBRST and BWRT.

The write-back caching scheme of the Cyrix 5x86 is charted mainly out of curiosity and is not a feature specific to Cyrix 5x86 processors. Both AMD and Intel employed write-back caching in their later 486 CPU revisions.

Looking now at the raw DOS gaming scores, LSSER and FP FAST showed the most improvement in Quake, gaining about 1.3 fps each, while BTB only improved Quake by 0.3 fps. With all stable Cyrix features (*B* – *I*) considered, we see about a 2.6 fps gain in Quake and about 2 fps gain in Doom. For 3Dbench, all stable Cyrix features (*B* – *I*) improved the score by 3%, whereas BTB alone improved the score by 4%.

Appendix 1 (Figures 1 – 6)



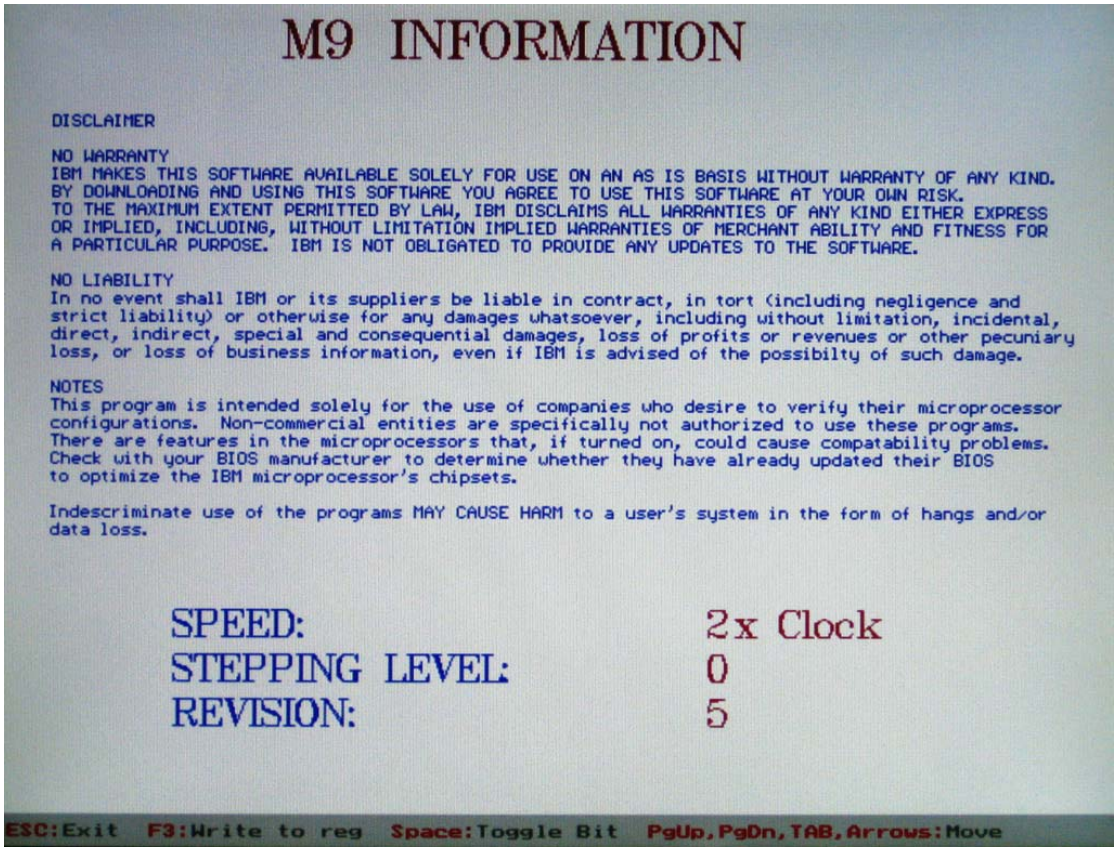
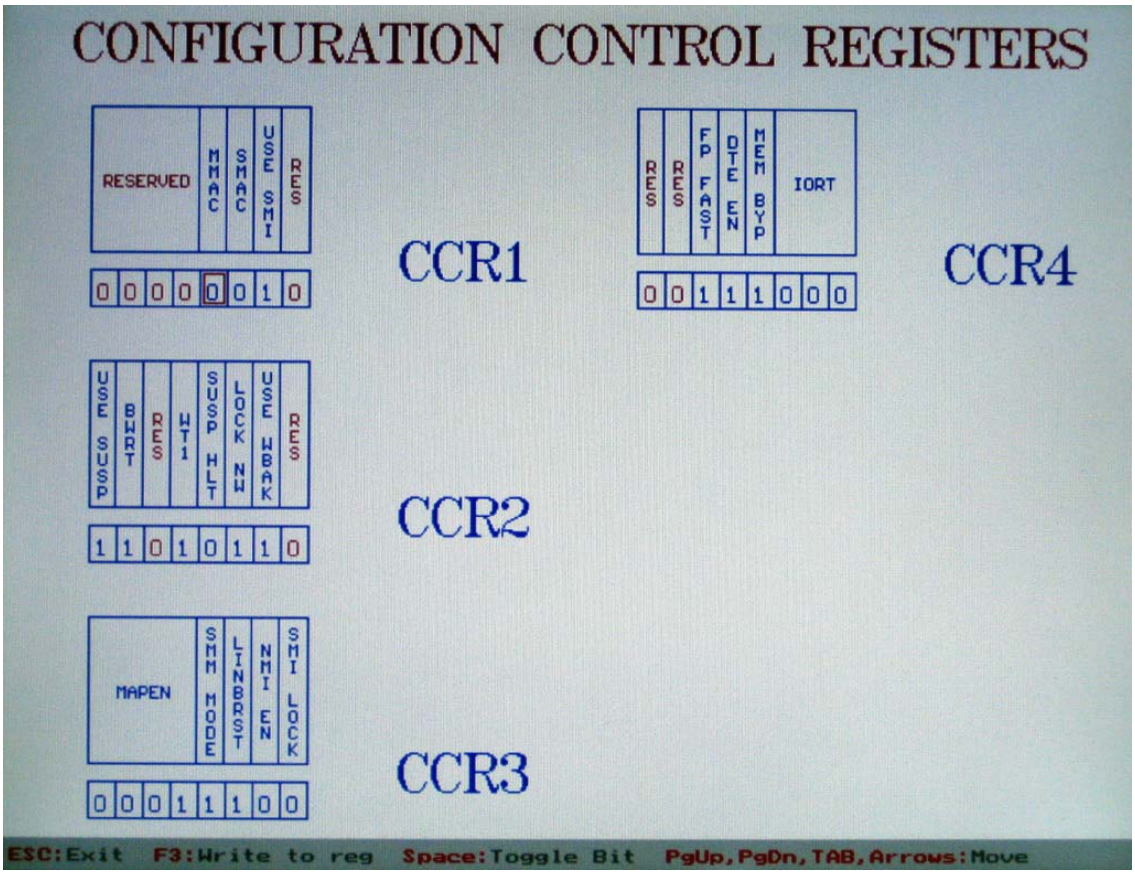


Figure 1/2: IBM utility used to enable/disable various Cyrix 5x86 features.




```
ET586 (c) 1995 by Evergreen Technologies, Inc. (11/28/95)
Version 1.1 (Release Version)

586 Configuration Register Dump

REGISTER   INDEX   BITS  7   6   5   4   3   2   1   0   =   Hex
--------   -----       --- --- --- --- --- --- --- ---     -----
 PCR0       20h         0   0   0   0   0   1   0   1       05h
 CCR1       C1h         0   0   0   0   0   0   1   0       02h
 CCR2       C2h         1   1   0   1   0   1   1   0       D6h
 CCR3       C3h         0   0   0   1   1   1   0   0       1Ch
 CCR4       E8h         0   0   1   1   1   0   0   0       38h
 SMAR0      CDh         0   0   0   0   1   1   1   0       0Eh
 SMAR1      CEh         0   0   0   0   1   0   1   0       0Ah
 SMAR2      CFh         0   0   0   0   0   1   0   1       05h
 PMR        F0h         0   0   0   0   0   0   0   1       01h
 DIR0       FEh         0   0   1   0   1   0   0   1       29h
 DIR1       FFh         0   0   0   0   0   1   0   1       05h

 MSW (CR0) = 20000010
 NW Bit    = 1
 CD Bit    = 0

Press any key to continue...
```

Figure 3/4: (3) One of several pages with adjustable settings from the IBM utility. (4) Evergreen ET586 utility.

```
A:\586>5x86 /e
Performance control register:
RSTK_EN: Return stack disabled
BTB_EN:  Branch target buffer disabled
Loop_EN: Prefetch buffer flush disabled
*        All itch buffer flush disabled
*        All instructions stalled to serialise, disabled
*        Locked misalighned load reordering disabled
*        Reserved bit 5 disabled
* BTBT:  BTB Test register disabled
LSSER:   Load store serialise is enabled.  Reorder disabled

Configuration control register 1:
USE_SMI: SMI and SMADS pins disabled

Configuration control register 2:
WRTBP:    Writeback pins enabled
Lock_NW:  NW bit locked
WT1:      Write through region one, enabled
BWRT:     Burst write disabled
SUSP:     Suspend pins enabled

Configuration control register 3:
SMI_LOCK: SMM bits unlocked
NMI_EN:   NMI disabled during SMM
LinBRST:  Linear address mode
SMM_Mode: SL compatable
Map_EN:   bit 0 disabled
Map_EN:   bit 1 disabled
Map_EN:   bit 2 disabled
Map_EN:   bit 3 disabled

Configuration control register 4:
MEM_BYP: Memory read bypassing, enabled
DTE_EN:  Directory table entry is cached
FP_FAST: NPU fast exception reporting disabled
IORT:    I/O recovery time = no clock delay

CR0 register:
NW: 0
CD: CPU cache is enabled
PG: Paging mode is enabled

Device identification register 0:
Cx5x86 3x clock

Device identification register 1:
Device stepping 0
Device revision 5

5x86.EXE                        Copyright (c) 1995 Peter N Moss
```

Figure 5: Results from the Peter N. Moss utility.

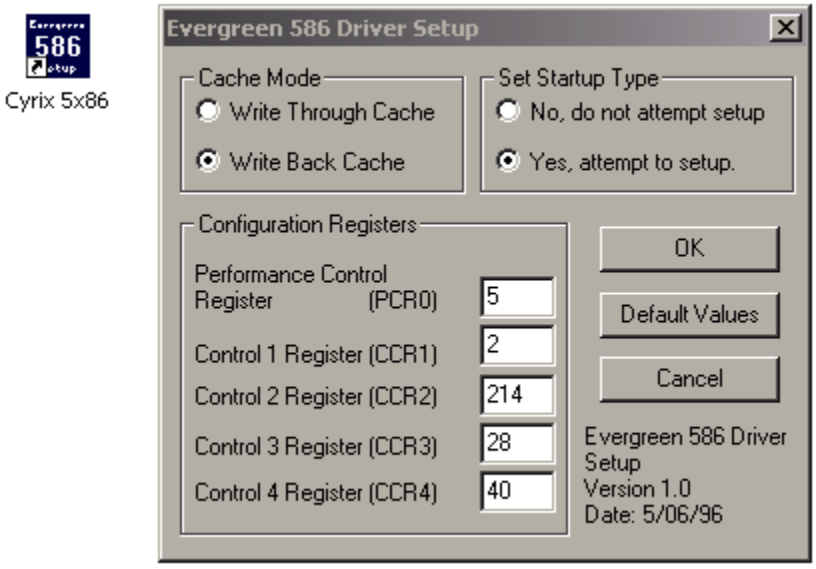


Figure 6: Evergreen Cyrix 5x86 driver for Windows NT/2000.

Cyrix 5x86 Feature Comparison (RAW)

DOS 7.10

	Deviation from default setting:	A DEFAULT SETTINGS (Optimal/Stable)	B LSSER = 1	C LOOP = 0	D RSTK = 0	E FP FAST = 0	F MEM BYP = 0	G DTE = 0	H LINBRST = 0	I BWRT = 0	J Enhancements (B - I) OFF [1]	K* BTB = 1 LOOP = 1	L* BTB = 1 LOOP = 0	M* WT = 0	N IORT = 111 (7h) 128-clock delay	O WBAK = 0 LOCK NW = 0 CD = 0 NW = 0 L1 Write-thru	P WBAK = 0 LOCK NW = 0 CD = 1 NW = 0 L1 Cache OFF
1	**Symantec Sysinfo v8.0** (arb. units)	352.1	352	352.1	352.1	352.1	**288.1**	352.1	352.1	352.1	**253.5**	**422.5**	**372.8**	352.1	352.1	**264.1**	**35.5**
2	**PC-Config v9.33** (% of Pentium 100)	113	**100**	**110**	113	113	**110**	113	113	113	**100**	113	113	113	113	**103**	**13**
3	**CpuIndex v2.3** (arb. units)	18	**17**	18	18	**17**	18	18	18	18	**16**	**19**	**19**	18	18	18	**3**
4	**PiDOS** [25k digits] (sec.)	16	**17**	16	16	16	16	16	**17**	16	**17**	**15**	**15**	16	16	16	**61**
	Landmark v2.0																
5	Integer ALU (Mhz)	567.6	564	567.6	567.6	567.6	567.6	567.6	567.6	567.6	564	**625.2**	**620.8**	567.6	567.6	567.6	**63.6**
6	Floating-point FPU (Mhz)	1712.1	**1614.4**	1712.1	1706.8	**1469**	1712.1	1712.1	1712.1	1712.1	**1438**	**1753**	**1750.2**	1712	1712.1	**1467**	**327.2**
	Chaikin Benchmark DOS v1.0																
8	Memory - ALU (arb. units)	11	**10.6**	11	11	**10.7**	11	11	11	11	**10.4**	11.1	11	11	11	10.85	**3.1**
9	Floating Point (arb. units)	16.2	16.1	16.2	16.2	**13.2**	16.2	16.2	16.2	16.2	**13.1**	16.4	16.3	16.2	16.2	16.2	**4.1**
	Roy Longbottom Dhrystone v1.1 [Integer, Optimised]																
22	DHRY1OD (VAX MIPS Rating)	136.94	**123.73**	136.94	138.19	136.94	137.15	137.15	136.94	136.94	**123.73**	**140.53**	**140.53**	137.15	137.15	**128.62**	**13.26**
	Roy Longbottom Linpack [Rolled Double Precision, Optimised]																
23	LINPCOD (MFLOPS)	7.27	7.23	7.29	7.28	**6.4**	7.29	7.27	7.27	**6.81**	**6**	7.27	7.29	7.28	7.29	8.28	**0.9**
	Roy Longbottom Whetstone [Single Precision, Optimised]																
24	WHETCOD, MWIPS (MFLOPS)	59.76	**53.43**	59.67	59.73	**52.83**	59.68	59.71	59.68	59.7	**50.35**	60.2	60.17	59.73	59.67	59.68	**21.34**
	Speedsys v4.78																
33	Score (arb. units)	73.41	**70.87**	73.41	73.41	**62.86**	72.88	73.41	73.41	73.41	**60.63**	**76.43**	**74.82**	73.41	73.41	**69.18**	**16.32**
35	System Memory Bandwidth (MB/s)	145.12	145.12	145.12	145.12	145.12	145.12	145.12	145.12	145.12	145.12	145.11	145.12	145.12	145.12	145.12	**81.26**
36	Ave. L1 Cache (MB/s)	189.41	**153.87**	189.41	189.41	189.42	189.41	189.41	189.41	189.41	**153.75**	**198.36**	190.08	189.41	189.41	**140.19**	**0**
37	Ave. L2 Cache (MB/s)	73.45	72.35	73.45	73.45	73.45	73.45	73.45	73.45	73.45	71	73.45	73.45	73.45	73.45	75.47	**0**
38	Ave. RAM Throughput (MB/s)	56.5	56.5	56.5	56.5	56.5	56.5	56.5	56.5	56.5	55.87	56.5	56.5	56.5	56.5	56.74	**48.3**
	Cachechk v4.0																
39	L1 Cache (MB/s)	272.7	272.7	272.7	272.7	272.7	272.7	272.7	272.7	272.7	272.7	**277.4**	274.3	272.7	272.7	272.7	**0**
40	L2 Cache (MB/s)	101.6	101.6	101.6	101.6	101.6	101.6	101.6	101.6	101.6	101.6	101.6	101.6	101.6	101.6	101.6	**0**
41	Memory (MB/s)	69.6	69.6	69.6	69.6	69.6	69.6	69.6	69.6	69.6	69.6	69.6	69.6	69.6	69.6	69.6	**39.8**
42	RAM Access Time (Read) (ns)	60	60	60	60	60	60	60	60	60	60	60	60	60	60	60	**105**
43	RAM Access Time (Write) (ns)	45	45	45	45	45	45	45	45	45	45	45	45	45	45	45	**45**
44	**3Dbench v1.0c** (arb. units)	91.7	**88.8**	91.7	91.8	91.7	91.7	91.7	92	91.7	**89.1**	x	**95.1**	91.7	91.6	90.6	**15.3**
45	**Doom v1.9s timedemo3** (fps)	56.0	**54.4**	55.9	56.1	56.0	56.0	55.9	55.6	55.9	**54.1**	x	**57.4**	**57.9**	**51.2**	55.0	**6.3**
46	**Pcpbench v1.04** (arb. units) [VESA Modus 100 (640x400 8bpp LFB)]	9.8	**9.6**	9.8	9.8	9.8	9.8	9.8	**9.6**	9.8	**9.5**	x	9.9	9.8	9.8	**9.6**	**1.7**
47	**Quake v1.06 timedemo1** (fps) [320x200, full screen, console off]	18.2	**16.9**	18.2	18.2	**16.8**	18.2	18.2	18	18.2	**15.5**	x	**18.5**	x	18.1	18.1	**2.5**

Test System

Biostar MB8433-UUD v3.0 Motherboard - UMC 8881F/8886BF, [BIOS: UUD960326S, 03/26/1996]
IBM 5x86C - 100HF at 133 MHz (Step 0, Rev 5), FSB = 66 MHz, CLKMUL = 2X, V_{core} = 3.85 V, 1:1/2 FSB:PCI
64 MB Fast-page mode RAM (60 ns) [BIOS: 1WS/0WS]
512 KB Single-banked L2 SRAM Cache (15 ns), Write-back [BIOS: 3-2-2]
PCI Slot 1 = Adaptec 2940U2W PCI SCSI Controller w/Seagate ST373307LW Ultra320 Harddrive
PCI Slot 2 = 3Com 3c905C-TX-M, 10/100Base-TX (disabled in Windows)
PCI Slot 3 = Matrox Millennium G200 PCI Graphics Card, 16 MB SDRAM
ISA Slot 4 = Creative Labs AWE64 Gold, 28MB (CT4390)

[1] Cyrix Enhancements set OFF [LSSER = 1 and RSTK, BTB, LOOP, FP_FAST, MEM_BYP, DTE, BWRT, LINBRST = 0]
* Configuration which indicates a performance boost from the chosen default setting.
x Test which did not complete

- Each feature (B-I & K-P) is tested independently of the other features. Tests are not additive.
- B-I are the feature disabled settings.
- Bolded value indicates a response greater than 2% from my default setting
- Values normalised to *Default Settings*

- BTB = 1, LOOP = 1, RSTK = 1 Unstable setting.
- BTB = 1, LOOP = 0, RSTK = 1 Stable setting in DOS. Step 1/Rev 3 stable in Windows.

- *Quake Timedemo*, enter new game, Ctrl~ to open console, type: timedemo demo1, then press Ctrl~ again
- *Doom Timedemo*, at DOS prompt type: doom -timedemo demo3
  Doom fps = gametics / realtics x 35, where gametics is typically 2134 for demo3 and realtics is measured

My Default Settings - Cyrix 5x86 Register Bits [PCR0=5, CCR1=2, CCR2=D6, CCR3=1C, CCR4=38, WBE (CD=0, NW=1)] (units are in hexadecimal)

RSTK_EN = 1	Enables the return stack so that RET instructions will speculatively execute following a CALL. [1 is optimal]
BTB_EN = 0	Invokes the branch target buffer for instruction addresses, thereby inducing branch prediction. Not used. [1 is optimal]
LOOP_EN = 1	Enables the prefetch buffer loop for destination jumps still present in the prefetch buffer (prevents buffer flushing/reloading). [1 is optimal]
LSSER = 0	If set to 0, memory reads and writes to the load/store memory management unit can be reordered for optimum performance. [LSSER=0 is optimal]
WT1 = 1	Enables write-through in region 1 (640KB-1MB). Forces all writes to region 1 that hit the L1 cache to be sent to the external bus. [WT1=0 is optimal]
BWRT = 1	Enables the use of 16-byte burst write-back cycles. [1 is optimal]
LINBRST = 1	Enables a linear address sequence while performing burst cycles (as opposed to i486 "1+4" address sequencing). [1 is optimal]
FP_FAST = 1	Enables Fast FPU exception handling. [1 is optimal]
MEM_BYP = 1	Enables memory read bypassing so that data can be read from the write buffers prior to being written to external memory. [1 is optimal]
DTE_EN = 1	Enables the directory table entry cache. [1 is optimal]
IORT = 000	Specifies the minimum number of clock cycles between I/O accesses (I/O recovery time). [000 is optimal]
USE_WBAK = 1	Enables write-back L1 cache pins. [1 is optimal]
CD = 0, NW = 1	Enables write-back L1 cache. [01 is optimal]

CR0	***CCR1***	***CCR3***	***PCR0***	***PMR***
PG = 0	MMAC = 0	MAPEN[3-0] = 000F	LSSER = 0	HLF CLK = 0
CD = 0	SMAC = 0	SMM MODE = 1	LOOP EN = 1	CLK1 = 0
NW = 1	USE SMI = 1	LINBRST = 1	BTB EN = 0	CLK0 = 1
AM = 0		NMI EN = 0	RSTK EN = 1	
WP = 0	***CCR2***	SMI LOCK = 0		
NE = 0	USE SUSP = 1		***SMAR***	
1 = 1	BWRT = 1	***CCR4***	Address A31-A15 = 0000111000001010	
TS = 0	WT = 1	FP FAST = 1	A15-12 = 0000	
EM = 0	SUSP HLT = 0	DTE EN = 1	Size[3-0] = 0101	
MP = 0	LOCK NW = 1	MEM BYP = 1		
PE = 0	USE WBAK = 1	IORT[2-0] = 000		

Cyrix 5x86 Feature Comparison (RAW)

Windows 98SE

		A	B	C	D	E	F	G	H	I	J	K*	L*	M*	N	O	P
	Deviation from default setting:	**DEFAULT SETTINGS** (Optimal/Stable)	**LSSER = 1**	**LOOP = 0**	**RSTK = 0**	**FP FAST = 0**	**MEM BYP = 0**	**DTE = 0**	**LINBRST = 0**	**BWRT = 0**	**Enhancements (B - I) OFF** [1]	**BTB = 1 LOOP = 1**	**BTB = 1 LOOP = 0**	**WT = 0**	**IORT = 111 (7h) 128-clock delay**	**WBAK = 0 LOCK NW = 0 CD = 0 NW = 0 L1 Write-thru**	**WBAK = 0 LOCK NW = 0 CD = 1 NW = 0 L1 Cache OFF**
48	**SuperPi v1.1** [32k digits] (sec.)	33.2	33.7	33.2	**34**	**37.2**	33.4	33.7	33.7	32.9	**37.8**	x	**31.7**	33	33.1	32.4	x
	Ziff-Davis Winbench96																
55	CPUMark32 v1.0 (arb. units)	192	**188**	192	193	192	192	191	**185**	**188**	**184**	x	**217**	191	191	**187**	x
56	Graphics WinMark v1.0 (arb. units)	22.7	**21.6**	22.7	**22.1**	22.9	23.1	22.9	22.4	22.8	**20.8**	x	**27**	22.4	22.6	**20.5**	x
	Ziff-Davis Winbench99																
57	CPUMark99 Stand-alone v1.0 (a.u.)	6.26	**5.94**	6.32	6.23	6.22	**6.16**	6.23	6.17	6.26	**5.97**	x	**7.65**	6.27	6.2	**6.12**	x
58	FPU WinMark99 v1.1 (arb. units)	249	**239**	249	249	**195**	249	249	249	250	**190**	x	**281**	249	249	**242**	x
	WinTune98 (3x)																
59	Integer (MIPS)	201.5	**175.2**	201.1	198.7	201.9	201.9	202	202.4	201.8	**172.2**	x	**296**	201	202	**177.1**	x
60	Floating Point (MFLOPS)	95.7	95.5	95.7	95.7	**88.3**	95.5	95.6	95.6	95.7	**89**	x	**83**	94.7	95.5	94.6	x
61	Video 2D (Mpixels/s)	22.1	**21.1**	22	21.8	22	23.1	21.8	21.8	22	**20.7**	x	**21.5**	22	22	22.8	x
62	Direct3D (Mpixels/s)	33.5	33.2	33.5	33.6	33.5	33.5	33.6	33.5	33.5	33	x	33	33.6	33.5	33.2	x
63	OpenGL (Mpixels/s)	2.54	**2.35**	2.52	2.53	2.53	**2.5**	2.52	2.54	2.54	**2.32**	x	**2.38**	2.53	2.52	**2.35**	x
64	Memory (MB/s)	80.6	79.4	80.3	80.6	81.1	79.7	79.3	79.5	80.7	80.5	x	98.9	80.9	79.6	80.2	x
	Sandra99																
65	CPU: ALU Dhrystone (MIPS)	218	**199**	215	216	216	218	223	218	222	**196**	x	327	220	216	**194**	x
66	CPU: FPU Whetstone (MFLOPS)	94	**90**	94	93	**88**	93	93	93	93	**85**	x	88	94	93	93	x
67	Multi-Media: ALU Integer (it/s)	71	**61**	71	71	71	71	71	71	71	**61**	x	87	71	71	71	x
68	Multi-Media: FPU Floating Point (it/s)	54	**46**	54	54	**33**	54	54	54	54	**37**	x	55	54	54	54	x
69	Memory: ALU Bandwidth (MB/s)	41	39	41	41	41	41	41	40	41	38	x	**47**	41	41	41	x
70	Memory: FPU Bandwidth (MB/s)	54	54	54	54	52	54	54	54	54	52	x	**49**	54	53	54	x
	PassMark v4.0																
71	2D Graphics Mark (arb. units)	54	53.5	54	53.9	53.8	54	54	53.9	54	53.7	x	52.3	53.9	53.9	53.7	x
72	Memory Mark (arb. units)	8.8	**8.6**	8.8	8.7	8.7	**7.6**	8.7	8.7	8.8	**7.5**	x	**13.6**	8.8	8.7	**8.6**	x
73	Math Mark (arb. units)	7.2	**5.2**	7.2	7.2	**6**	**6.9**	7.2	7.2	7.2	**4.9**	x	**7.8**	7.2	7.1	7.1	x
74	Math Max MFLOPS	11	**5.8**	10.9	10.9	**7.3**	10.9	10.9	11	11	**5.3**	x	**7.9**	10.9	10.9	**10.7**	x
75	Integer Addition (arb. units)	10.9	**9.8**	10.9	10.9	10.9	**10.5**	10.9	10.9	10.9	**9.4**	x	**17.3**	10.9	10.8	10.8	x
76	Integer Subtraction (arb. units)	10.9	**9.8**	10.9	10.9	10.9	**10.5**	10.9	10.9	10.9	**9.4**	x	**17.3**	10.9	10.8	10.8	x
77	Integer Multiplication (arb. units)	5.9	**5.1**	5.9	5.9	5.9	**5.8**	5.9	5.9	**5.8**	**5**	x	**4**	5.9	**5.8**	**5.8**	x
78	Integer Division (arb. units)	2.5	**2.4**	2.5	2.5	2.5	**2.4**	2.5	2.5	2.5	**2.3**	x	**3.6**	2.5	2.5	2.5	x
79	FPU Addition (arb. units)	9.1	**5.3**	9	9	**6.2**	**8.7**	9.1	9.1	9.1	**4.6**	x	**7.7**	9.1	8.9	**8.9**	x
80	FPU Subtraction (arb. units)	7.8	**4.8**	7.8	7.8	**5.7**	**7.4**	7.8	7.8	7.8	**4.4**	x	**7.7**	7.8	7.7	7.7	x
81	FPU Multiplication (arb. units)	8.3	**5.0**	8.3	8.3	**6.0**	**7.9**	8.3	8.3	8.3	**4.6**	x	**7.1**	8.3	8.2	8.2	x
82	FPU Division (arb. units)	3.1	**2.4**	3.1	3.1	**2.7**	**2.9**	3.1	3.1	3.1	**2.4**	x	**2.5**	3.1	3.1	3.1	x

Cyrix 5x86 Feature Comparison (NORMALISED)

DOS 7.10

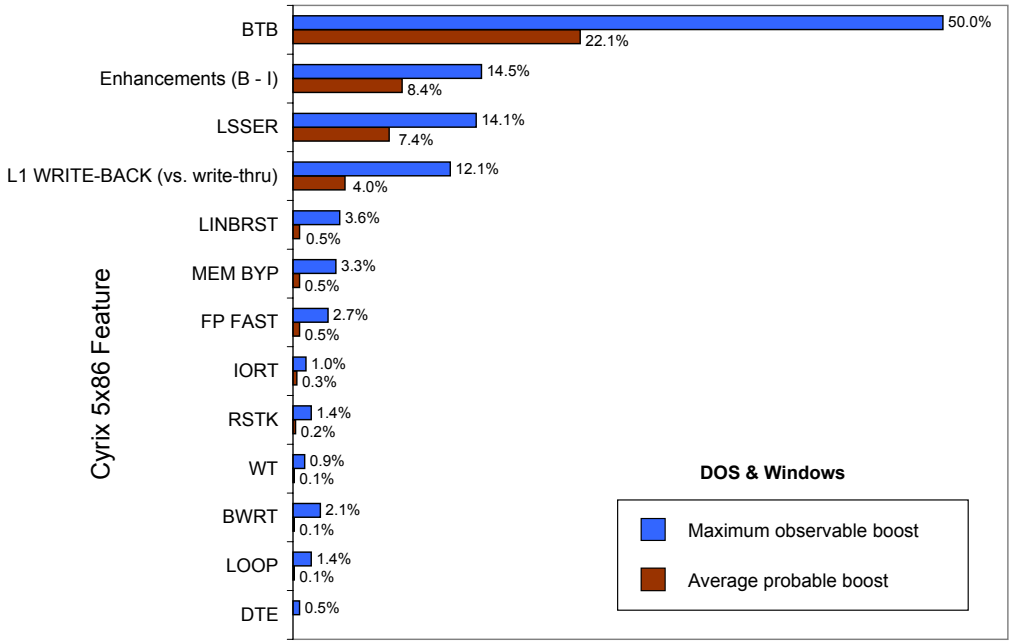
		A	B	C	D	E	F	G	H	I	J	K*	L*	M*	N	O	P
	Deviation from default setting:	**DEFAULT SETTINGS** (Optimal/Stable)	**LSSER = 1**	**LOOP = 0**	**RSTK = 0**	**FP FAST = 0**	**MEM BYP = 0**	**DTE = 0**	**LINBRST = 0**	**BWRT = 0**	**Enhancements (B - I) OFF [1]**	**BTB = 1 LOOP = 1**	**BTB = 1 LOOP = 0**	**WT = 0**	**IORT = 111 (7h) 128-clock delay**	**WBAK = 0 LOCK NW = 0 CD = 0 NW = 0 L1 Write-thru**	**WBAK = 0 LOCK NW = 0 CD = 1 NW = 0 L1 Cache OFF**
1	**Symantec Sysinfo v8.0** (arb. units)	1.00	1.00	1.00	1.00	1.00	**0.82**	1.00	1.00	1.00	**0.72**	**1.20**	**1.06**	1.00	1.00	**0.75**	**0.10**
2	**PC-Config v9.33** (% of Pentium 100)	1.00	**0.88**	**0.97**	1.00	1.00	**0.97**	1.00	1.00	1.00	**0.88**	1.00	1.00	1.00	1.00	**0.91**	**0.12**
3	**CpuIndex v2.3** (arb. units)	1.00	**0.94**	1.00	1.00	**0.94**	1.00	1.00	1.00	1.00	**0.89**	**1.06**	**1.06**	1.00	1.00	1.00	**0.17**
4	**PiDOS** [25k digits] (1/sec.)	1.00	**0.94**	1.00	1.00	1.00	1.00	1.00	**0.94**	1.00	**0.94**	**1.07**	**1.07**	1.00	1.00	1.00	**0.26**
	Landmark v2.0																
5	Integer ALU (Mhz)	1.00	0.99	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.99	**1.10**	**1.09**	1.00	1.00	1.00	**0.11**
6	Floating-point FPU (Mhz)	1.00	**0.94**	1.00	1.00	**0.86**	1.00	1.00	1.00	1.00	**0.84**	**1.02**	**1.02**	1.00	1.00	**0.86**	**0.19**
	Chaikin Benchmark DOS v1.0																
8	Memory - ALU (arb. units)	1.00	**0.96**	1.00	1.00	**0.97**	1.00	1.00	1.00	1.00	**0.95**	1.01	1.00	1.00	1.00	0.99	**0.28**
9	Floating Point (arb. units)	1.00	0.99	1.00	1.00	**0.81**	1.00	1.00	1.00	1.00	**0.81**	1.01	1.01	1.00	1.00	1.00	**0.25**
	Roy Longbottom Dhrystone v1.1																
	[Integer, Optimised]																
22	DHRY1OD (VAX MIPS Rating)	1.00	**0.90**	1.00	1.01	1.00	1.00	1.00	1.00	1.00	**0.90**	**1.03**	**1.03**	1.00	1.00	**0.94**	**0.10**
	Roy Longbottom Linpack																
	[Rolled Double Precision, Optimised]																
23	LINPCOD (MFLOPS)	1.00	0.99	1.00	1.00	**0.88**	1.00	1.00	1.00	**0.94**	**0.83**	1.00	1.00	1.00	1.00	1.14	**0.12**
	Roy Longbottom Whetstone																
	[Single Precision, Optimised]																
24	WHETCOD, MWIPS (MFLOPS)	1.00	**0.89**	1.00	1.00	**0.88**	1.00	1.00	1.00	1.00	**0.84**	1.01	1.01	1.00	1.00	1.00	**0.36**
	Speedsys v4.78																
33	Score (arb. units)	1.00	**0.97**	1.00	1.00	**0.86**	0.99	1.00	1.00	1.00	**0.83**	**1.04**	**1.02**	1.00	1.00	**0.94**	**0.22**
35	System Memory Bandwidth (MB/s)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	**0.56**
36	Ave. L1 Cache (MB/s)	1.00	**0.81**	1.00	1.00	1.00	1.00	1.00	1.00	1.00	**0.81**	**1.05**	1.00	1.00	1.00	**0.74**	**0.00**
37	Ave. L2 Cache (MB/s)	1.00	0.99	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.97	1.00	1.00	1.00	1.00	1.03	**0.00**
38	Ave. RAM Throughput (MB/s)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.99	1.00	1.00	1.00	1.00	1.00	**0.85**
	Cachechk v4.0																
39	L1 Cache (MB/s)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	**1.02**	1.01	1.00	1.00	1.00	**0.00**
40	L2 Cache (MB/s)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	**0.00**
41	Memory (MB/s)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	**0.57**
42	RAM Access Time (Read) (ns)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	**1.75**
43	RAM Access Time (Write) (ns)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	**1.00**
44	**3Dbench v1.0c** (arb. units)	1.00	**0.97**	1.00	1.00	1.00	1.00	1.00	1.00	1.00	**0.97**	x	**1.04**	1.00	1.00	0.99	**0.17**
45	**Doom v1.9s timedemo3** (fps)	1.00	**0.97**	1.00	1.00	1.00	1.00	1.00	0.99	1.00	**0.97**	x	**1.02**	**1.03**	**0.91**	**0.98**	**0.11**
46	**Pcpbench v1.04** (arb. units)	1.00	**0.98**	1.00	1.00	1.00	1.00	1.00	**0.98**	1.00	**0.97**	x	1.01	1.00	1.00	**0.98**	**0.17**
	[VESA Modus 100 (640x400 8bpp LFB)]											x					
47	**Quake v1.06 timedemo1** (fps)	1.00	**0.93**	1.00	1.00	**0.92**	1.00	1.00	0.99	1.00	**0.85**	x	**1.02**	x	0.99	0.99	**0.14**
	[320x200, full screen, console off]																
86	**ALU** (% boost of best case)	-	**10**	0	0	**3**	0	0	0	0	**10**	**10**	**9**	0	0	**6**	**90**
87	**ALU** (% of cases > 2% sensitivity)	-	67	0	0	33	0	0	0	0	67	67	67	0	0	33	100
88	**ALU** (% ave. probable boost)	-	**5.0**	0	0	**0.0**	0	0	0	0	**5.3**	**4.7**	**0.0**	0	0	**2.3**	**83.7**
	Tests: 5, 8, 22																
89	**FPU** (% boost of best case)	-	**11**	0	0	**19**	0	0	**6**	**6**	**19**	**7**	**7**	0	0	**14**	**81**
90	**FPU** (% of cases > 2% sensitivity)	-	40	0	0	80	0	0	20	20	100	40	40	0	0	20	100
91	**FPU** (% ave. probable boost)	-	**5.0**	0	0	**11.4**	0	0	**1.2**	**1.2**	**14.8**	**2.2**	**2.2**	0	0	**2.8**	**76.4**
	Tests: 4, 6, 9, 23, 24																
92	**Overall** (% boost of best case)	-	**19**	**3**	0	**19**	**18**	0	**6**	**6**	**28**	**20**	**9**	**3**	**9**	**26**	**90**
93	**Overall** (% of cases > 2% sensitivity)	-	72	6	0	44	11	0	11	6	89	44	50	6	6	39	100
94	**Overall** (% ave. probable boost)	-	**5.3**	**0.2**	0	**4.9**	**1.2**	0	**0.6**	**0.3**	**11.2**	**3.9**	**2.5**	**0.2**	**0.5**	**5.2**	**84.1**
	Tests: 1, 2, 3, 4, 5, 6, 7, 8, 9, 22, 23, 24, 33, 36, 39, 44, 45, 46, 47																

Cyrix 5x86 Feature Comparison (NORMALISED)

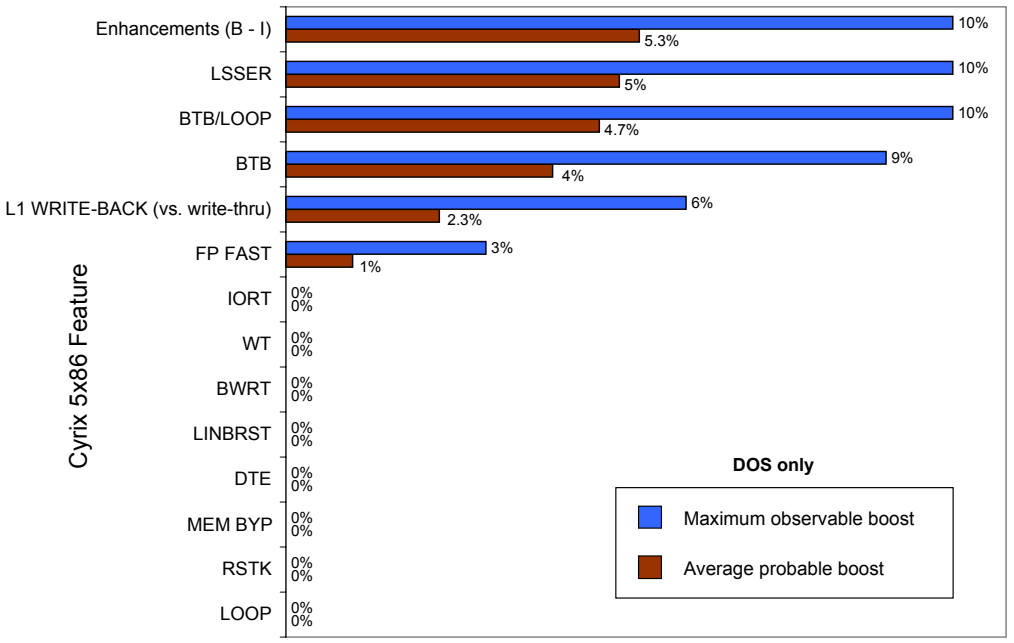
Windows 98SE

		A	B	C	D	E	F	G	H	I	J	K*	L*	M*	N	O	P
	Deviation from default setting:	**DEFAULT SETTINGS** (Optimal/Stable)	**LSSER = 1**	**LOOP = 0**	**RSTK = 0**	**FP FAST = 0**	**MEM BYP = 0**	**DTE = 0**	**LINBRST = 0**	**BWRT = 0**	**Enhancements (B - I) OFF [1]**	**BTB = 1 LOOP = 1**	**BTB = 1 LOOP = 0**	**WT = 0**	**IORT = 111 (7h) 128-clock delay**	**WBAK = 0 LOCK NW = 0 CD = 0 NW = 0 L1 Write-thru**	**WBAK = 0 LOCK NW = 0 CD = 1 NW = 0 L1 Cache OFF**
48	**SuperPi v1.1** [32k digits] (1/sec.)	1.00	0.99	1.00	**0.98**	**0.89**	0.99	0.99	0.99	1.01	**0.88**	x	**1.05**	1.01	1.00	1.02	x
	Ziff-Davis Winbench96	1.00															
55	CPUMark32 v1.0 (arb. units)	1.00	**0.98**	1.00	1.01	1.00	1.00	0.99	**0.96**	**0.98**	**0.96**	x	**1.13**	0.99	0.99	**0.97**	x
56	Graphics WinMark v1.0 (arb. units)	1.00	**0.95**	1.00	**0.97**	1.01	1.02	1.01	0.99	1.00	**0.92**	x	**1.19**	0.99	1.00	**0.90**	x
	Ziff-Davis Winbench99																
57	CPUMark99 Stand-alone v1.0 (a.u.)	1.00	**0.95**	1.01	1.00	0.99	**0.98**	1.00	0.99	1.00	**0.95**	x	**1.22**	1.00	0.99	**0.98**	x
58	FPU WinMark99 v1.1 (arb. units)	1.00	**0.96**	1.00	1.00	**0.78**	1.00	1.00	1.00	1.00	**0.76**	x	**1.13**	1.00	1.00	**0.97**	x
	WinTune98 (3x)																
59	Integer (MIPS)	1.00	**0.87**	1.00	0.99	1.00	1.00	1.00	1.00	1.00	**0.85**	x	**1.47**	1.00	1.00	**0.88**	x
60	Floating Point (MFLOPS)	1.00	1.00	1.00	1.00	**0.92**	1.00	1.00	1.00	1.00	**0.93**	x	**0.87**	0.99	1.00	0.99	x
61	Video 2D (Mpixels/s)	1.00	**0.95**	1.00	0.99	1.00	1.05	0.99	0.99	1.00	**0.94**	x	**0.97**	1.00	1.00	1.03	x
62	Direct3D (Mpixels/s)	1.00	0.99	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.99	x	0.99	1.00	1.00	0.99	x
63	OpenGL (Mpixels/s)	1.00	**0.93**	0.99	1.00	1.00	**0.98**	0.99	1.00	1.00	**0.91**	x	**0.94**	1.00	0.99	**0.93**	x
64	Memory (MB/s)	1.00	0.99	1.00	1.00	1.01	0.99	0.98	0.99	1.00	1.00	x	1.23	1.00	0.99	1.00	x
	Sandra99																
65	CPU: ALU Dhrystone (MIPS)	1.00	**0.91**	0.99	0.99	0.99	1.00	1.02	1.00	1.02	**0.90**	x	**1.50**	1.01	0.99	**0.89**	x
66	CPU: FPU Whetstone (MFLOPS)	1.00	**0.96**	1.00	0.99	**0.94**	0.99	0.99	0.99	0.99	**0.90**	x	**0.94**	1.00	0.99	0.99	x
67	Multi-Media: ALU Integer (it/s)	1.00	**0.86**	1.00	1.00	1.00	1.00	1.00	1.00	1.00	**0.86**	x	**1.23**	1.00	1.00	1.00	x
68	Multi-Media: FPU Floating Point (it/s)	1.00	**0.85**	1.00	1.00	**0.61**	1.00	1.00	1.00	1.00	**0.69**	x	**1.02**	1.00	1.00	1.00	x
69	Memory: ALU Bandwidth (MB/s)	1.00	0.95	1.00	1.00	1.00	1.00	1.00	0.98	1.00	0.93	x	1.15	1.00	1.00	1.00	x
70	Memory: FPU Bandwidth (MB/s)	1.00	1.00	1.00	1.00	0.96	1.00	1.00	1.00	1.00	0.96	x	0.91	1.00	0.98	1.00	x
	PassMark v4.0																
71	2D Graphics Mark (arb. units)	1.00	0.99	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.99	x	0.97	1.00	1.00	0.99	x
72	Memory Mark (arb. units)	1.00	**0.98**	1.00	0.99	0.99	**0.86**	0.99	0.99	1.00	**0.85**	x	**1.55**	1.00	0.99	**0.98**	x
73	Math Mark (arb. units)	1.00	**0.72**	1.00	1.00	**0.83**	**0.96**	1.00	1.00	1.00	**0.68**	x	**1.08**	1.00	0.99	0.99	x
74	Math Max MFLOPS	1.00	**0.53**	0.99	0.99	**0.66**	0.99	0.99	1.00	1.00	**0.48**	x	**0.72**	0.99	0.99	**0.97**	x
75	Integer Addition (arb. units)	1.00	**0.90**	1.00	1.00	1.00	**0.96**	1.00	1.00	1.00	**0.86**	x	**1.59**	1.00	0.99	0.99	x
76	Integer Subtraction (arb. units)	1.00	**0.90**	1.00	1.00	1.00	**0.96**	1.00	1.00	1.00	**0.86**	x	**1.59**	1.00	0.99	0.99	x
77	Integer Multiplication (arb. units)	1.00	**0.86**	1.00	1.00	1.00	**0.98**	1.00	1.00	**0.98**	**0.85**	x	**0.68**	1.00	**0.98**	**0.98**	x
78	Integer Division (arb. units)	1.00	**0.96**	1.00	1.00	1.00	**0.96**	1.00	1.00	1.00	**0.92**	x	**1.44**	1.00	1.00	1.00	x
79	FPU Addition (arb. units)	1.00	**0.58**	0.99	0.99	**0.68**	**0.96**	1.00	1.00	1.00	**0.51**	x	**0.85**	1.00	**0.98**	**0.98**	x
80	FPU Subtraction (arb. units)	1.00	**0.62**	1.00	1.00	**0.73**	**0.95**	1.00	1.00	1.00	**0.56**	x	**0.99**	1.00	0.99	0.99	x
81	FPU Multiplication (arb. units)	1.00	**0.60**	1.00	1.00	**0.72**	**0.95**	1.00	1.00	1.00	**0.55**	x	**0.86**	1.00	0.99	0.99	x
82	FPU Division (arb. units)	1.00	**0.77**	1.00	1.00	**0.87**	**0.94**	1.00	1.00	1.00	**0.77**	x	**0.81**	1.00	1.00	1.00	x
95	**ALU** (% boost of best case)	-	14.1	1.4	1.4	2.7	3.3	0.5	3.6	2.1	14.5	10.0	50.0	0.9	1.0	12.1	90.0
96	**ALU** (% of cases > 2% sensitivity)	-	89	0	0	11	22	0	11	14	89	67	89	89	0	58	100
97	**ALU** (% ave. probable boost)	-	**7.4**	**0.1**	**0.2**	**0.5**	**0.5**	**-0.2**	**0.5**	**0.1**	**8.4**	**4.7**	**22.1**	**0.1**	**0.3**	**4.0**	**83.7**
	Tests: 5, 8, 22, 55, 57, 59, 65, 67, (75-78)																
98	**FPU** (% boost of best case)	-	47.3	0.9	2.4	38.9	5.2	1.5	5.9	6.3	51.8	7.0	12.9	0.6	1.2	14.3	81.0
99	**FPU** (% of cases > 2% sensitivity)	-	75	0	8	92	8	0	8	8	100	40	75	75	0	27	100
100	**FPU** (% ave. probable boost)	-	**11.4**	**0.1**	**0.4**	**18.2**	**0.7**	**0.3**	**0.3**	**0.6**	**22.2**	**2.2**	**-3.4**	**-0.1**	**0.3**	**0.6**	**76.4**
	Tests: 4, 6, 9, 23, 24, 48, 58, 60, 66, 68, 74, (79-82)																
101	**Overall** (% boost of best case)	-	47.3	2.7	2.6	38.9	18.2	1.6	5.9	6.3	51.8	20.0	54.5	3.4	8.6	26.0	90.0
102	**Overall** (% of cases > 2% sensitivity)	-	81	3	6	44	22	0	8	6	94	44	75	81	3	51	100
103	**Overall** (% ave. probable boost)	-	**7.9**	**0.2**	**0.3**	**6.0**	**1.4**	**0.1**	**0.5**	**0.2**	**13.5**	**3.9**	**8.5**	**0.0**	**0.6**	**3.7**	**84.1**
	Tests: 1, 2, 3, 33, 36, 39, 44, 45, 46, 47, 56, 61, 63, 72, 73, 5, 8, 22, 55, 57, 59, 65, 67, (75-78), (4, 6), 9, 23, 24, 48, 58, (60, 66), (68, 74), (79-82)																

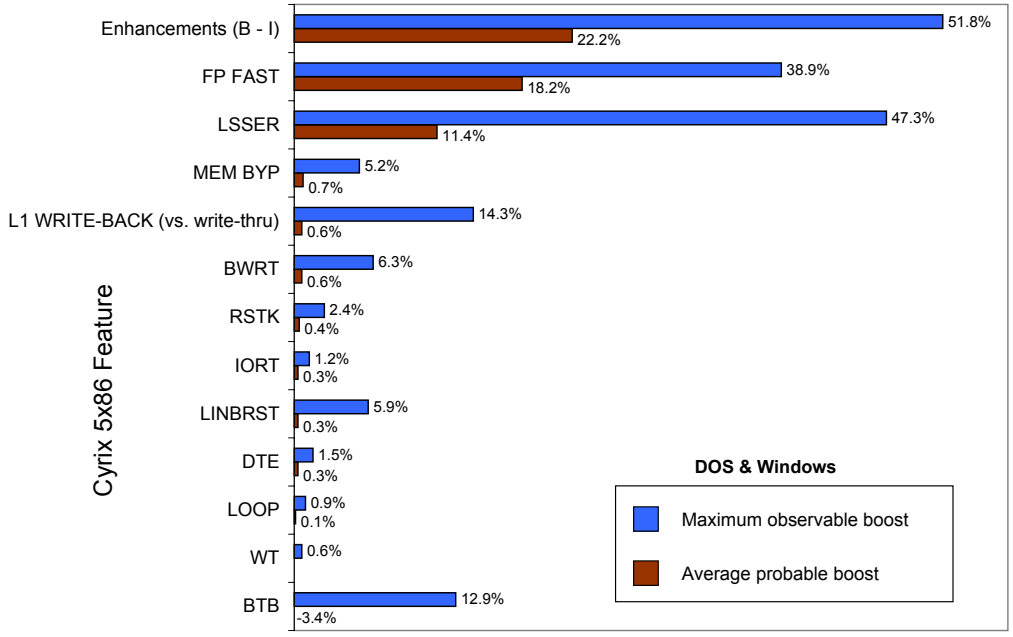
ALU Performance Boost



ALU Performance Boost



FPU Performance Boost



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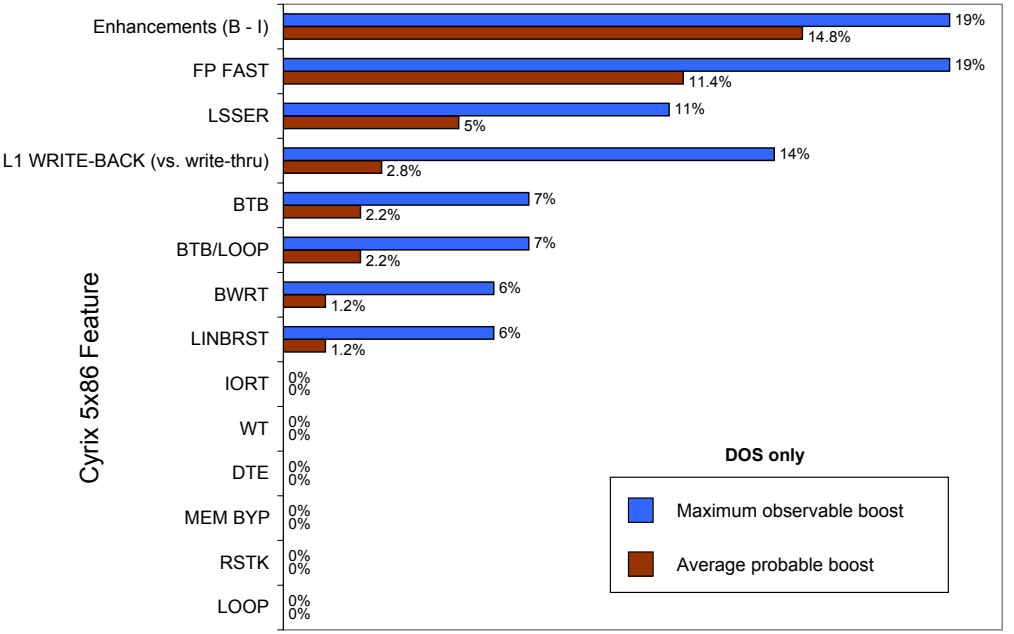
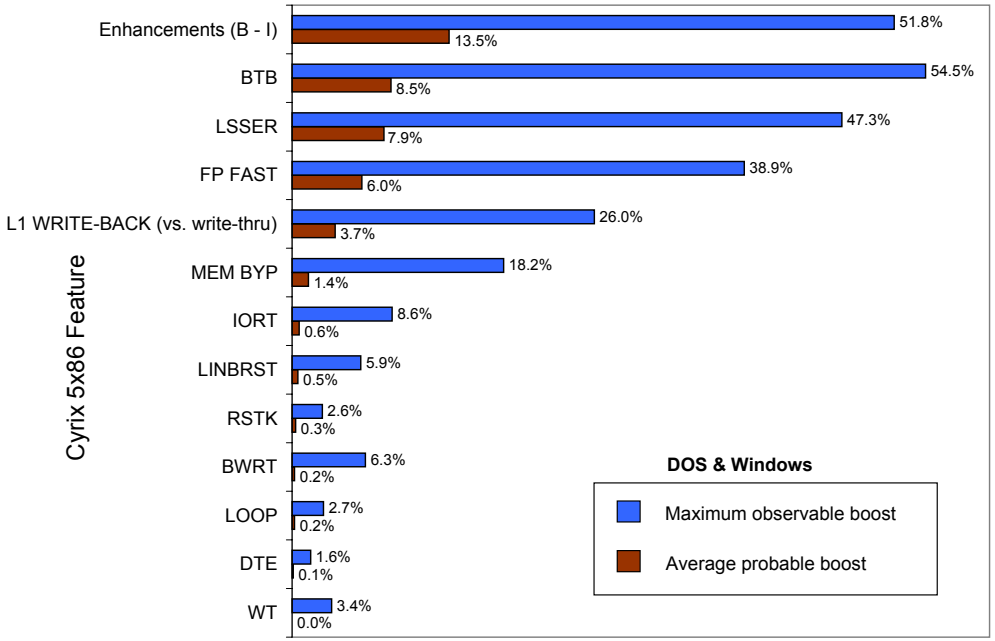


Overall Performance Boost



Overall Performance Boost