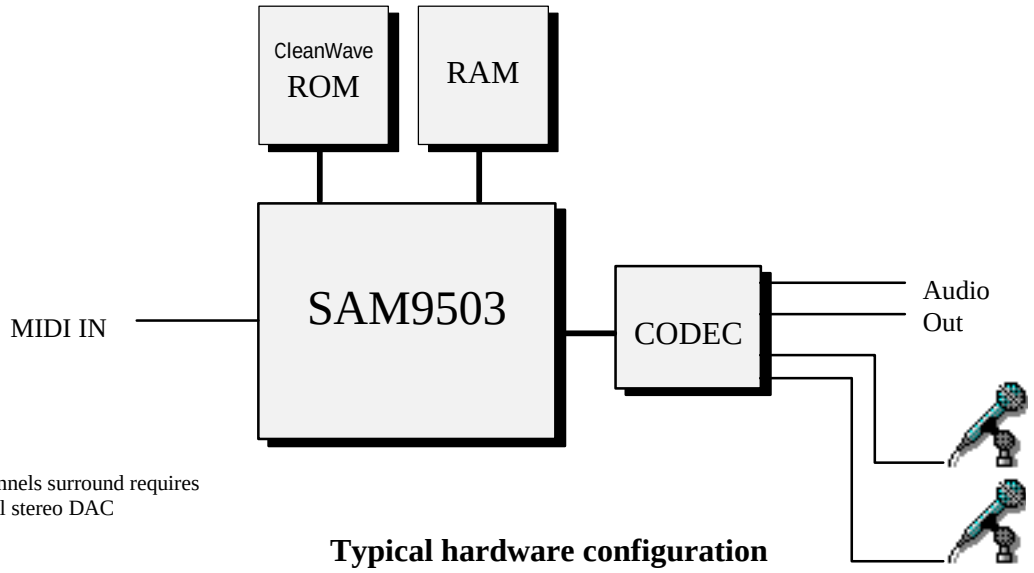
SAM9503

rev 2 - May 1997

PROFESSIONAL INTEGRATED SYNTHESIZER

- All-in-one design
  - MIDI control processor
  - Synthesis
  - Compatible effects : reverb + chorus
  - Microphone echo processing (2 channels)
  - Programmable Spatializer or four channels surround (*)
  - 4 bands stereo equalizer.
- High quality synthesis
  - Max 48 voices polyphony + reverb/chorus (34 if all features ON)
  - 24 dB resonant filter per voice
  - 16 bits samples
  - Alternate loop
  - Internal computations on 28 bits
- Crisp MIDI response : built-in 16 bit processor runs at 38.4 MHz
- High quality sound post-processing
  - 13 delay lines for stereo reverb
  - Programmable stereo echo for microphone
  - Spatializer/surround allows wide stereo image for strong sound presence
- Top technology
  - Synthesizer chip set : SAM9503 + 32Mbit ROM + 64kx8 RAM + DAC or Codec
  - Single 9.6 MHz crystal, built-in PLL
  - TQFP100 space saver package
- Standard firmware includes top quality CleanWave™ sound set.
- Typical applications : karaokes, musical instruments



(*) 4 channels surround requires additional stereo DAC

Typical hardware configuration

1- GENERAL DESCRIPTION

The highly integrated architecture from SAM9503 combines a specialized high performance RISC digital signal processor and a general purpose 16 bits CISC control processor on a single chip. An on-chip memory management unit allows the digital signal processor and the control processor to share external ROM and RAM devices. The ROM bus width should be 16 bits, while the SRAM can be selected to be 8 or 16 bits width. When using 8 bits SRAM, fast type (static cache) should be selected as two SRAM cycles will be done in one ROM cycle duration.

Running at 300 million operation per second (MOPS), the digital signal processor takes care of high quality PCM synthesis but also of most important functions like reverb, chorus, spatial effect, equalizer. By adding an additional stereo DAC, four channels audio surround can be obtained as well.

Computer karaoke manufacturers will enjoy the built-in high quality dual microphone echo processing.

Dream licenses a 32 Mbit jumper configurable firmware ROM CleanWave32TM which includes high quality GM compliant synthesis with many additional sounds and drumsets. Please refer to the corresponding CleanWave32TM data sheet.
Several reference designs are available which can be used for evaluation purposes. More information including licensing can be obtained from Dream sales offices.

Smaller capacity firmwares are also available for more cost sensitive or portable applications.

The firmware can also be modified to fit customers specifications. A SAM9503 based development / prototyping board is available, which includes the SAM9503, 32 Mbits of flash memory, 32k words of RAM, a Codec and one DAC, providing 4 channels of audio out, 2 microphone inputs and a stereo line input (ref. 9503DVB).

The SAM9503 internal sound definitions format is compatible with the SAM9407 sound studio IC. Therefore it is possible to develop specific sounds for the SAM9503 by using the development tools from the SAM9407.

The SAM9503 operates from a « low » frequency 9.6 MHz typical crystal. A built-in PLL rises this frequency to a 38.4 MHz internal clock which controls the two processors. Care has been taken that output pins signals change only when necessary. This allows to minimize RFI (radio frequency interferences) and power consumption. Minimizing RFI is mostly important to comply with standard such as FCC, CSA and CE.

2- PIN DESCRIPTION

2-1- PINS BY FUNCTION

Power supply group

PIN NAME	PIN #	TYPE	FUNCTION
GND	2,6,8,16,20,22,26,28, 38,46,49,53,59,71,75, 82,83, 94	PWR	DIGITAL GROUND All pins should be connected to a ground plane
VCC	1,7,15,21,27,37,48, 52,58,70,74,81,95	PWR	POWER SUPPLY, 5V +/- 10% All pins should be connected to a VCC plane
VC3	9,19,24,77	PWR	CORE POWER SUPPLY, 5V +/- 10% All pins should be connected to VCC. Future IC release will implement 3.3V core supply. Therefore it is advised to separate VC3 supply from VCC supply.

Serial MIDI

PIN NAME	PIN #	TYPE	FUNCTION
MIDI IN	17	IN	Serial TTL MIDI IN. All controls are received by this pin.

External ROM/RAM group

PIN NAME	PIN #	TYPE	FUNCTION
WA0-WA24	47,50,5154-57,60-69, 72,73,76,78-80,84,85	OUT	External ROM/RAM address for up to 32 Mega words (64MB) of memory. ROM memory holds firmware and PCM data. RAM memory holds working variables and effect delay lines.
WD0-WD15	86-93,96-100,3-5	I/O	External ROM/RAM data. Holds read data from ROM or RAM when WOE/ is low, write data to RAM when WWE/ is low.
WCS0/	34	OUT	External ROM chip select, active low
WCS1/	35	OUT	External RAM chip select, active low
WOE/	36	OUT	External ROM/RAM output enable, active low
WWE/	33	OUT	External RAM write, active low
RBS	25	OUT	Ram byte select. Used as lower address from RAM when 8 bit wide RAM is connected.

DIGITAL AUDIO GROUP

PIN NAME	PIN #	TYPE	FUNCTION
CLBD	23	OUT	Digital audio bit clock
WSBD	32	OUT	Digital audio left/right select
DABD0	30	OUT	Digital audio main stereo output
DABD1	31	OUT	Auxiliary digital stereo output. Reserved for surround effects.
DAAD	29	IN	Digital audio 2 channels input

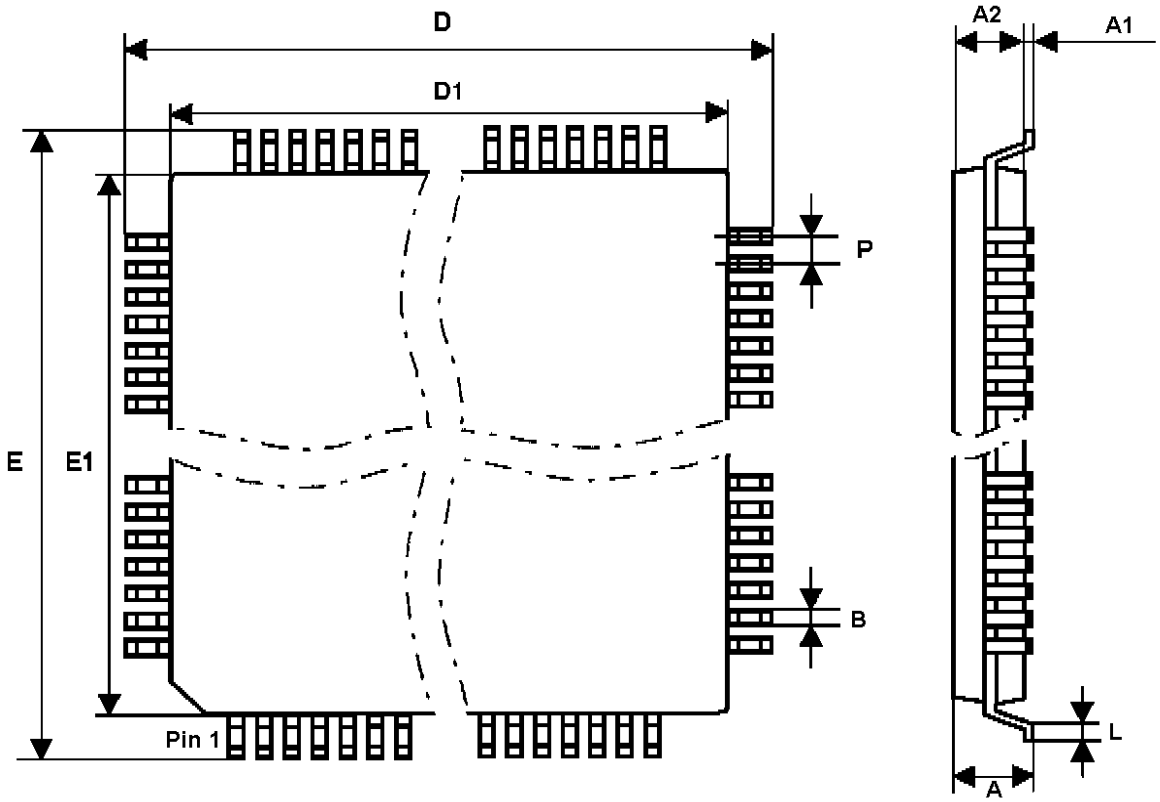
MISCELLANEOUS GROUP

PIN NAME	PIN #	TYPE	FUNCTION
X1-X2	12, 11	-	9.6 MHz crystal connection. An external 9.6 MHz clock can also be used on X1. X2 is at 256xFs, Fs being the sample frequency. Therefore X2 can be used to drive an external oversampling DAC.
LFT	10	-	PLL external RC network
RESET/	13	IN	Reset input, active low. This is a Schmidt trigger input, allowing direct connection of an RC network
PDWN/	14	IN	Power down, active low. When power down is active, then all output pins will be floated. The crystal oscillator will be stopped. To exit from power down, PDWN/ should be high and RESET applied.
TEST0-TEST2	43, 44, 45	IN	Test pins. Should be grounded
P0-P3	39, 40, 41, 42	I/O	General purpose I/O pins. As inputs can be used to configure the software.
RUN	18	OUT	When high, indicates that the synthesizer is up and running. May be used as a RESET/ input for an external DAC

2-2- PINOUT BY PIN

PIN#	PIN NAME	PIN #	PIN NAME	PIN#	PIN NAME	PIN#	PIN NAME
1	VCC	26	GND	51	WA2	76	WA19
2	GND	27	VCC	52	VCC	77	VC3
3	WD13	28	GND	53	GND	78	WA20
4	WD14	29	DAAD	54	WA3	79	WA21
5	WD15	30	DABD0	55	WA4	80	WA22
6	GND	31	DABD1	56	WA5	81	VCC
7	VCC	32	WSBD	57	WA6	82	GND
8	GND	33	WWE/	58	VCC	83	GND
9	VC3	34	WCS0/	59	GND	84	WA23
10	LFT	35	WCS1/	60	WA7	85	WA24
11	X2	36	WOE/	61	WA8	86	WD0
12	X1	37	VCC	62	WA9	87	WD1
13	RESET/	38	GND	63	WA10	88	WD2
14	PDWN/	39	P0	64	WA11	89	WD3
15	VCC	40	P1	65	WA12	90	WD4
16	GND	41	P2	66	WA13	91	WD5
17	MIDI IN	42	P3	67	WA14	92	WD6
18	RUN	43	TEST0	68	WA15	93	WD7
19	VC3	44	TEST1	69	WA16	94	GND
20	GND	45	TEST2	70	VCC	95	VCC
21	VCC	46	GND	71	GND	96	WD8
22	GND	47	WA0	72	WA17	97	WD9
23	CLBD	48	VCC	73	WA18	98	WD10
24	VC3	49	GND	74	VCC	99	WD11
25	RBS	50	WA1	75	GND	100	WD12

2-3- MECHANICAL DIMENSIONS



SAM9503
THIN PLASTIC 100 LEAD QUAD FLAT PACK (TQFP100)

	MIN.	NOM.	MAX.
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	15.90	16.00	16.10
D1	13.90	14.00	14.10
E	15.90	16.00	16.10
E1	13.90	14.00	14.10
L	0.45	0.60	0.75
P		0.50	
B	0.17	0.22	0.27

All dimensions in mm

3- ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature (Power applied)	-	-40	-	+85	°C
Storage temperature	-	-65	-	+150	°C
Voltage on any pin	-	-0.5	-	VCC+0.5	V
Supply voltage	VCC/VC 3	-0.5	-	6.5	V
Maximum IOL per I/O pin	-	-	-	10	mA

4- RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VCC	4.5	5.0	5.5	V
Supply voltage (note 1)	VC3	4.5	5.0	5.5	V
Operating ambient temperature	tA	0	-	70	°C

note 1 : Future issues will have VC3 = 3.3V and 5V tolerant I/Os

5- D.C. CHARACTERISTICS (TA=25°C, VCC,VC3=5V±10%)

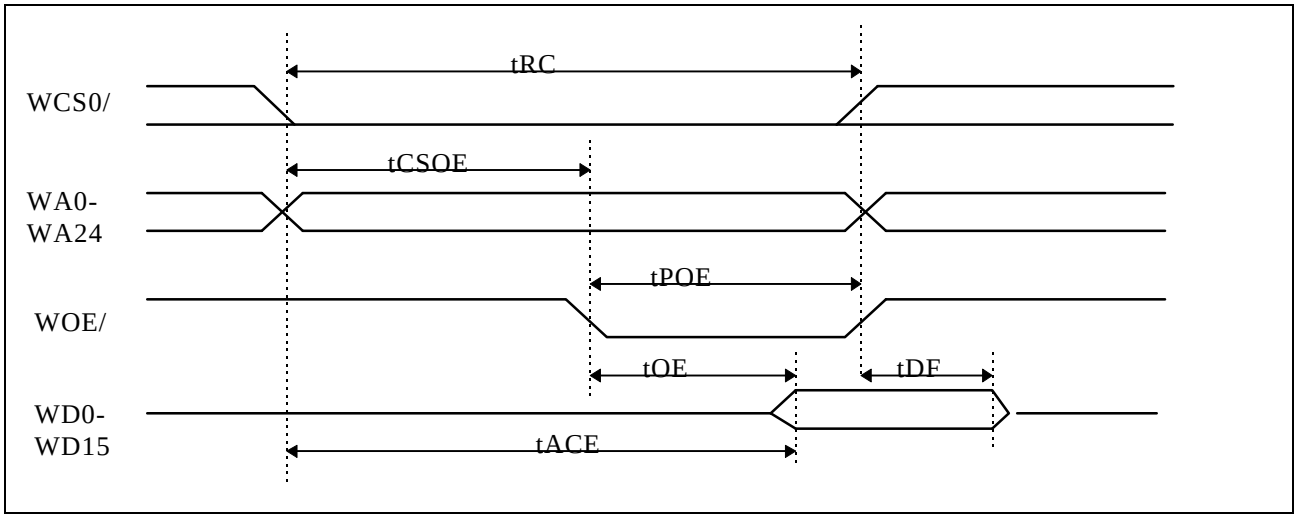
Parameter	Symbol	Min	Typ	Max	Unit
Low level input voltage	VIL	-0.5	-	0.8	V
High level input voltage	VIH	2.0	-	VCC+0.5	V
Low level output voltage IOL=-3.2mA	VOL	-	-	0.45	V
High level output voltage IOH=0.8mA	VOH	2.4	-	-	V
Power supply current (crystal freq.=9.6MHz)	ICC	-	40	100	mA
Power down supply current	-		100	150	µA

6- TIMINGS

All timing conditions : Ta=25°C, VCC=VC3=5V ± 5% all outputs except X2 and LFT load capacitance=30pF, crystal frequency or external clock at X1 = 9.6 MHz

6-1- EXTERNAL ROM TIMING

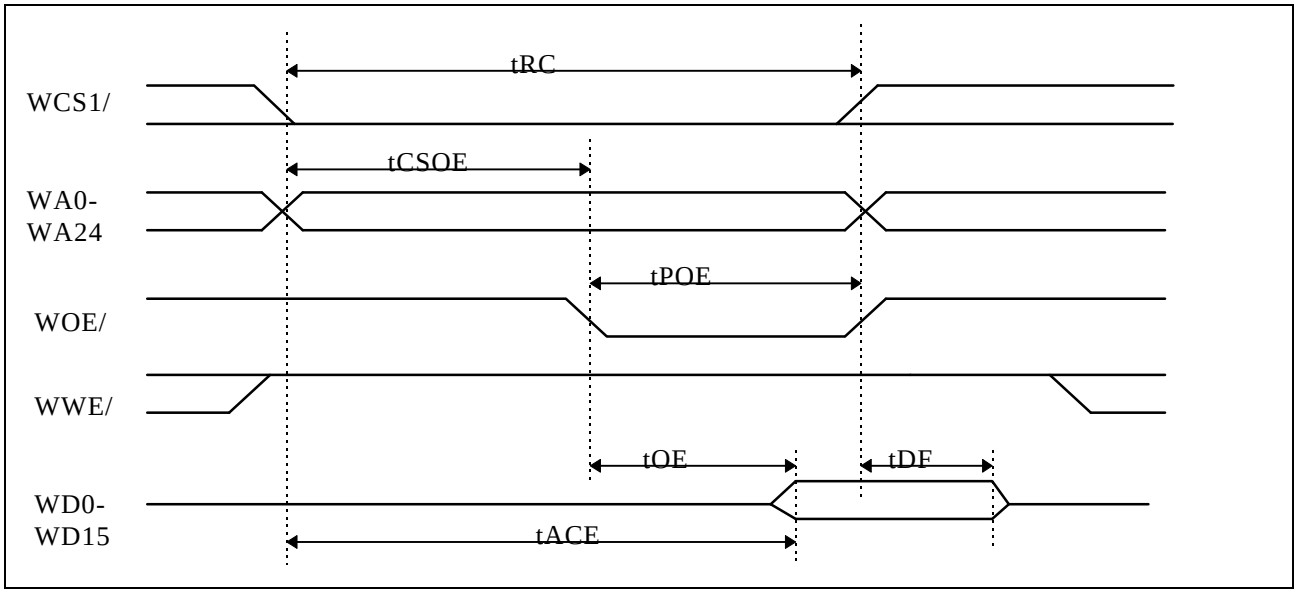
ROM READ CYCLE



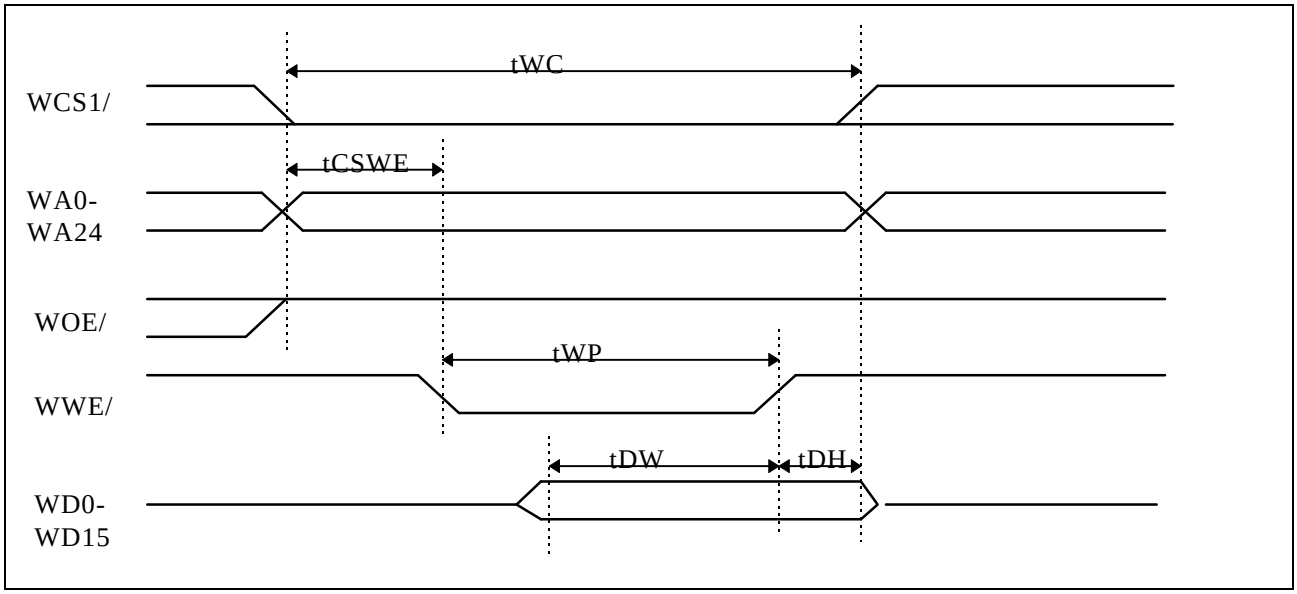
Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	130	-	-	ns
Chip select low / address valid to WOE/ low	tCSOE	45	-	80	ns
Output enable pulse width	tPOE	-	78	-	ns
Chip select/address access time	tACE	125	-	-	ns
Output enable access time	tOE	70	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	50	ns

6-2- EXTERNAL RAM TIMING

16 BIT SRAM READ CYCLE

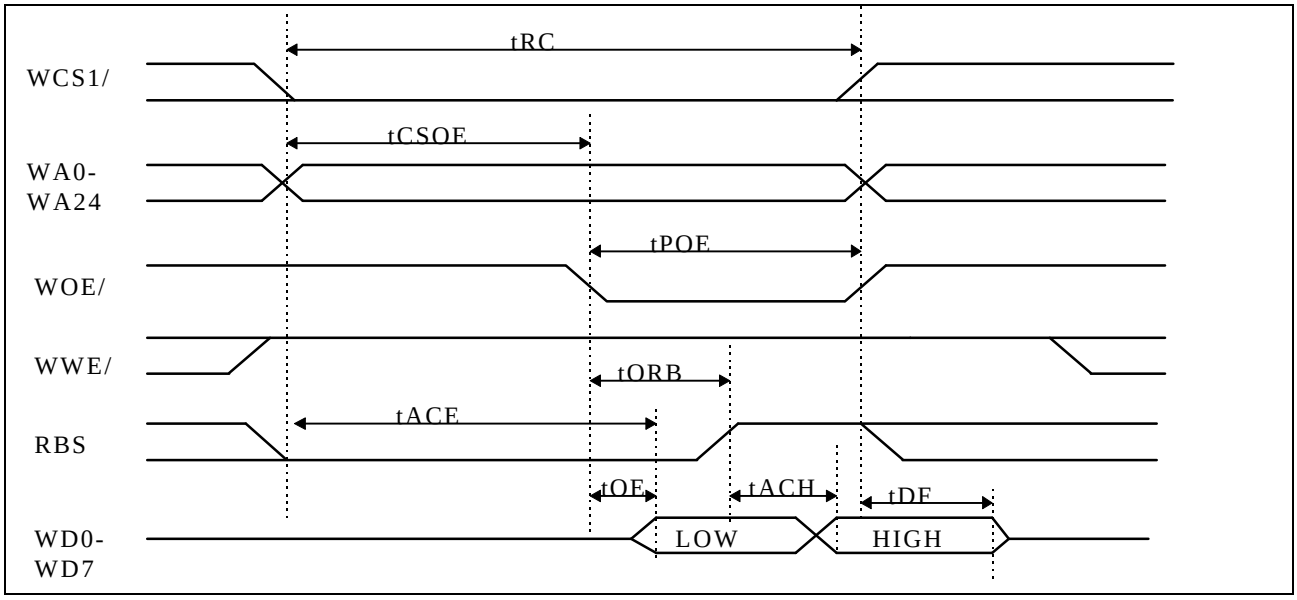


16 BIT SRAM WRITE CYCLE

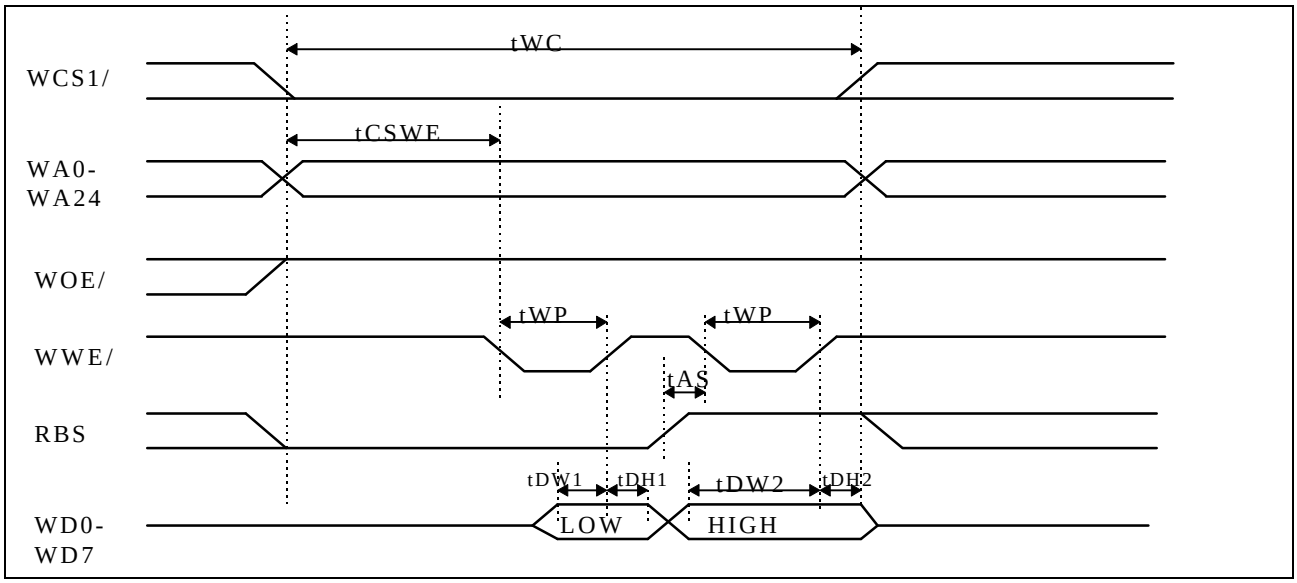


Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	130	-	-	ns
Chip select low / address valid to WOE/ low	tCSOE	45	-	80	ns
Output enable pulse width	tPOE	-	78	-	ns
Chip select/address access time	tACE	125	-	-	ns
Output enable access time	tOE	70	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	50	ns
Write cycle time	tWC	130	-	-	ns
Write enable low from CS/ or Address or WOE/	tCSWE	40	-	-	ns
Write pulse width	tWP	-	104	-	ns
Data out setup time	tDW	95	-	-	ns
Data out hold time	tDH	10	-	-	ns

8 BIT SRAM READ CYCLE

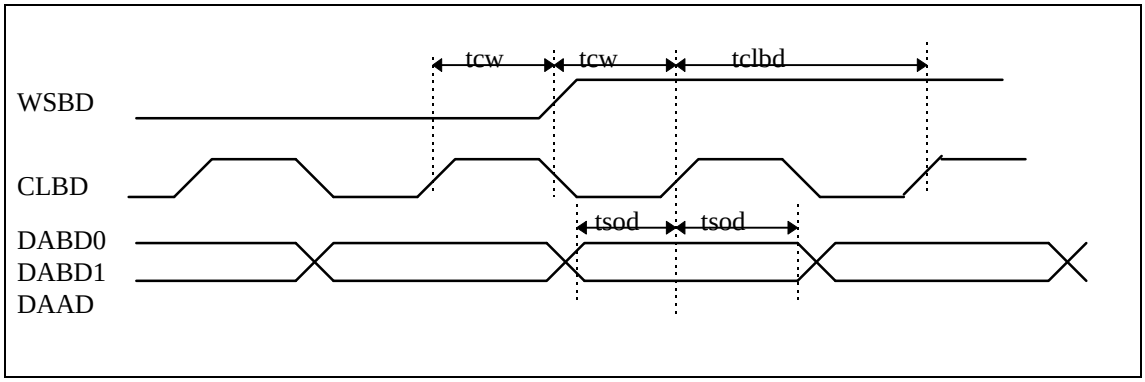


8 BIT SRAM WRITE CYCLE



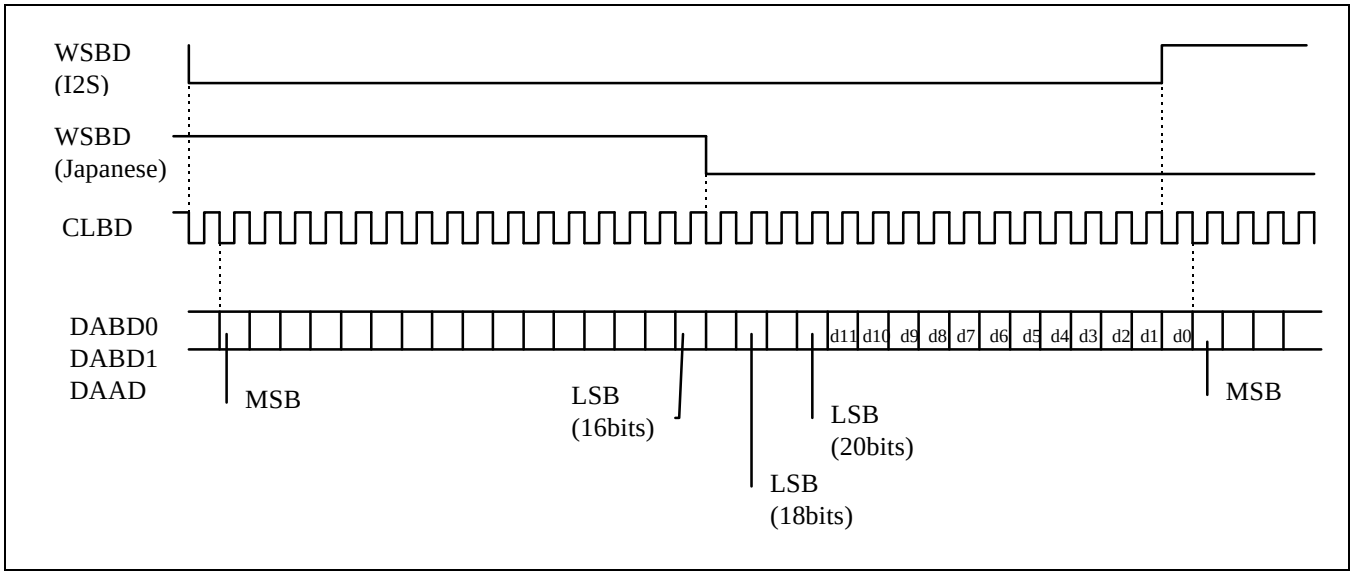
Parameter	Symbol	Min	Typ	Max	Unit
Word (2xbytes) read cycle time	tRC	130	-	-	ns
Chip select low / address valid to WOE/ low	tCSOE	45	-	80	ns
Output enable pulse width	tPOE	-	78	-	ns
Chip select / address low byte access time	tACE	70	-	-	ns
Output enable low byte access time	tOE	20	-	-	ns
Output enable low to byte select high	tORB	-	26	-	ns
Byte select high byte access time	tACH	45	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	50	ns
Word (2xbytes) write cycle time	tWC	130	-	-	ns
1st WWE/ low from CS/ or Address or WOE/	tCSWE	40	-	-	ns
Write (low & high byte) pulse width	tWP	20	-	-	ns
Data out low byte setup time	tDW1	25	-	-	ns
Data out low byte hold time	tDH1	20	-	-	ns
RBS high to second write pulse	tAS	8	-	-	ns
Data out high byte setup time	tDW2	40	-	-	ns
Data out high byte hold time	tDH2	10	-	-	ns

6-3- DIGITAL AUDIO TIMING



Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	200	-	-	ns
DABD valid prior/after CLBD rising	tsod	200	-	-	ns
CLBD cycle time	tclbd	-	416.67	-	ns

DIGITAL AUDIO FRAME FORMAT



Notes :
- Selection between I2S and Japanese format is a firmware option
- DAAD is 16 bits only
- When connected with codecs like CS4216 or CS4218, d0-d11 can be used to hold independent auxiliary information on left and right words. Refer to corresponding Codec data sheets for details

7- RESET AND POWER DOWN

During power-up, the RESET/ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20ms. A typical RC/diode power-up network can be used.
After the low to high transition of RESET/, following happens :

- The Synthesis enters an idle state.
- The RUN output is set to zero.
- Firmware execution starts from address 0100H in ROM space (WCS0/ low).

If PDWN/ is asserted low, then all I/Os and outputs will be floated, the crystal oscillator and PLL will be stopped. The chip enters a deep power down sleep mode. To exit power down, PDWN/ has to be asserted high, then RESET/ applied.

8- RECOMMENDED BOARD LAYOUT

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations :

- GND, VCC, VC3 distribution, decouplings

All GND, VCC, VC3 pins should be connected. GND + VCC planes are strongly recommended below the SAM9503. The board GND + VCC distribution should be in grid form. With current silicon releases, VC3 should be connected to VCC. Provision should be made for 3.3V VC3. The easiest way is to leave room for 2x1N4148 diodes in series between VCC and VC3.
Recommended decoupling is 0.1µF at each corner of the IC with an additional 10µFT decoupling close to the crystal.

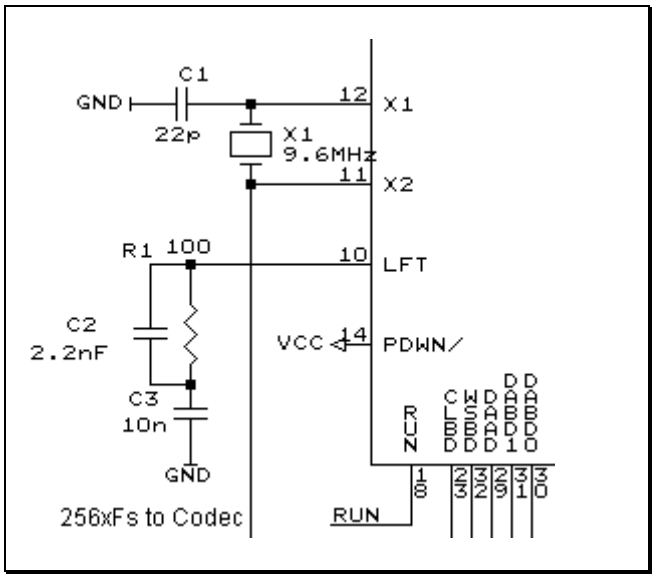
- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the SAM9407 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from SAM9503.

- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section.

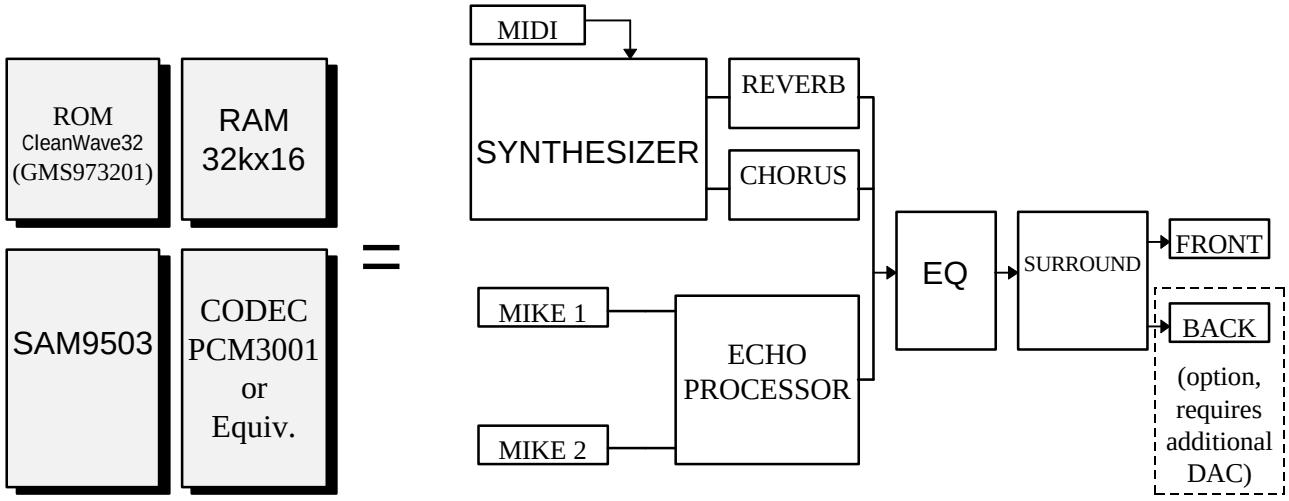
9- RECOMMENDED CRYSTAL COMPENSATION AND LFT FILTER



Note : If the X2 output is not used as a Codec clock, then an additional 22pF capacitor from X2 to GND should be implemented.

10- CleanWave32™ ROM FIRMWARE (ref. GMS973201)

- ROM includes firmware and PCM data
- Full GM implementation with top quality additional sounds
  - 128 General Midi sounds
  - 189 Variation sounds including sound effects
  - 9 drum sets + 1 SFX set
- Powerful MIDI implementation
- Built-in compatible reverb and chorus
- Built-in 4 bands parametric equalizer, fully controlable by MIDI
- Built-in Spatializer effect with MIDI control
- Microphone echo processing



HARDWARE **FUNCTION**

General MIDI logo under license of Midi Manufacturers Association

For detailed information about sound list and MIDI implementation, please request the CleanWave32 user's manual

11- REFERENCE DESIGNS

11-1- 9503DVB

SAM9503 + 2 x 16Mbit flash memories + 2 x 32K x 8 SRAMs + Codec + DAC

9503DVB can be used for CleanWave32 evaluation or other specific applications requiring less than 4 Mega bytes PCM data.

11-2- 9503DVB2 + DAC1305

9503DVB2 :
SAM9503 + sockets for 8 x 16MBits EPROMs + 2 x 32K x 8 SRAMs + Codec connector

DAC1305 :
High quality 20 bit matching DAC using Philips TDA1305T

This design can be used for top quality products prototyping with up to 16 Mega bytes PCM data. The separate DAC/Codec board allows evaluation of different DAC/Codec brands

Other designs / applications are or will become available. Please contact Dream distributors for up to date information.

NOTES :

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