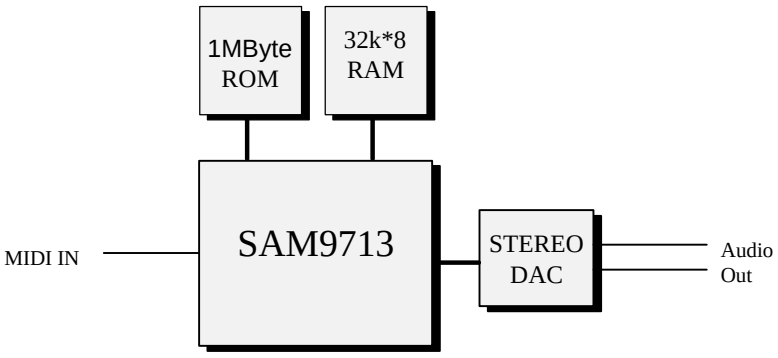
SAM9713

LOW COST INTEGRATED SYNTHESIZER WITH EFFECTS

- All-in-one design
  - MIDI control processor
  - Synthesis
  - Compatible effects : reverb + chorus
  - Programmable Spatializer or four channels surround (*)
  - 4 bands stereo equalizer.
- State of the art synthesis for best quality/price products
  - 34 voices polyphony + effects
  - Up to 1 Megabyte wavetable/firmware support
- Synthesizer chipset : SAM9713 + 8Mbit ROM + 32kx8 SRAM + DAC
- Hardware programmable DAC mode
  - I2S 16 to 20 bits
  - Japanese 16 bits
- Available firmware/sample set for turnkey designs
  - 8 Mbit GS GMS960800B (**)
  - 8 Mbit CleanWave® GMS970800B
- Typical applications : cost sensitive portable karaoke / VCD karaoke
- TQFP80 package : small footprint, easy mouting
- Ideal for battery operation
  - Low power
  - Power down mode
  - Wide supply voltage range : 3V to 4.5V core, 3V to 5.5V periphery

(*) Four channel surround requires additional DAC
(**) GMS960800B with express permission of Roland Corporation, special licensing conditions apply.
WARNING: GMS960800B may not be installed in any musical instrument except for electronic keyboards and synthesizers that have a sale price of less than $75 FOB. Using this product in the manufacture of musical instruments or selling this product for use in a musical instrument (other than the exceptions noted above) is a violation of the intellectual property rights of Roland Corporation and will result in liability for infringement.



Typical hardware configuration

Rev Jan 1998 – Objective specification.

1- GENERAL DESCRIPTION

The highly integrated architecture from SAM9713 combines a specialized high performance RISC digital signal processor and a general purpose 16 bits CISC control processor on a single chip. An on-chip memory management unit allows the digital signal processor and the control processor to share external ROM and RAM devices. The ROM bus width should be 16 bits, while the SRAM can be selected to be 8 or 16 bits width. When using 8 bits SRAM, fast type (static cache) should be selected as two SRAM cycles will be done in one ROM cycle duration.

Running at 300 million operation per second (MOPS), the digital signal processor takes care of high quality PCM synthesis but also of most important functions like reverb, chorus, surround effect, equalizer. By adding an additional stereo DAC, four channels audio surround can be obtained as well.

The SAM9713 operates from a « low » frequency 9.6 MHz typical crystal. A built-in PLL rises this frequency to a 38.4 MHz internal clock which controls the two processors. Care has been taken that output pins signals change only when necessary. This allows to minimize RFI (radio frequency interferences) and power consumption. Minimizing RFI is mostly important to comply with standard such as FCC, CSA and CE.

The core power supply for the SAM9713 should be from 3V to 4.5V, while the periphery supports supply from 3V to 5.5V. Therefore, by selecting 3.3V ROM, SRAM and DAC, it is possible to develop low power/low voltage portable applications.

2- PIN DESCRIPTION

2-1- PINS BY FUNCTION

Power supply group

PIN NAME	PIN #	TYPE	FUNCTION
GND	5,14,21,23,36,38,57 61,62,65,74	PWR	DIGITAL GROUND All pins should be connected to a ground plane
VCC	1,6,13,18,22,32,56 64,80	PWR	POWER SUPPLY, 3V to 5.5V All pins should be connected to a VCC plane
VC3	7,17,63	PWR	CORE POWER SUPPLY, 3V to 4.5V All pins should be connected to nominal 3.3V. If 3.3V is not available, then VC3 can be derived from 5V by two 1N4148 diodes in series.

Serial MIDI

PIN NAME	PIN #	TYPE	FUNCTION
MIDI IN	15	IN	Serial TTL MIDI IN. All controls are received by this pin.

External ROM/RAM group

PIN NAME	PIN #	TYPE	FUNCTION
WA0-WA18	37,39,41-55,58,59	OUT	External ROM/RAM address for up to 512 k words (8Mbits) of memory. ROM memory holds firmware and PCM data. RAM memory holds working variables and effect delay lines.
WD0-WD15	66-73,75-79,2-4	I/O	External ROM/RAM data. Holds read data from ROM or RAM when WOE/ is low, write data to RAM when WWE/ is low.
WCS0/	29	OUT	External ROM chip select, active low
WCS1/	30	OUT	External RAM chip select, active low
WOE/	31	OUT	External ROM/RAM output enable, active low
WWE/	28	OUT	External RAM write, active low
RBS	20	OUT	RAM byte select. Used as lower address from RAM when 8 bit wide RAM is connected.

DIGITAL AUDIO GROUP

PIN NAME	PIN #	TYPE	FUNCTION
CLBD	19	OUT	Digital audio bit clock
WSBD	27	OUT	Digital audio left/right select
DABD0	25	OUT	Digital audio main stereo output
DABD1	26	OUT	Auxiliary digital stereo output. Reserved for surround effects.
DAC/DAAD	24	IN	DAC type : 0 = I2S 16 to 20 bits, 1 = Japanese 16 bits Can also be used as digital audio input if 32k x 16 RAM is connected.

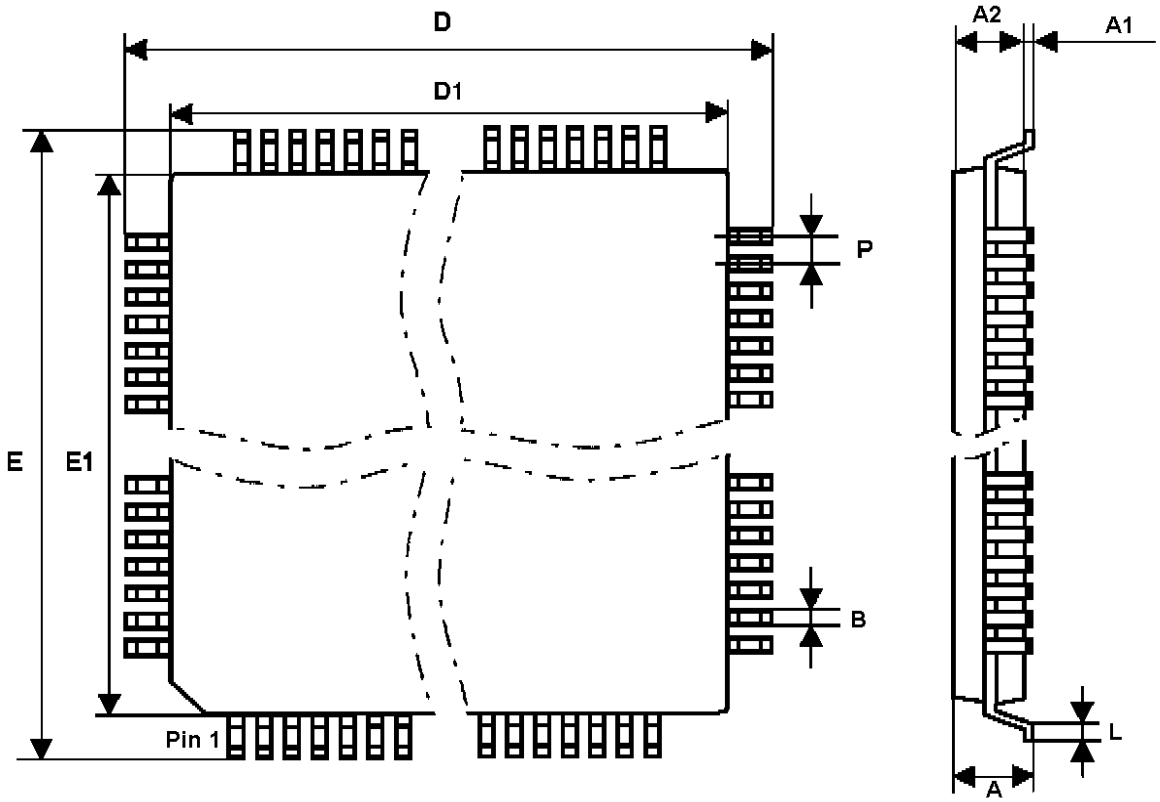
MISCELLANEOUS GROUP

PIN NAME	PIN #	TYPE	FUNCTION
X1-X2	10, 9	-	9.6 MHz crystal connection. An external 9.6 MHz clock can also be used on X1 (3.3V input). X2 cannot be used to drive external circuits.
LFT	8	-	PLL external RC network
RESET/	11	IN	Reset input, active low. This is a Schmidt trigger input, allowing direct connection of an RC network
PDWN/	12	IN	Power down, active low. When power down is active, then all output pins will be floated. The crystal oscillator will be stopped. To exit from power down, PDWN/ should be high and RESET applied.
TEST0-TEST2	33, 34, 35	IN	Test pins. Should be grounded
RUN	16	OUT	When high, indicates that the synthesizer is up and running.

2-2- PINOUT BY PIN

PIN#	PIN NAME	PIN #	PIN NAME	PIN#	PIN NAME	PIN#	PIN NAME
1	VCC	21	GND	41	WA2	61	GND
2	WD13	22	VCC	42	WA3	62	GND
3	WD14	23	GND	43	WA4	63	VC3
4	WD15	24	DAC/DAAD	44	WA5	64	VCC
5	GND	25	DABD0	45	WA6	65	GND
6	VCC	26	DABD1	46	WA7	66	WD0
7	VC3	27	WSBD	47	WA8	67	WD1
8	LFT	28	WWE/	48	WA9	68	WD2
9	X2	29	WCS0/	49	WA10	69	WD3
10	X1	30	WCS1/	50	WA11	70	WD4
11	RESET/	31	WOE/	51	WA12	71	WD5
12	PDWN/	32	VCC	52	WA13	72	WD6
13	VCC	33	TEST0	53	WA14	73	WD7
14	GND	34	TEST1	54	WA15	74	GND
15	MIDI IN	35	TEST2	55	WA16	75	WD8
16	RUN	36	GND	56	VCC	76	WD9
17	VC3	37	WA0	57	GND	77	WD10
18	VCC	38	GND	58	WA17	78	WD11
19	CLBD	39	WA1	59	WA18	79	WD12
20	RBS	40	DO NOT CONNECT	60	DO NOT CONNECT	80	VCC

2-3- MECHANICAL DIMENSIONS



SAM9713
THIN PLASTIC 80 LEAD QUAD FLAT PACK (TQFP80)

	MIN.	NOM.	MAX.
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	15.90	16.00	16.10
D1	13.90	14.00	14.10
E	15.90	16.00	16.10
E1	13.90	14.00	14.10
L	0.45	0.60	0.75
P		0.65	
B	0.22	0.32	0.38

All dimensions in mm

3- ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature (Power applied)	-	-40	-	+85	°C
Storage temperature	-	-65	-	+150	°C
Voltage on any pin (except X1)	-	-0.5	-	VCC+0.5	V
Supply voltage	VCC	-0.5	-	6.5	V
Supply voltage	VC3	-0.5	-	4.5	V
Maximum IOL per I/O pin	-	-	-	10	mA

4- RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage (note 1)	VCC	3	3.3/5.0	5.5	V
Supply voltage	VC3	3	3.3	4.5	V
Operating ambient temperature	tA	0	-	70	°C

note 1 : When using 3.3V VCC supply in a 5V environment, care must be taken that pin voltage does not exceed VCC+0.5V. Pin X1 is powered by VC3 input. If X1 is driven by a 5V device, then a minimum series resistor is required (typ 330 Ohms).

5- D.C. CHARACTERISTICS (TA=25°C, VC3=3.3V±10%)

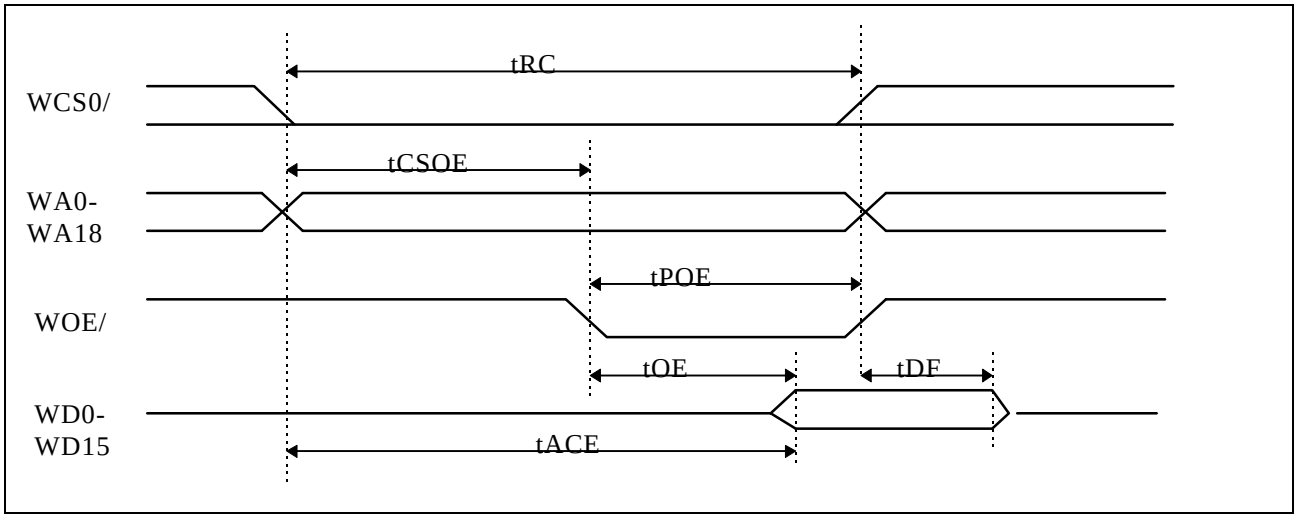
Parameter	Symbol	VCC	Min	Typ	Max	Unit
Low level input voltage	VIL	3.3 5.0	-0.5 -0.5	-	1.0 1.7	V
High level input voltage	VIH	3.3 5.0	2.3 3.3	-	VCC+0.5 VCC+0.5	V
Low level output voltage IOL=-3.2mA	VOL	3.3 5.0	-	-	0.45 0.45	V
High level output voltage IOH=0.8mA	VOH	3.3 5.0	2.8 4.5	-	-	V
Power supply current (crystal freq.=9.6MHz)	ICC	3.3 5.0	-	20 30	45 70	mA
Power down supply current	-			70	100	µA

6- TIMINGS

All timing conditions : Ta=25°C, VCC=5V, VC3=3.3V, all outputs except X2 and LFT load capacitance=30pF, crystal frequency or external clock at X1 = 9.6 MHz

6-1- EXTERNAL ROM TIMING

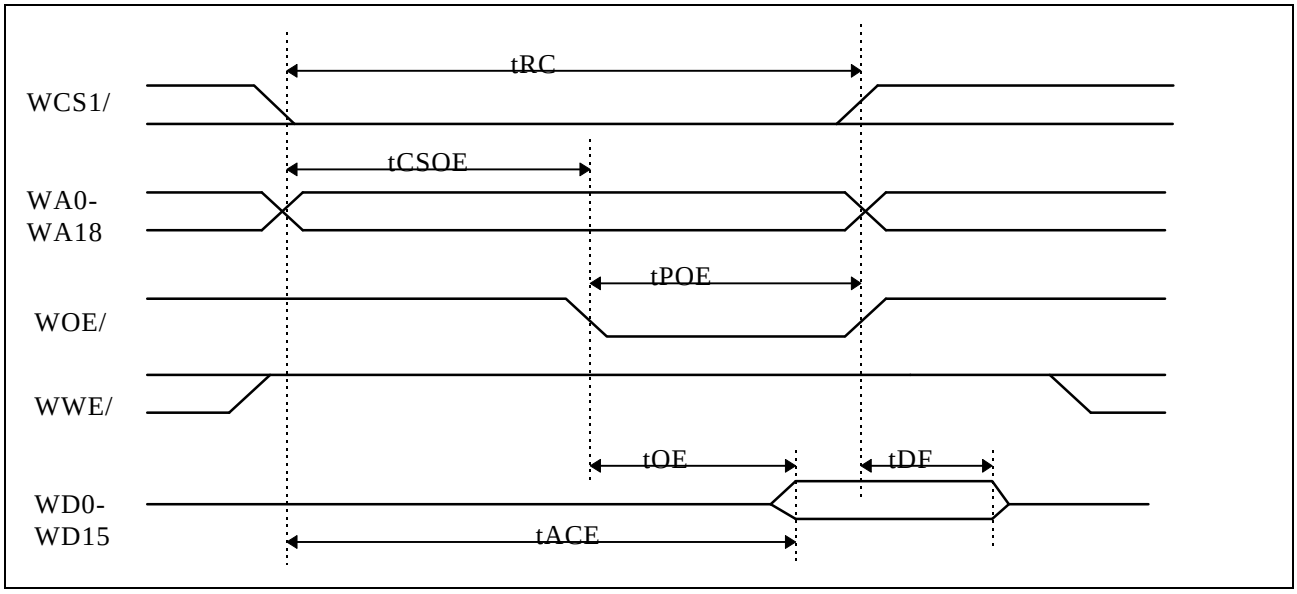
ROM READ CYCLE



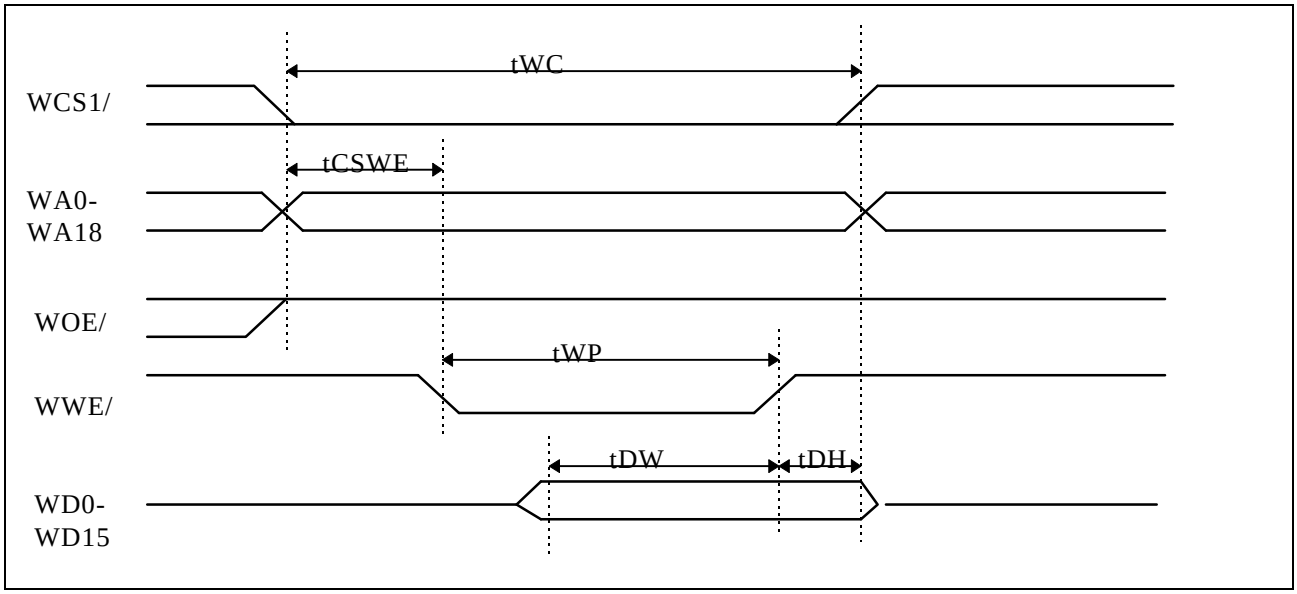
Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	130	-	-	ns
Chip select low / address valid to WOE/ low	tCSOE	45	-	80	ns
Output enable pulse width	tPOE	-	78	-	ns
Chip select/address access time	tACE	125	-	-	ns
Output enable access time	tOE	70	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	50	ns

6-2- EXTERNAL RAM TIMING

16 BIT SRAM READ CYCLE

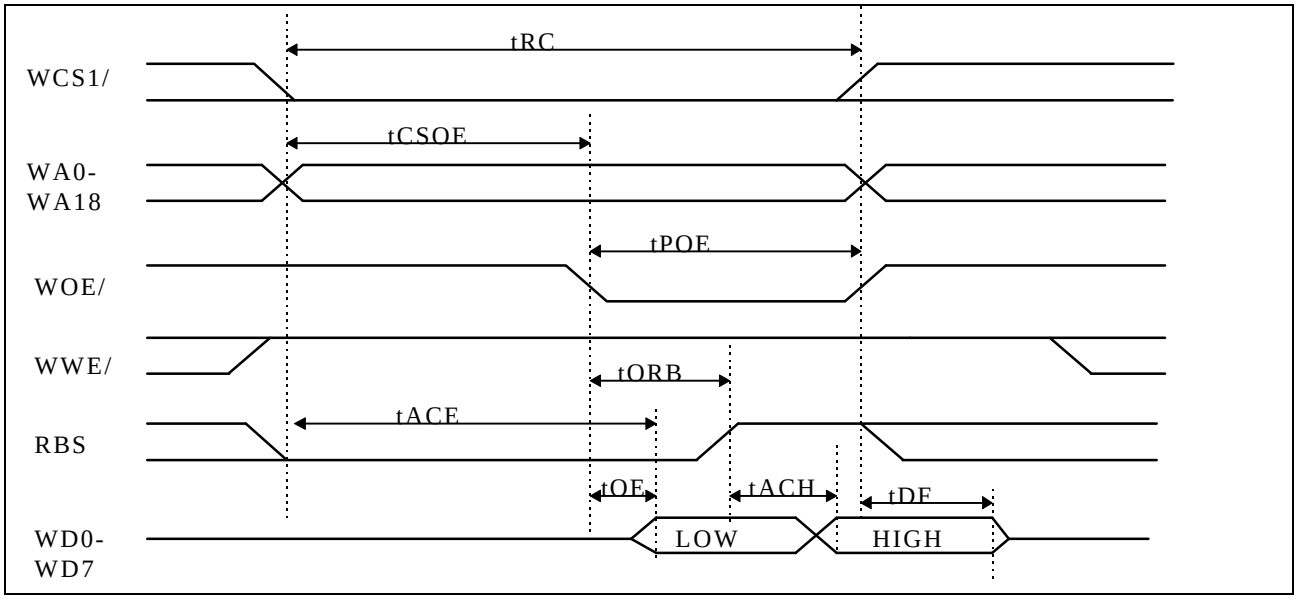


16 BIT SRAM WRITE CYCLE

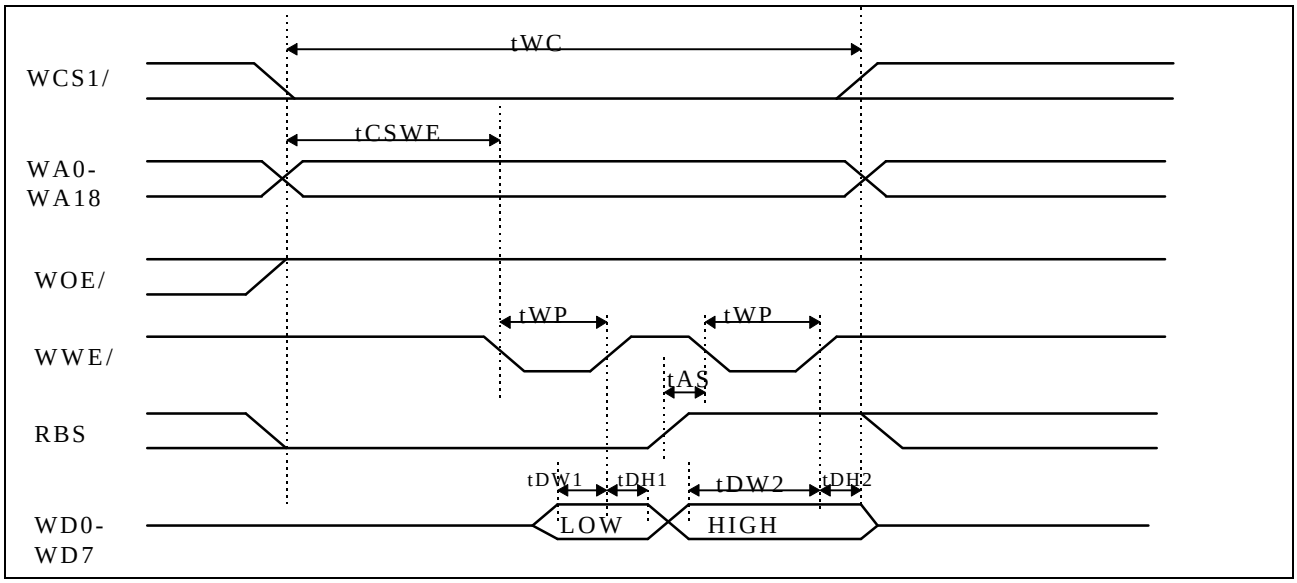


Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	130	-	-	ns
Chip select low / address valid to WOE/ low	tCSOE	45	-	80	ns
Output enable pulse width	tPOE	-	78	-	ns
Chip select/address access time	tACE	125	-	-	ns
Output enable access time	tOE	70	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	50	ns
Write cycle time	tWC	130	-	-	ns
Write enable low from CS/ or Address or WOE/	tCSWE	40	-	-	ns
Write pulse width	tWP	-	104	-	ns
Data out setup time	tDW	95	-	-	ns
Data out hold time	tDH	10	-	-	ns

8 BIT SRAM READ CYCLE

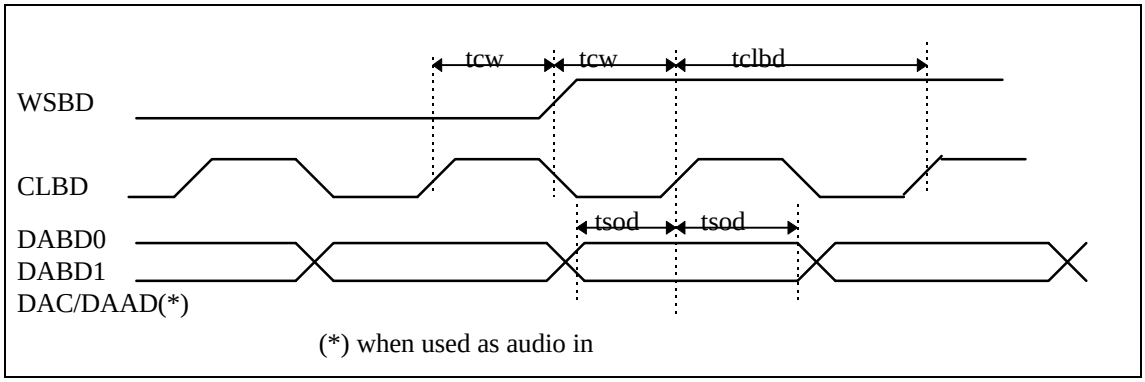


8 BIT SRAM WRITE CYCLE



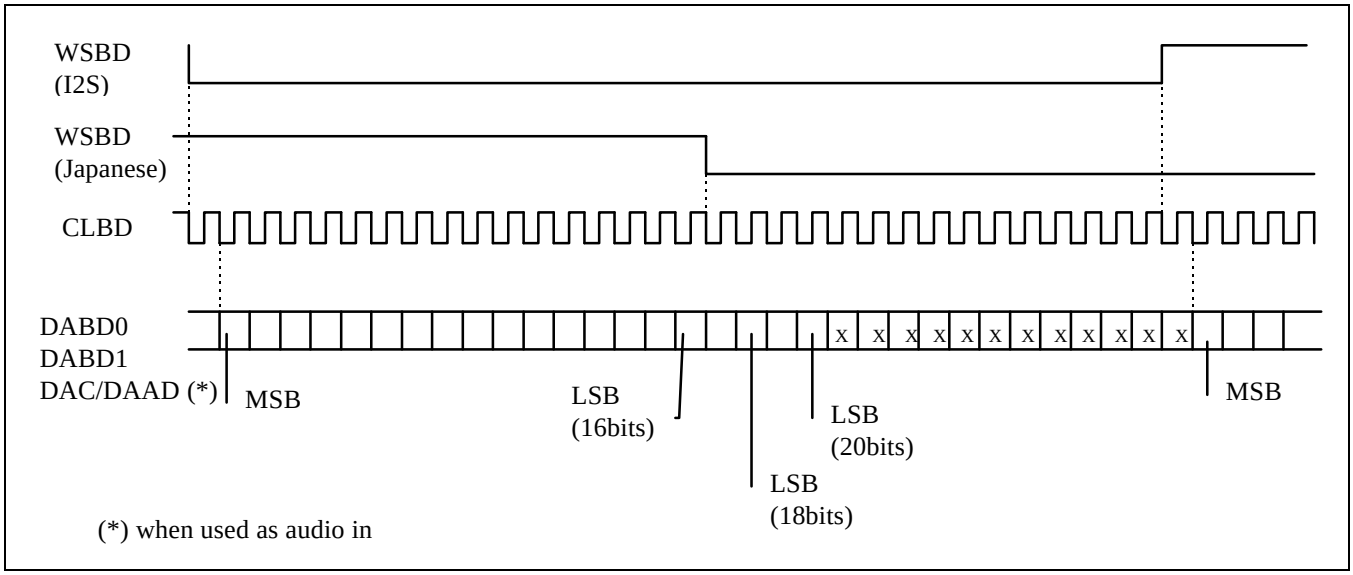
Parameter	Symbol	Min	Typ	Max	Unit
Word (2xbytes) read cycle time	tRC	130	-	-	ns
Chip select low / address valid to WOE/ low	tCSOE	45	-	80	ns
Output enable pulse width	tPOE	-	78	-	ns
Chip select / address low byte access time	tACE	70	-	-	ns
Output enable low byte access time	tOE	20	-	-	ns
Output enable low to byte select high	tORB	-	26	-	ns
Byte select high byte access time	tACH	45	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	50	ns
Word (2xbytes) write cycle time	tWC	130	-	-	ns
1st WWE/ low from CS/ or Address or WOE/	tCSWE	40	-	-	ns
Write (low & high byte) pulse width	tWP	20	-	-	ns
Data out low byte setup time	tDW1	25	-	-	ns
Data out low byte hold time	tDH1	20	-	-	ns
RBS high to second write pulse	tAS	8	-	-	ns
Data out high byte setup time	tDW2	40	-	-	ns
Data out high byte hold time	tDH2	10	-	-	ns

6-3- DIGITAL AUDIO TIMING



Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	200	-	-	ns
DABD valid prior/after CLBD rising	tsod	200	-	-	ns
CLBD cycle time	tclbd	-	416.67	-	ns

DIGITAL AUDIO FRAME FORMAT



Notes :
- Selection between I2S and Japanese format is through pin DAC/DAAD in case of 32kx8 SRAM.
- Digital audio in is available only in case of 32kx16 SRAM. In this case DAAD is 16 bits only.

7- RESET AND POWER DOWN

During power-up, the RESET/ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20ms. A typical RC/diode power-up network can be used.
After the low to high transition of RESET/, following happens :

- The Synthesis enters an idle state.
- The RUN output is set to zero.
- Firmware execution starts from address 0100H in ROM space (WCS0/ low).

If PDWN/ is asserted low, then all I/Os and outputs will be floated, the crystal oscillator and PLL will be stopped. The chip enters a deep power down sleep mode. To exit power down, PDWN/ has to be asserted high, then RESET/ applied.

8- RECOMMENDED BOARD LAYOUT

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations :

- GND, VCC, VC3 distribution, decouplings

All GND, VCC, VC3 pins should be connected. GND + VCC planes are strongly recommended below the SAM9713. The board GND + VCC distribution should be in grid form. For 5V VCC operation, if 3.3V is not available, then VC3 can be connected to VCC by two 1N4148 diodes in series. This guarantees a minimum voltage drop of 1.2V. Recommended VCC decoupling is 0.1µF at each corner of the IC with an additional 10µFT decoupling close to the crystal. VC3 requires a single 0.1 uF decoupling close to the IC.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the SAM9713 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from SAM9713.

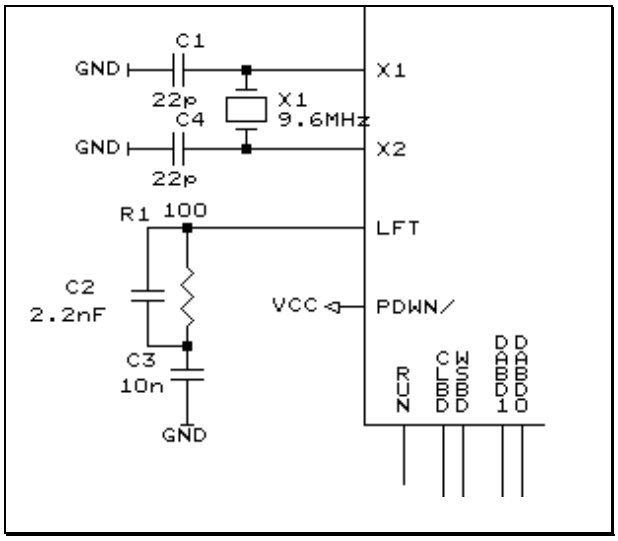
- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section.

- Unused inputs

Unused inputs should always be connected. A floating input can cause internal oscillation inside the IC, which can destroy the IC by dramatically increasing the power consumption. If you plan to use the power down feature, care should be taken that no pin is left floating during power down. Usually, a 1MOhm ground return is sufficient.

9- RECOMMENDED CRYSTAL COMPENSATION AND LFT FILTER



Note : the X2 output cannot be used to drive another circuit

NOTES :

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