SAM9733

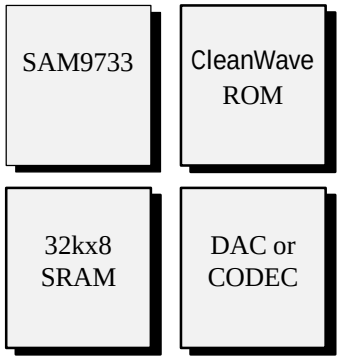
INTEGRATED SYNTHESIZER WITH EFFECTS

- Single chip synthesizer + effects, typical application includes :
  - wavetable synthesis, serial MIDI in & out, MPU-401 (UART)
  - effects : reverb + chorus, on MIDI and/or audio in
  - Surround on 2 or 4 speakers with intensity/delay control
  - Equalizer : 4 bands, parametric
  - Audio in processing through reverb, chorus, equalizer, surround
  - Independent microphone echo function for karaoke
- High quality wavetable synthesis
  - 16 bits samples, 44.1 KHz sampling rate, 24dB digital filter per voice
  - Up to 64 voices polyphony
- High performance
  - RISC structure for sound synthesis/processing
  - CISC structure for MIDI/MPU-401 communication and house-keeping
- Available wavetable firmwares and sample sets
  - CleanWave8® low cost General MIDI (GM) 1 megabyte firmware + sample set
  - CleanWave32® top quality 4 megabyte firmware + sample set
  - Other sample sets available under special conditions.
- Compatible
  - Firmware and sounds compatible with SAM9407/SAM9503
  - New applications can be developped using Dream SAM9407 standard development tools
- Low voltage, low power
  - Single low frequency crystal operation & built-in PLL minimize RFI
  - I/O from 3V to 5.5V, core 3.3V ± 10%
  - Power down mode
- Low cost
  - Industry standard PQFP100 package
- Typical applications
  - PC sound cards with the best quality/price ratio
  - Computer karaokes, portable karaokes
  - Keyboards, portable keyboards instruments

Release specification Sept. 1997

1- TYPICAL DESIGNS

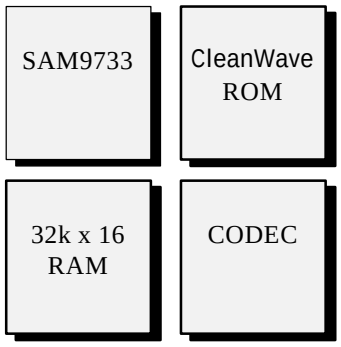
1-1- PC MULTIMEDIA



=

- √ **General Midi compliant wavetable synthesis**
- √ **MPU401 interface (UART)**
- √ **Compatible reverb + chorus**
- √ **Surround**
- √ **4 bands parametric equalizer**
- √ **Audio in effects (Codec required)**
- √ **Serial MIDI in & out**
- √ **4 channels output (extra DAC required)**

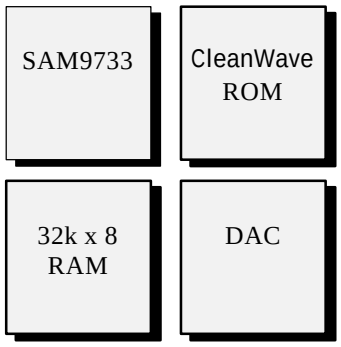
1-2- LOW COST KARAOKE, HAND-HELD KARAOKE



=

- √ **General Midi compliant synthesis**
- √ **Sound extensions (CleanWave32)**
- √ **Compatible reverb + chorus**
- √ **MIDI serial or 8 bit parallel interface**
- √ **Surround effect**
- √ **4 channels surround (requires extra DAC)**
- √ **4 bands equalizer**
- √ **Microphone echo**

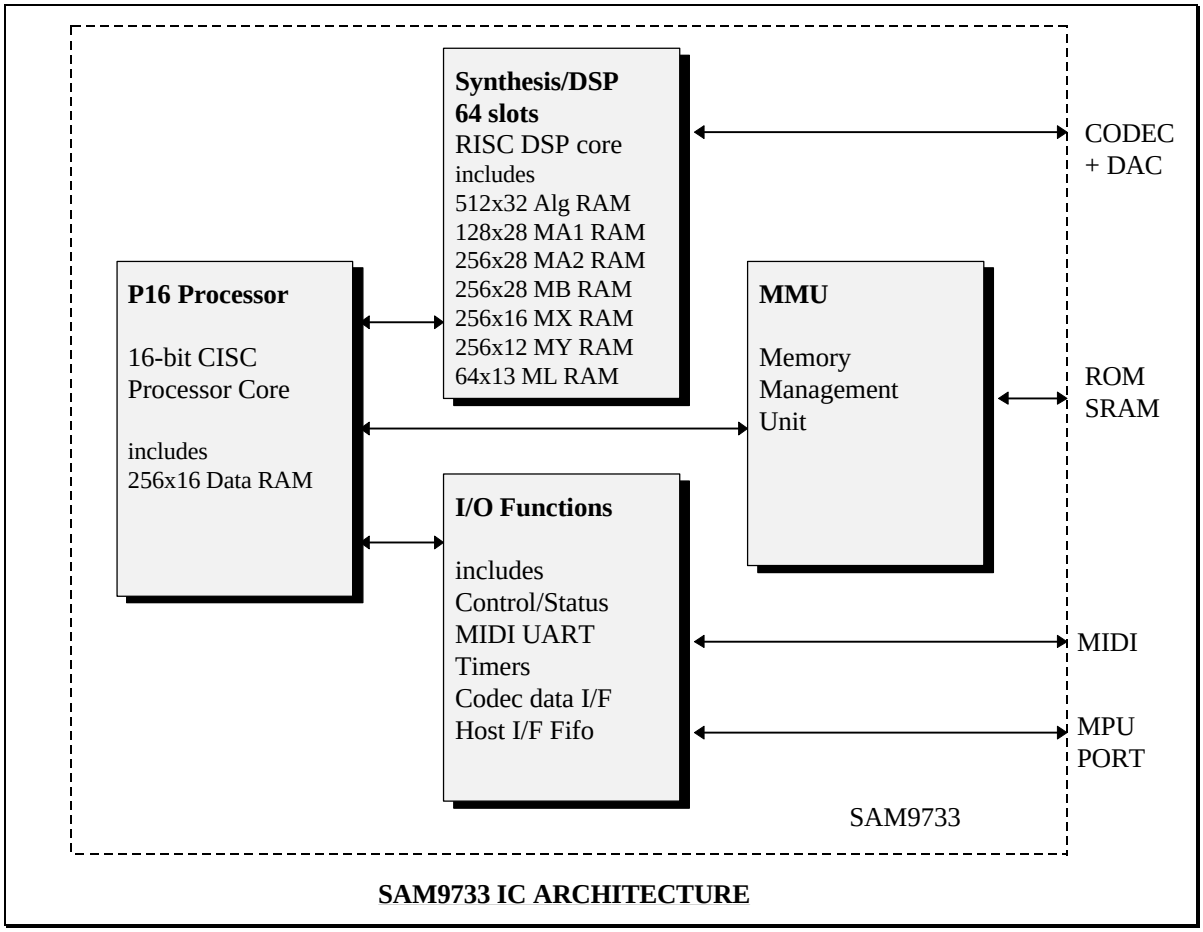
1.3 LOW COST KEYBOARD INSTRUMENT



=

- √ **General Midi compliant synthesis**
- √ **Sound extensions (CleanWave32)**
- √ **Compatible reverb + chorus**
- √ **MIDI serial or 8 bit parallel interface**
- √ **Surround effect**
- √ **4 bands parametric equalizer**

2- GENERAL DESCRIPTION



SAM9733 IC ARCHITECTURE

The SAM9733 is a low cost derivative of the SAM9407 and SAM9503. It retains the same high quality synthesis with up to 64 voices polyphony. The SAM9733 maximum wavetable memory is 4 megabytes and the ISA bus communication is through a standard MPU-401. The SAM9733 is packaged into an industry standard 100 pins plastic quad flat pack (PQFP100)

The highly integrated architecture from SAM9733 combines a specialized high-performance RISC-based digital signal processor (Synthesis/DSP) and a general purpose 16 bits CISC-based control processor on a single chip. An on-chip memory management unit (MMU) allows the synthesis/DSP and the control processor to share external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the ISA PC bus, the on-chip MIDI UART, and the Codec control interface, with minimum intervention from the control processor.

Synthesis/DSP engine

The synthesis/DSP engine operates on a frame timing basis with the frame subdivided into 64 processes slots. Each process is itself divided into 16 micro-instructions known as « algorithm ». Up to 32 synthesis/DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications. The synthesis/DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24dB resonant filtering for each voice. Slots may be

linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical application will use half the capacity of the synthesis/DSP engine for synthesis, thus providing state of the art 32 voices wavetable polyphony. The remaining processing power will be used for typical function like reverberation, chorus, audio in processing, surround effect, equalizer, etc.

Frequently accessed synthesis/DSP parameter data are stored into 5 banks of on-chip RAM memory. Sample data or delay lines, which are accessed relatively infrequently are stored in external ROM or SRAM memory. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20 ns (50 MIPS). Separate busses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to 6 simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 300 million operations per second (MOPS).

P16 control processor and I/O functions

The P16 control processor is a general purpose 16-bit CISC processor core, which runs from external memory. It includes 256 words of local RAM data memory.

The P16 control processor writes to the parameter RAM blocks within the synthesis/DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the PC ISA interface and then controls the Synthesis/DSP by writing into the parameter RAM banks in the DSP core. Slowly changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the ISA PC interface through specialized « intelligent » peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

The ISA PC interface is implemented using one address lines (A0), a chip select signal, read and write strobes from the host and an 8 bits data bus (D0-D7).
The data bus can drive the PC bus directly (24mA buffers). An external plug & play IC is required to map the 16 bits I/O addresses and AEN from the PC into the address line and chip select from the SAM9733.

The ISA PC interface is normally used to implement a MPU-401 UART-mode compatible interface, with address 0 being the data register and address 1 being the status/control registers. Besides the standard two status bits of the MPU-401, two additional bits are provided to expand the MPU-401 protocol.
Karaoke and keyboard applications can take advantage of the 8 bit MPU-401 interface to communicate with the SAM9733 at high speed, with the MIDI IN and MIDI OUT signals remaining available.

Memory Management Unit (MMU)

The Memory Management Unit (MMU) block allows external ROM and/or RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single device (i.e. SRAM) to serve as delay lines for the synthesis/DSP and as data memory for the P16 control processor.

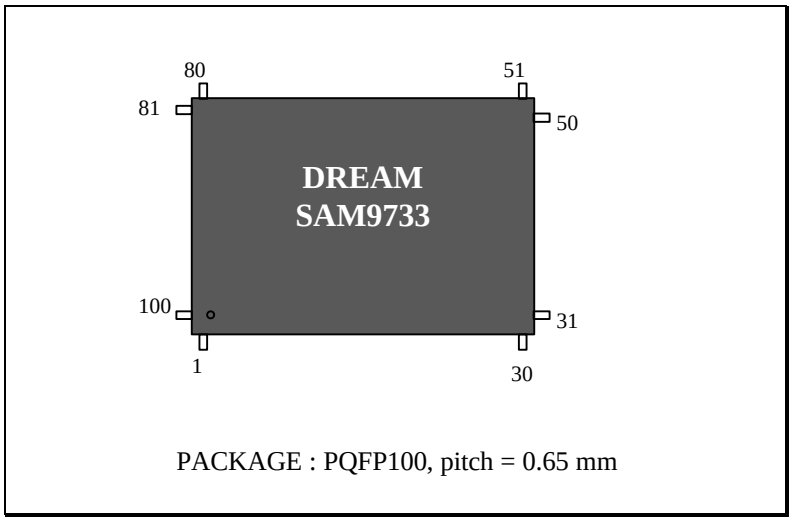
3- PIN DESCRIPTION

3-1- PIN BY FUNCTION

name	pin #	type	
GND	14	PWR	Power ground - all GND pins should be returned to digital ground
VC3	4	PWR	Core power +3.3V +/-10% all VC3 pins should be returned to +3.3V.
VCC	11	PWR	Power +3V to +5.5V - all VCC pins should be returned to +5V (or 3.3V in case of single 3.3V supply)
D0-D7	8	I/O	8 bit data bus to host processor. Has enough driving power to drive ISA PC bus directly (24mA buffer). Information on these pins is parallel MIDI (MPU-401 type applications) Direct ISA PC bus drive requires 5V VCC
CS/	1	IN	Chip select from host, active low.
WR/	1	IN	Write from host, active low.
RD/	1	IN	Read from host, active low.
A0	1	IN	Selects MPU-401 internal registers 0 : data registers (read/write) 1 : status register (read) control register (write)
IRQ	1	TSout	Tri-state output pin. Can be connected directly to host IRQ line (24mA).
RESET/	1	IN	Master reset input, active low. Schmidt trigger input.
X1,X2	2	-	Crystal connection. Crystal frequency should be Fs*256 (typ 11.2896 MHz) Xtal frequency is internally multiplied by 4 to provide the IC master clock. X1 can also be used as external clock input (3.3V input). X2 cannot be used to drive external ICs
DABD0-1	2	OUT	Two stereo serial audio data output (4 audio channels). Each output holds 64 bits (2x32) of serial data per frame. Audio data has up to 20 bits precision. DABD0 can hold additional control data (mute, A/D gain, D/A gain, etc.)
CLBD	1	OUT	Audio data bit clock, provides timing to DABD0-1.
WSBD	1	OUT	Audio data word select. The timing of WSBD can be selected to be I2S or Japanese compatible.
DAAD	1	IN	Stereo serial audio data input.
MIDI IN	1	IN	TTL level MIDI IN input
MIDI OUT	1	OUT	TTL level MIDI OUT output
WA0-20	21	OUT	External memory address (ROM/SRAM). Up to 4 Mega bytes ROM
WD0-15	16	I/O	PCM ROM/SRAM data
RBS	1	OUT	SRAM byte select : should be connected to the lower RAM address when 8 bit wide SRAM is used. The type of RAM (16bits/8bits) can be selected by program
WCS0/	1	OUT	PCM ROM chip select, active low
WCS1/	1	OUT	SRAM chip select, active low
WWE/	1	OUT	SRAM write enable, active low.
WOE/	1	OUT	PCM ROM/SRAM output enable, active low
RUN	1	OUT	High when the synthesis is initialized. Can be used as RESET/ for an external device (CODEC).
LFT	1	ANA	PLL low pass filter : should be connected to an external RC network
TEST0-2	3	IN	Test pins, should be returned to GND.
PDWN/	1	IN	Power down, active low

3-2- PIN-OUT BY PIN

pin#	signal name	pin#	signal name	pin#	signal name	pin#	signal name
1	VCC	31	VCC	51	WA1	81	VC3
2	IRQ	32	D3	52	WA2	82	WA20
3	GND	33	GND	53	D6	83	VCC
4	WD13	34	DAAD	54	VCC	84	GND
5	MIDI OUT	35	DABD0	55	D7	85	WD0
6	WD14	36	DABD1	56	GND	86	WD1
7	WD15	37	WSBD	57	WA3	87	WD2
8	GND	38	WWE/	58	WA4	88	WD3
9	VCC	39	WCS0/	59	WA5	89	WD4
10	GND	40	WCS1/	60	WA6	90	WD5
11	VC3	41	WOE/	61	VCC	91	WD6
12	LFT	42	VCC	62	GND	92	WD7
13	X2	43	GND	63	WA7	93	GND
14	X1	44	TEST0	64	WA8	94	CS/
15	RESET/	45	TEST1	65	WA9	95	VCC
16	PDWN/	46	TEST2	66	A0	96	WD8
17	VCC	47	GND	67	WA10	97	WD9
18	GND	48	WA0	68	WA11	98	WD10
19	MIDI IN	49	D4	69	WA12	99	WD11
20	RUN	50	D5	70	WA13	100	WD12
21	VC3			71	WA14		
22	GND			72	WA15		
23	VCC			73	WA16		
24	GND			74	WR/		
25	D0			75	VCC		
26	CLBD			76	RD/		
27	VC3			77	GND		
28	D1			78	WA17		
29	RBS			79	WA18		
30	D2			80	WA19		



PACKAGE : PQFP100, pitch = 0.65 mm

4- ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature (Power applied)	-	-40	-	+85	°C
Storage temperature	-	-65	-	+150	°C
Voltage on any pin X1 Others	- -	-0.5 -0.5	- -	VC3+0.5 VCC+0.5	V V
Supply voltage	VCC VC3	-0.5 -0.5	- -	6.5 4.5	V V
Maximum IOL per I/O pin	-	-	-	10 30 (D0-D7,IRQ)	mA mA

5- RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage (note 1)	VCC	3	3.3/5.0	5.5	V
Supply voltage	VC3	3	3.3	3.6	V
Operating ambient temperature	tA	0	-	70	°C

note 1 : D0-D7 and IRQ can only be connected to PC ISA bus if VCC = 5V ± 10%

6- D.C. CHARACTERISTICS (TA=25°C, VCC=3 to 5.5V, VC3=3.3V±10%)

Parameter	Symbol	VCC	Min	Typ	Max	Unit
Low level input voltage	VIL	3.3 5.0	-0.5 -0.5	-	1.0 1.7	V
High level input voltage	VIH	3.3 5.0	2.3 3.3	-	VCC+0.5 VCC+0.5	V
Low level output voltage D<7:0>, IRQ : IOL=-24mA others except LFT, X2 : IOL=-3.2mA	VOL	3.3 5.0	-	-	0.45 0.45	V
High level output voltage D<7:0>, IRQ : IOH=10mA others except LFT, X2 : IOH=0.8mA	VOH	3.3 5.0	2.8 4.5	-	-	V
Power supply current (crystal freq.=12MHz)	ICC		-	30	70	mA
Power down supply current	-			70	100	µA

7- TIMINGS

All timings conditions : VCC=5V, VC3=3.3V, Ta=25°C, signals D0-D7 with 220 ohms pull-up, 30pF capacitance, signal IRQ with 470 ohms pull-down, 30pF capacitance, all other outputs except X2 and LFT load capacitance=30pF.
All timings refer to tck, which is the internal master clock period.
The internal master clock frequency is 4 times the frequency at pin X1. Therefore tck=txtal/4.
The sampling rate is given by 1/(tck*1024). The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 KHz sampling rate).

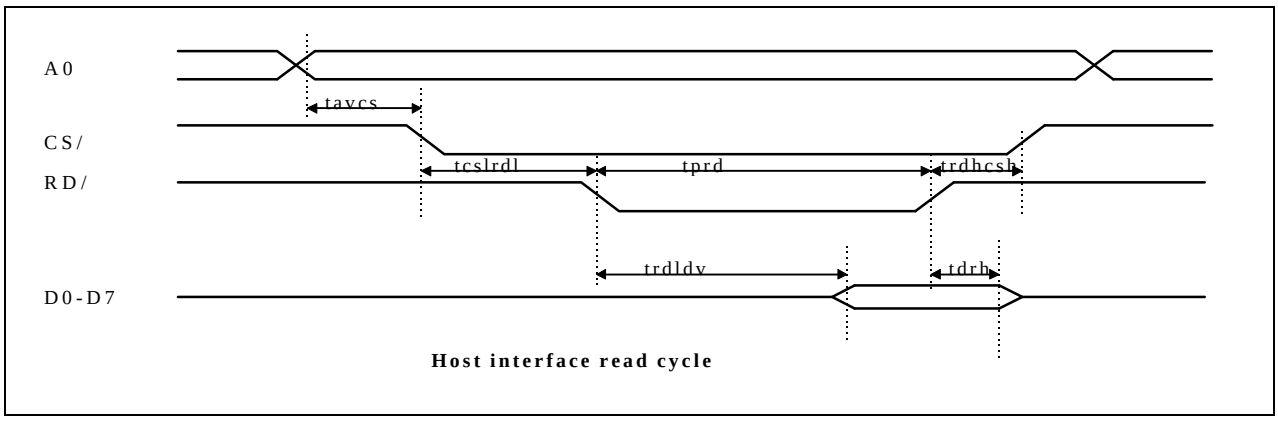
7-1- CRYSTAL FREQUENCY SELECTION CONSIDERATIONS

There is a trade-off between the crystal frequency and the support of widely available external ROM components. The following chart allows to select the best fit for a given application :

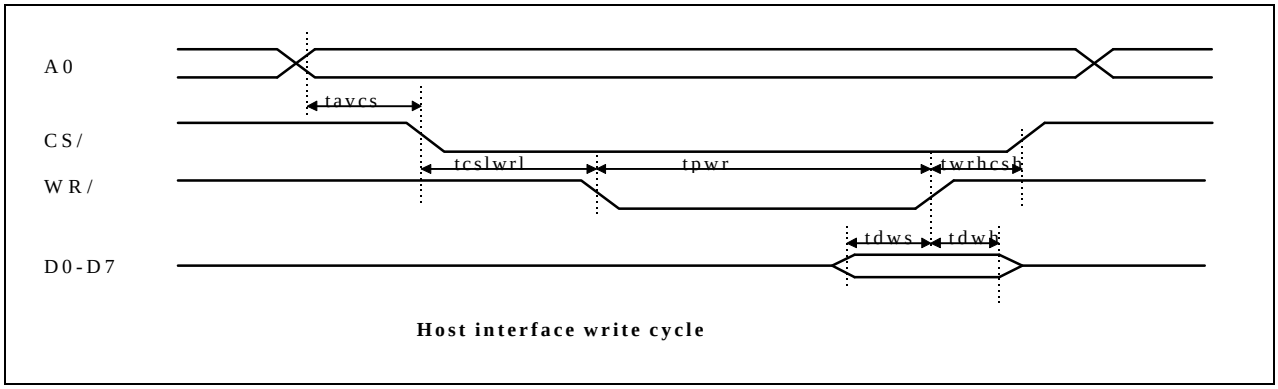
Sample rate (KHz)	Xtal (MHz)	tck (ns)	ROM tA (ns)	COMMENT
48	12.288	20.35	92	maximum frequency
44.1	**11.2896**	**22.14**	**101**	**Recommended for current designs**
37.5	9.60	26.04	120	
31.25	8.00	31.25	146	

Using 11.2896 MHz crystal frequency allows to use widely available ROMs with 100ns access time, while providing state of the art 44.1 KHz sampling rate

7-2- PC HOST INTERFACE



Host interface read cycle

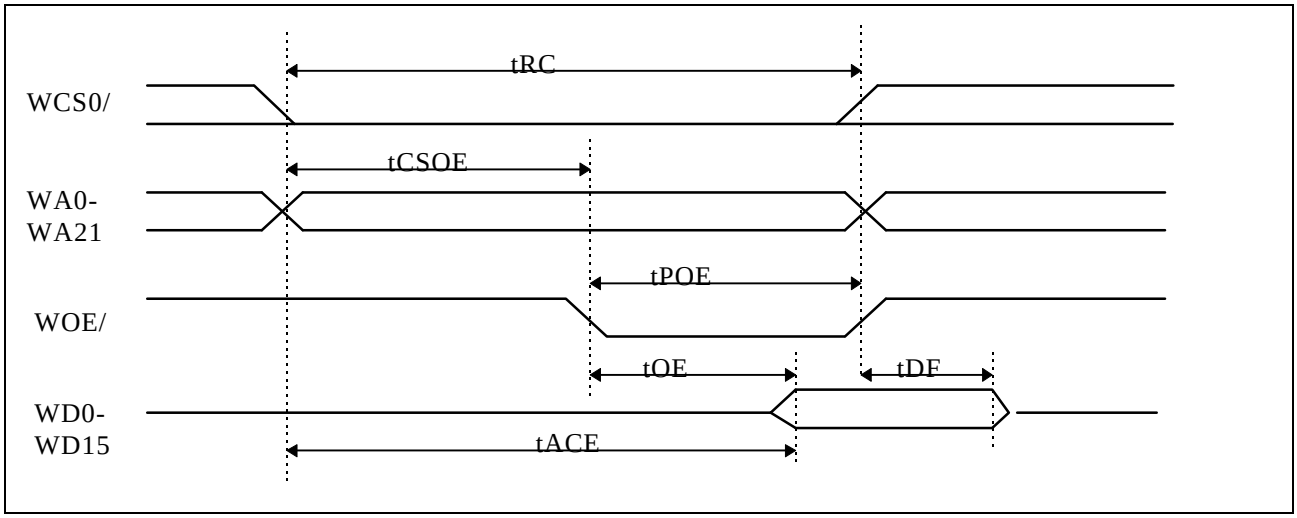


Host interface write cycle

Parameter	Symbol	Min	Typ	Max	Unit
Address valid to chip select low	tavcs	0	-	-	ns
Chip select low to RD/ low	tcslrdl	5	-	-	ns
RD/ high to CS/ high	trdhcsh	5	-	-	ns
RD/ pulse width	tprd	50	-	-	ns
Data out valid from RD/	trdldv	-	-	20	ns
Data out hold from RD/	tdrh	5	-	10	ns
Chip select low to WR/ low	tcslrwrl	5	-	-	ns
WR/ high to CS/ high	twrhcsh	5	-	-	ns
WR/ pulse width	tpwr	50	-	-	ns
Write data setup time	tdws	10	-	-	ns
Write data hold time	tdwh	0	-	-	ns

7-3- EXTERNAL ROM TIMING

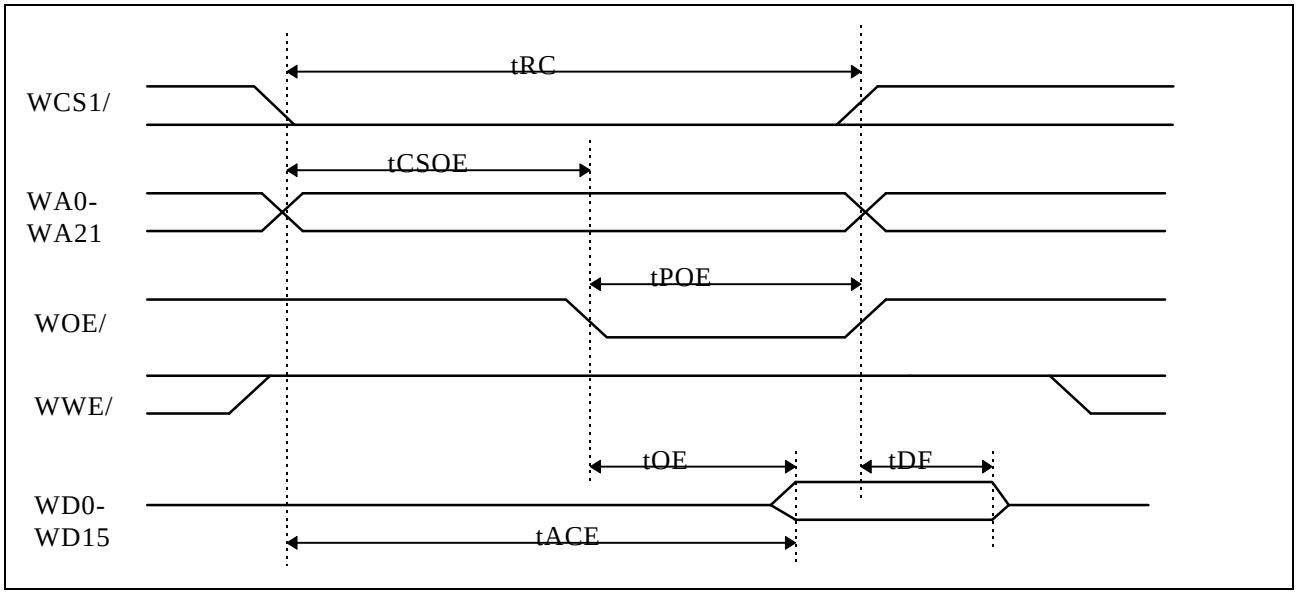
ROM READ CYCLE



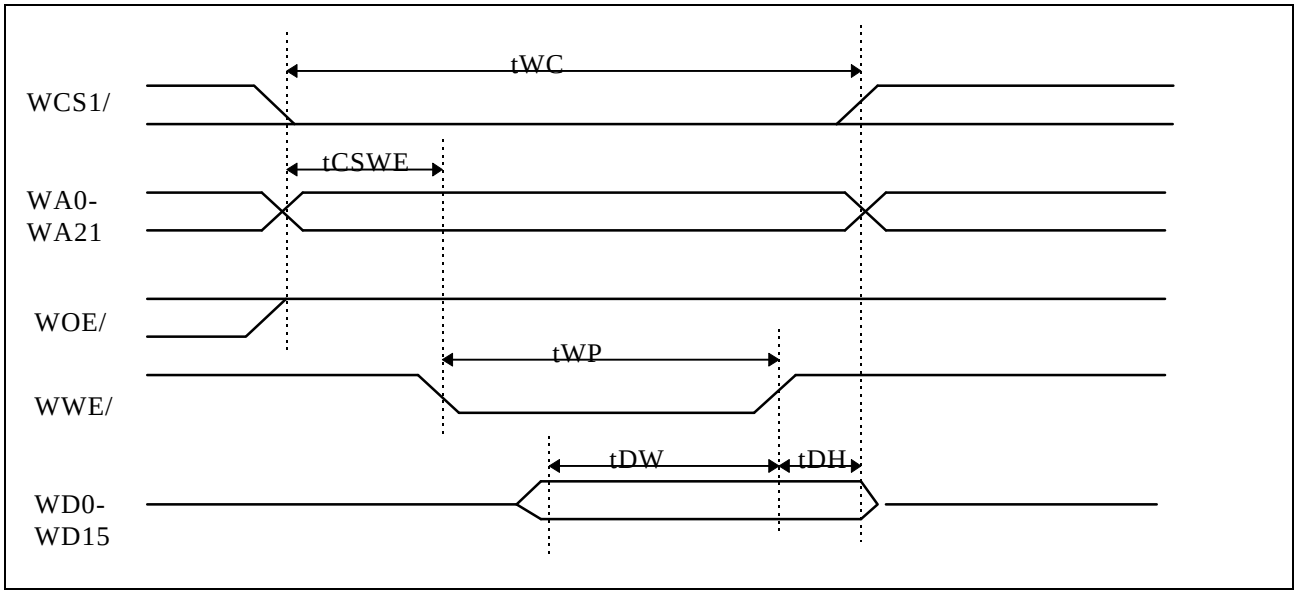
Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	5*tck	-	6*tck	ns
Chip select low / address valid to WOE/ low	tCSOE	2*tck-5	-	3*tck+5	ns
Output enable pulse width	tPOE	-	3*tck	-	ns
Chip select/address access time	tACE	5*tck-5	-	-	ns
Output enable access time	tOE	3*tck-5	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	2*tck-5	ns

7-4- EXTERNAL RAM TIMING

16 BIT SRAM READ CYCLE

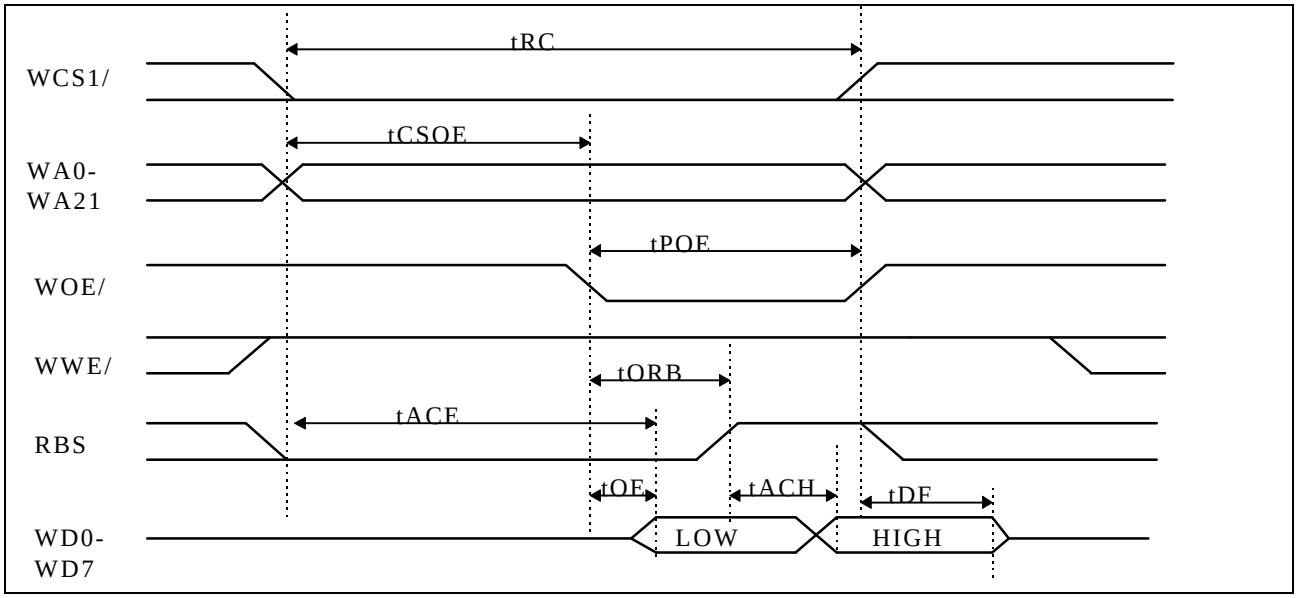


16 BIT SRAM WRITE CYCLE

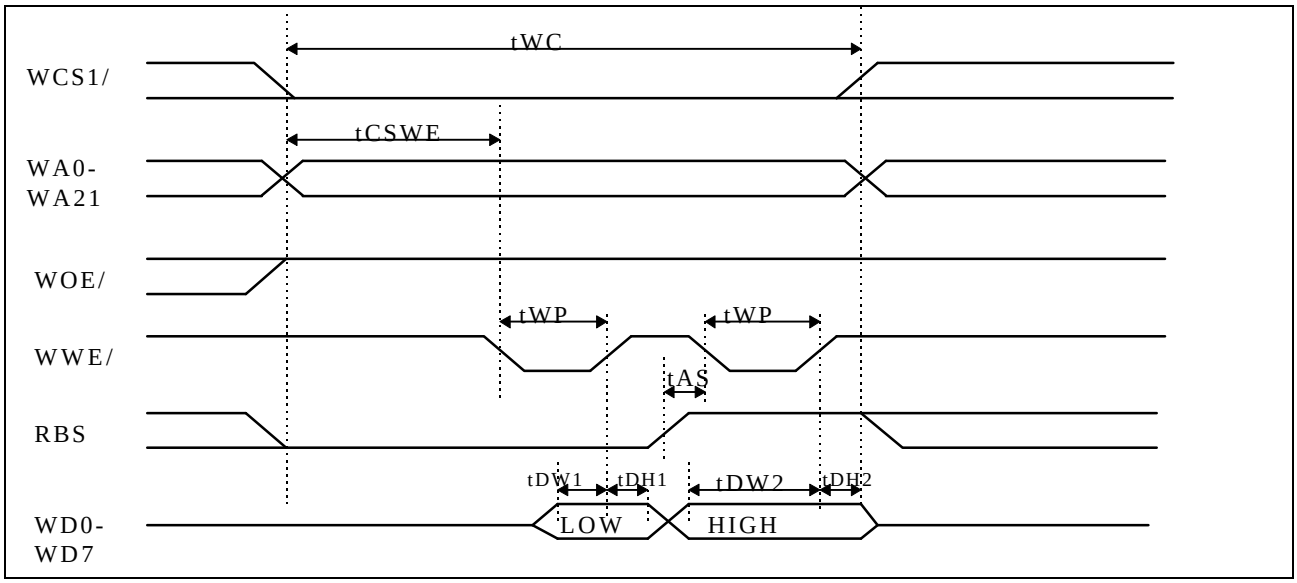


Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	5*tck	-	6*tck	ns
Chip select low / address valid to WOE/ low	tCSOE	2*tck-5	-	3*tck+5	ns
Output enable pulse width	tPOE	-	3*tck	-	ns
Chip select/address access time	tACE	5*tck-5	-	-	ns
Output enable access time	tOE	3*tck-5	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	2*tck-5	ns
Write cycle time	tWC	5*tck	-	6*tck	ns
Write enable low from CS/ or Address or WOE/	tCSWE	2*tck-10	-	-	ns
Write pulse width	tWP	-	4*tck	-	ns
Data out setup time	tDW	4*tck-10	-	-	ns
Data out hold time	tDH	10	-	-	ns

8 BIT SRAM READ CYCLE

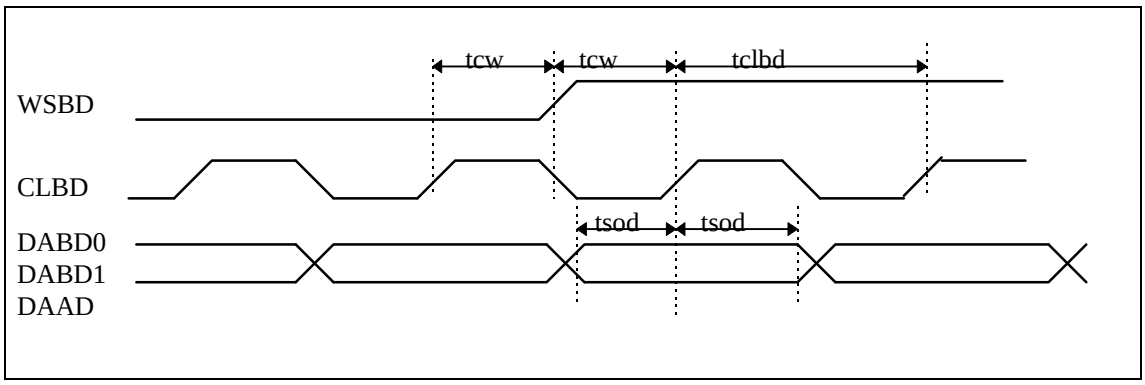


8 BIT SRAM WRITE CYCLE



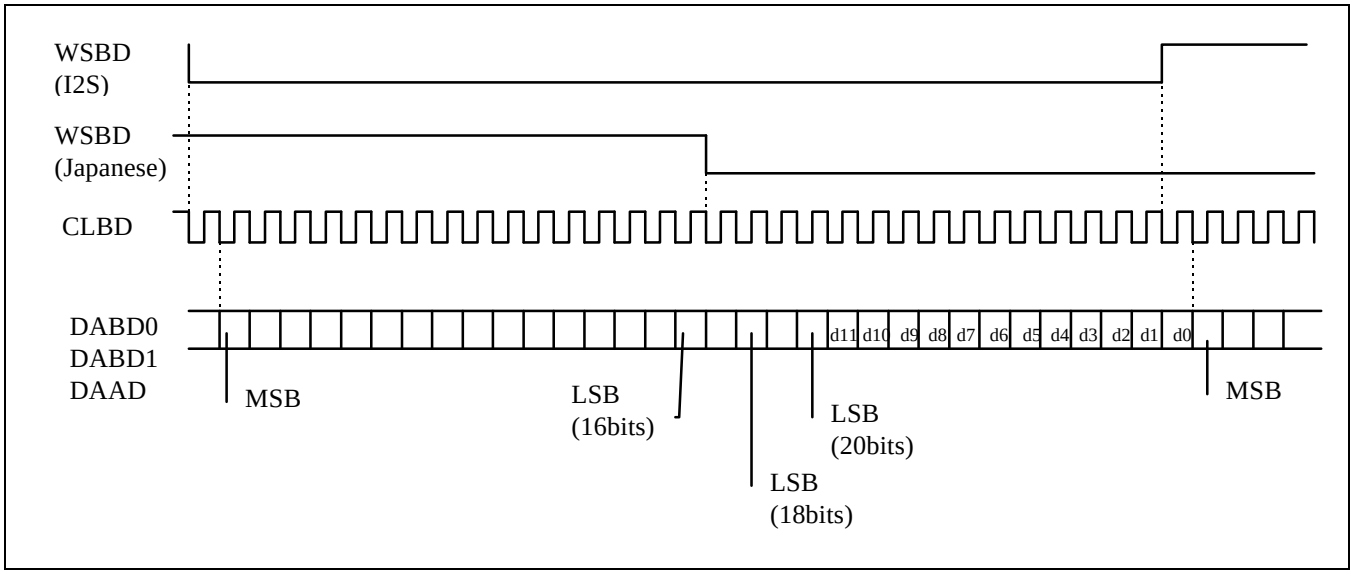
Parameter	Symbol	Min	Typ	Max	Unit
Word (2xbytes) read cycle time	tRC	5*tck	-	6*tck	ns
Chip select low / address valid to WOE/ low	tCSOE	2*tck-5	-	3*tck+5	ns
Output enable pulse width	tPOE	-	3*tck	-	ns
Chip select / address low byte access time	tACE	3*tck-5	-	-	ns
Output enable low byte access time	tOE	tck-5	-	-	ns
Output enable low to byte select high	tORB	-	tck	-	ns
Byte select high byte access time	tACH	2*tck-5	-	-	ns
Chip select or WOE/ high to input data Hi-Z	tDF	0	-	2*tck-5	ns
Word (2xbytes) write cycle time	tWC	5*tck	-	6*tck	ns
1st WWE/ low from CS/ or Address or WOE/	tCSWE	2*tck-10	-	-	ns
Write (low & high byte) pulse width	tWP	1.5*tck-5	-	-	ns
Data out low byte setup time	tDW1	1.5*tck-10	-	-	ns
Data out low byte hold time	tDH1	0.5*tck+10	-	-	ns
RBS high to second write pulse	tAS	0.5*tck-5	-	-	ns
Data out high byte setup time	tDW2	2*tck-10	-	-	ns
Data out high byte hold time	tDH2	10	-	-	ns

7-5- DIGITAL AUDIO TIMING



Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	8*tck-10	-	-	ns
DABD valid prior/after CLBD rising	tsod	8*tck-10	-	-	ns
CLBD cycle time	tclbd	-	16*tck	-	ns

DIGITAL AUDIO FRAME FORMAT



Notes :
- Selection between I2S and Japanese format is a firmware option
- DAAD is 16 bits only
- When connected with codecs like CS4216 or CS4218, d0-d11 can be used to hold independent auxiliary information on left and right words. Refer to corresponding Codec data sheets for details

8- RESET AND POWER DOWN

During power-up, the RESET/ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20ms. The RESET/ signal is normally derived from the main board or PC master reset. However a typical RC/diode power-up network can also be used for some applications.
After the low to high transition of RESET/, following happens :

- The Synthesis/DSP enters an idle state.
- The RUN output is set to zero.
- P16 program execution starts from address 0100H in ROM space (WCS0/ low).

If PDWN/ is asserted low, then all I/Os and outputs will be floated, the crystal oscillator and PLL will be stopped. The chip enters a deep power down sleep mode. To exit power down, PDWN/ has to be asserted high, then RESET/ applied.

9- RECOMMENDED BOARD LAYOUT

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations :

- GND, VCC, VC3 distribution, decouplings

All GND, VCC, VC3 pins should be connected. GND, VCC, VC3 planes are strongly recommended below the SAM9733. The board GND + VCC distribution should be in grid form.
If 3.3V is not available, then VC3 can be connected to VCC through 2*1N4148 diodes in series. This provides a minimum 1.4V voltage drop which allows VC3 to be within specifications.

Recommended decoupling is 0.1µF at each corner of the IC with an additional 10µFT decoupling close to the crystal. VC3 requires a single 0.1uF decoupling.

- Crystal, LFT

The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the SAM9733 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from SAM9733.

- Busses

Parallel layout from D0-D7 and WA0-WA21/WD0-WD15 should be avoided. The D0-D7 bus is an asynchronous high transient current type bus. Even on short distances, it can induce pulses on WA0-WA21/WD0-WD15 which can corrupt address and/or data on these busses.

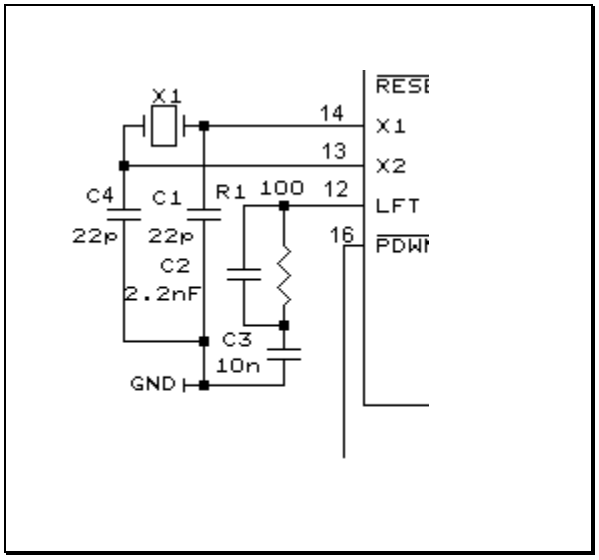
A ground plane should be implemented below the D0-D7 bus, which connects both to the PC-ISA connector and to the SAM9733 GND.

A ground plane should be implemented below the WA0-WA21/WD0-WD15 bus, which connects both to the ROM/SRAM grounds and to the SAM9733.

- Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the Codec vendor recommended layout for correct implementation of the analog section.

10 - RECOMMENDED CRYSTAL COMPENSATION AND LFT FILTER



Note : the X2 output cannot be used to drive another circuit.

Atmel Dream Sales Contacts

Europe **France head office :**
Tel : +33 380 96 62 07
Fax : +33 380 97 27 58
German office :
Tel : +49 7632 62 65
Fax : +49 7632 63 68

USA
Tel : +1 408 451 4876
Fax : +1 408 451 4804

Hong Kong
Tel : +852 2721 9778
Fax : +852 2723 0651

Japan
Tel : +81 3 3523 3551
Fax : +81 3 3523 7581

Korea
Tel : +82 2 277 89 05
Fax : +82 2 272 58 30

Singapore
Tel : +65 299 9212
Fax: +65 291 0955

Taiwan
Tel : +886 2 2600 8666
Fax : +886 2 2600 8186

Original issue : March 1998