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The known Revisions

So far, the following revisions are known: **1.2**, **3.1**, **5.1**. All revisions of the M537 can use the same Bios. The Rev. 5.1 is nearly identical to the M537DMA (which starts at Rev. 5.2!). The differences are the chipset and the missing JP3D. The picture above does show an early rev (1.2 or 3.1) with a linear voltage regulator (see the two big heatsinks beside the CPU). The 5.1 has a switching voltage regulator.

Mouse Port confusion

As you can see on the picture just beside the keyboard connector, at least some board revisions have a 2x4 pin PS/2 header (my Rev. 5.1 has, the picture shows an earlier Rev. which has it also).

The manual describes a 1x6 pin header, which is simply useless here.

You will find a description of the mouse port here. This works great on my Rev. 5.1.

USB Port confusion

Although you'll find a USB-Header on the board, the USB is not working.

Why? Simply the specs for USB changed dramatically from pre-relase to final. This was too late for some chipsets/boards already in production. All major boardand chipset-manufacturers had to deal with this problem, so this is not a PCChips problem. The USB-Port on all affected boards is permanently disabled via the BIOS.

The M537 is such a board, so if you need USB, you will have to buy a USB-PCI card.

I recently discovered, that my board has a 586A (Rev. 0x2h) Southbridge installed. Windows 98 incorrectly displayed a 586B (which is Rev. 0x3h or 0x4h). This chip should have a working USB-part. Unfortunately I was unable to modify the Bios to get it working.

Memory upgrade confusion

The VP-1 chipset can only handle 16MBit technology. Memory modules based on the later 64MBit technology will only be recognized at a quarter of their capacity. So you are limited to modules which have



The 64 MByte modules are rare, expensive, big and may cause troubles.

Cache confusion

During the tests of this board, I discovered, that my board doesn't have a working cache.

The Bios Message about size and state of the External Cache is useless.

Use a test program like ctcm to examine your board.

The latest Beta-Version does offer an Option "Sustained 3T Write". This options toggles the cache strategy from Write Back to Write Trough. This may double the cacheable area of your board to 128 MB. As I don't have working cache, I can't test it, but this is the common behavior of VIA-Chipsets.

Tuning your M537

As I only have the Rev. 5.1 my tips are restricted to this Revision only!

Transfer the tips to other revisions with great care.

First take a look at the Unofficial Homepage for the PCChips M537DMA33.

The modifications for adding the BF2 jumper and modifying the power plane should work for the M537 too.

NOTE: Due to lack of time, I haven't tested this yet, but I will

The switching power supply of my M537 V5.1 is capable of feeding a VIA/Cyrix MII with 2.9V core. Take care for a high quality fan/heatsink combo and use thermal grease. This is most probably the fastest CPU you can put into this board, without hardware modifications.

Note on major difference between the M537DMA and the M537. The M537DMA can handle setups >66 MHz **without** overclocking the PCI-Bus, as soon as the JP3D is available and set correct. The M537 simply can't, so using speeds above 66MHz may cause some wierd behaviour and data loss/corruption. You have been warned.

Anyway before you ask:

| Bus Speeds | | | | |
|------------|-------|-------|-----|--|
| JP3 A | ЈРЗ В | ЈРЗ С | MHz | |
| 2-3 | 2-3 | 2-3 | 50 | |
| 1-2 | 2-3 | 2-3 | 55 | |
| 2-3 | 2-3 | 1-2 | 60 | |
| 2-3 | 1-2 | 2-3 | 66 | |
| 1-2 | 2-3 | 1-2 | 75 | |

| 1-2 | 1-2 | 2-3 | 83 | |
|------------------------------|-----|-----|-----|--|
| 2-3 | 1-2 | 1-2 | N/A | |
| 1-2 | 1-2 | 1-2 | N/A | |
| Thanks to AJZ for this table | | | | |

If you have questions, contact me

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