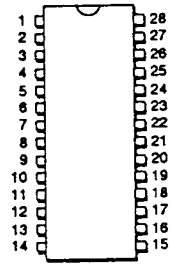
SIERRA SEMICONDUCTOR

SC11482/SC11483/SC11484
Universal HiCOLOR™ Palette

FEATURES

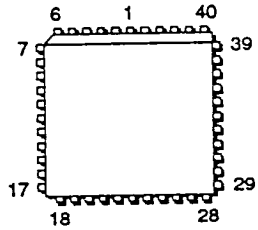
- ☐ Supports 5-5-5 TARGA™ format (32,768 colors) in HiCOLOR mode
- ☐ Supports Pseudo Color format (256 colors)
- ☐ Anti-aliasing capability
- ☐ Maintains color integrity when multiple windows are displayed
- ☐ Up to 100 MHz Pipelined Operation
- ☐ Triple 6-bit or 8-bit D/A Converters
- ☐ Analog Output Comparators
- ☐ On-chip Voltage Reference
- ☐ Anti-Sparkle Circuitry
- ☐ 15 Overlay Registers (SC11482/SC11484)
- ☐ 256 x 24 Color Lookup Table
- ☐ RS-343A/RS-170 Compatible Outputs
- ☐ Standard MPU Interface
- ☐ Sync on all Three Channels (SC11482/SC11484)
- ☐ Programmable Pedestal (SC11482/SC11484)
- ☐ +5V CMOS Monolithic (EPI) Construction
- ☐ Available Clock Rates for Pseudo Color
  - 80 MHz • 50 MHz
  - 66 MHz
- ☐ Pin compatible and software compatible with the SC11471, SC11476, SC11478, SC11481, SC11486 and SC11488.
- ☐ Power on reset for the command register.

28-PIN DIP PACKAGE



SC11483CN

44-PIN PLCC PACKAGE



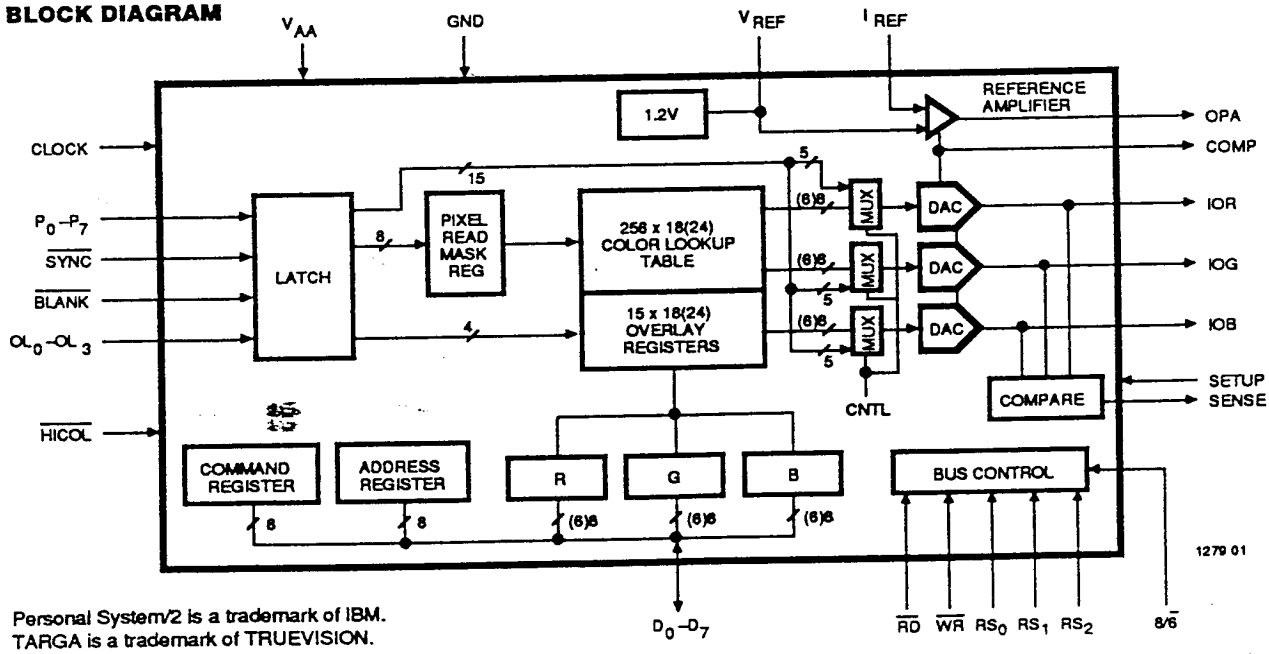
SC11482CV
SC11483CV
SC11484CV

GENERAL DESCRIPTION

The SC11482/SC11483/SC11484 is a family of 16-bit HiCOLOR palettes that support the popular TARGA format which uses 5 bits/primary color and 8 bit pseudo (256 colors) color mode. The total colors available using the TARGA format are 32,768. The SC11482/SC11483/SC11484 palette offers the capability of the expensive TARGA board and provides access to the wide variety of software packages (once dedicated to TARGA boards only) to the low cost VGA market.

The SC11482/SC11483/SC11484 also provides the ability to maintain color integrity in PC-windowing applications, when more than one application or window is displayed with different images simultaneously. Also supported is anti-aliasing capability—a technique which can significantly improve the

BLOCK DIAGRAM



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TARGA is a trademark of TRUEVISION.

graphics quality by smoothing jagged edges. This technique requires a great number of different colors and can be easily implemented with the large number of colors offered by HiCOLOR palettes.

These three products are pin and function compatible with the Sierra SC11481/SC11486/SC11488 HiCOLOR palettes, the Sierra SC11471/SC11476/SC11478 pseudo color (8 bit, 256 color) palettes and the Brooktree BT471/BT476/BT478 palettes.

The top-of-the-line product in this family is the SC11484 which offers three 8-bit D/A converters, 256 x 24 color lookup table, and 15 overlay registers. It may be converted for either 6 bits or 8 bits per color operation in the 256 color mode. The SC11482 is the same as the SC11484 except that it offers three 6-bit D/A converters instead of 8-bit, a 256 x 18 lookup table and 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Sync generation on all three channels, a programmable pedestal (0 or 7.5 IRE), and use of either an external voltage or current reference is also supported.

The SC11483 is similar to the SC11482, but has no overlays or sync information on the analog outputs.

On-chip analog comparators are included to simplify diagnostics and debugging, with the resulting output onto the SENSE pin. Also included is an on-chip voltage reference to simplify using the device.

When the HiCOLOR mode is not activated, the SC11482/483/484 behaves exactly as a SC11471/476/478 with anti-sparkle capabilities, on-chip voltage/current reference, and analog comparators.

The SC11482/483/484 generate RS-343A compatible red, green, and blue video signals, are capable of driving doubly-terminated 75Ω coax directly, and generate RS-170 compatible video signals into a singly-terminated 75Ω load, without requiring external buffering.

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER			DESCRIPTION
	SC11482 SC11484	SC11483		
	P_1	P_1	P_2	
8/$\overline{6}$	2*			8-bit/$\overline{6}$-bit select input (TTL compatible). This bit specifies whether the MPU is reading and writing 8-bits (logical one) or 6-bits (logical zero) of color information each cycle. For 8-bit operation, D_7 is the most significant data bit during color read/write cycles. For 6-bit operation, D_5 is the most significant bit during color read/write cycles (D_6 and D_7 are ignored during color write cycles and logical zero during color read cycles). This bit is implemented only on the SC11484.
$\overline{BLANK}$	7	16	7	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 5 and 6. It is latched on the rising edge of CLOCK. When $\overline{BLANK}$ is a logical zero, the pixel and overlay inputs are ignored.
CLOCK	40	13	40	Clock input (TTL compatible). The rising edge of CLOCK latches the P_0–P_7, OL_0–OL_3, $\overline{SYNC}$, and $\overline{BLANK}$ inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
COMP	29		29	Compensation pin. If an external voltage reference is used (Figure 3), this pin should be connected to OPA. If an external current reference is used (Figure 4), this pin should be connected to I_{REF}. A 0.1 µF ceramic capacitor must always be used to bypass this pin to V_{AA}. The COMP capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum.
D_0–D_7	8–15	17–24	8–15	Data bus (TTL compatible). Data is transferred into and out of the device over this eight bit bidirectional data bus. D_0 is the least significant bit.
GND	3, 24	14	3, 24	Analog ground. All GND pins must be connected.
$\overline{HICOL}$	20		20	HiCOLOR Mode select input (TTL compatible). This signal is inverted and logical ORed with D_7 of the command register for compatibility with the SC11481/486/488. A logic zero will enable the HiCOLOR mode (either the HiCOLOR mode 1 or the HiCOLOR mode 2) selected by the D_5 bit of the command register. See Table 2 for details. The $\overline{HICOL}$ pin should be tied to V_{AA} to disable hardware selection of the HiCOLOR mode.
IOR, IOG, IOB	25–27	1–3	25–27	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75 Ω coaxial cable.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER			DESCRIPTION
	SC11482 SC11484	SC11483		
	P_1	P_1	P_2	
I_{REF}	28	4	28	Full scale adjust control. Note that the IRE relationships in Figures 1 and 2 are maintained, regardless of the full scale output current. When using an external voltage reference (Figure 3), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is: RSET (Ω) = K • 1000 • V_{REF} (V)/I_{OUT} (mA) K is defined in the table below for doubly-terminated 75 Ω loads. When using an external current reference (Figures 4 and 5) the relationship between I_{REF} and the full scale output current on each output is: I_{REF} (mA) = I_{OUT} (mA)/K
N/C			2,5,19 23,41-44	Not Connected
OL_0–OL_3	41–44			Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 4. When accessing the overlay register, the P_0–P_7 inputs are ignored. They are latched on the rising edge of CLOCK. OL_0 is the LSB. Unused inputs should be connected to GND.
OPA	30		30	Reference amplifier output. If an external or the internal voltage reference is used (Figure 3), this pin must be connected to COMP. When using an external current reference (Figure 4), this pin should be left floating.
P_0–P_7	32–39	5–12	32–39	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color lookup table is to be used to provide color information. They are latched on the rising edge of CLOCK in Pseudo-color mode and HiCOLOR mode 2. They will be latched on both the rising and falling edges of CLOCK in the HiCOLOR mode 1. P_0 is the LSB. Unused inputs should be connected to GND.
$\overline{RD}$	6	15	6	Read control input (TTL compatible). To read data from the device, $\overline{RD}$ must be a logical zero. RS_0–RS_2 are latched on the falling edge of $\overline{RD}$ during MPU read operations.
RS_0–RS_2	17–19	26, 27†	17, 18†	Register select inputs (TTL compatible). RS_0–RS_2 specify the type of read or write operation being performed, as illustrated in Tables 2 and 3.
SENSE	1		1	Sense output (TTL compatible). SENSE is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). Note that SENSE may not be stable while SYNC is toggling.
SETUP	23			Setup control input. Used to specify either a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal.
$\overline{SYNC}$	5			Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1 and 2). $\overline{SYNC}$ does not override any other control or data input, as shown in Tables 5 and 6; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.

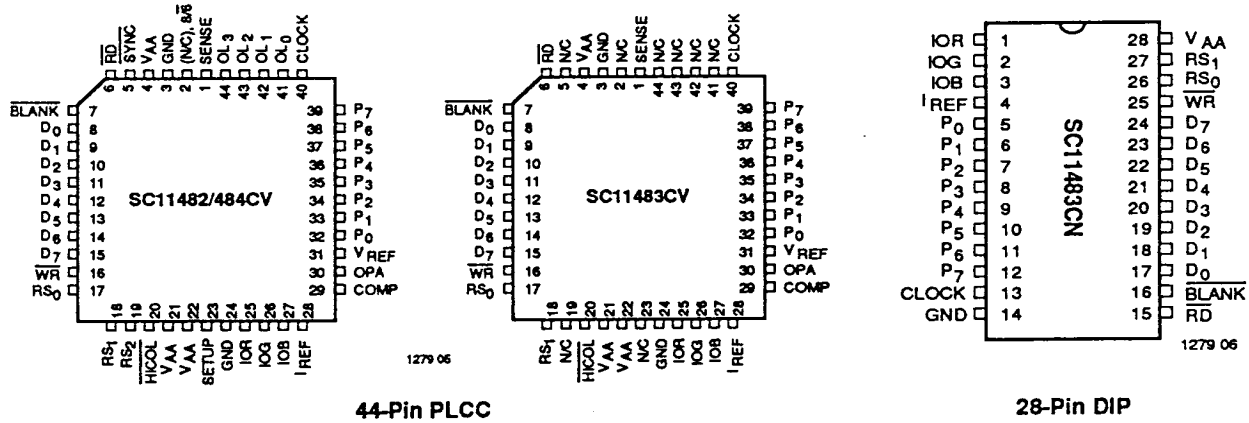
Part Number	Mode	Pedestal	K
SC11484	6-bit	7.5 IRE	3.170
	8-bit	7.5 IRE	3.195
	6-bit	0.0 IRE	3.000
	8-bit	0.0 IRE	3.025
SC11482	6-bit	7.5 IRE	3.170
		0.0 IRE	3.000
SC11483	6-bit	0.0 IRE	2.100

NOTE: P_1 is the 44 pin PLCC package, P_2 is the 28 pin DIP package. †RS_2 is not available on the SC11483. *8/$\overline{6}$ is only available on the SC11484.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER			DESCRIPTION
	SC11482 SC11484	SC11483		
	P_1	P_1	P_2	
V_{AA}	4,21,22	28	4, 21, 22	Analog power. All V_{AA} pins must be connected.
V_{REF}	31		31	Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 4), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must be used to decouple this input to V_{AA}, as shown in Figures 3 and 4. The decoupling capacitor must be as close to the device as possible to keep the lead lengths to an absolute minimum. When using internal reference this pin should not drive any external circuitry except for the decoupling capacitor.
$\overline{WR}$	16	25		Write control input (TTL compatible). D_0–D_7 data is latched on the rising edge of $\overline{WR}$, and RS_0–RS_2 are latched on the falling edge of $\overline{WR}$ during MPU write operations.

CONNECTION DIAGRAMS



44-Pin PLCC

28-Pin DIP

NOTE: N/C pins may be left unconnected without affecting the performance of the SC11482/483/484. Names in parentheses are pin names for SC11482.

FUNCTIONAL DESCRIPTION

MPU Interface

As illustrated in the functional block diagram, the SC11482/483/484 supports a standard MPU bus interface, allowing the MPU direct access to the color lookup table and overlay registers.

The RS_0–RS_2 select inputs specify whether the MPU is accessing the address register, color lookup table, overlay registers, command registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color lookup table and overlay registers, eliminating the requirement for external address multiplexers.

RS_2	RS_1	RS_0	Addressed by MPU
0	0	0	Address register (RAM write mode)
0	1	1	Address register (RAM read mode)
0	0	1	Color lookup table
0	1	0	Pixel read mask register
1	0	0	Address register (overlay write mode)
1	1	1	Address register (overlay read mode)
1	0	1	Overlay registers
1	1	0	Command Register

Table 1. Control Input Truth Table

Writing Color Lookup Table and Overlay Color Data

To write color data, the MPU writes the address register (selecting RAM write or overlay write mode) with the address of either the color lookup table location or the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS_0–RS_2 to select either the color lookup table or the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the SC11482/483) and written to the location specified by the address register. The address register then increments to the next location which MPU may modify by simply writing another sequence of red, green and blue data. A block of color values in consecutive locations

may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Color Lookup Table and Overlay Color Data

To read color data, the MPU loads the address register (selecting lookup table or overlay read mode) with the address of the color lookup table location or overlay register to be read. The contents of the color lookup table at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS_0–RS_2 to select either the color lookup table or overlay registers. Following the blue read cycle, the contents of the lookup table or the contents of the overlay location specified by the address register are copied into the R, G, B registers and the address register gets incremented again. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color lookup table, the address register resets to $00 following a blue read or write cycle to RAM location $FF. When accessing the overlay registers, the address register increments following a blue read or write cycle. However, while accessing the overlay registers, the four most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color lookup table/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses.

To reduce noticeable sparkling on the CRT screen during MPU access to the color lookup table or the overlay registers, an internal anti-sparkle logic is implemented to maintain the previous output color data on the three D/A Converters output while the transfer between the color look-up table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 3. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other eight bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color lookup table locations and overlay registers, as shown in Table 3. ADDR0 is the LSB when the MPU is accessing the RAM or overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

SC11482/483 Data Bus Interface

Color data is contained on the lower six bits of the data bus, with D_0 being the LSB and D_5 the MSB of color data. When writing color data, D_6 and D_7 are ignored. During color read cycles, D_6 and D_7 will be a logical zero.

SC11484 Data Bus Interface

On the SC11484, the $8/\overline{6}$ control input is used to specify whether the MPU is reading and writing 8-bits ($8/\overline{6}$ = logical one) or 6-bits ($8/\overline{6}$ = logical zero) of color information each cycle.

For 8-bit operation, D_0 is the LSB and D_7 is the MSB of color data.

For 6-bit operation (and also when using the SC11482/483), color data is contained on the lower six bits of the data bus, with D_0 being the LSB and D_5 the MSB of color data. When writing color data, D_6 and D_7 are ignored. During color read cycles, D_6 and D_7 will be a logical zero. Note that in the 6-bit mode, the SC11484's full scale output current will be about 1.5% lower than when it is in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being logic zero in the 6-bit mode.

HICOLOR Modes

When a HiCOLOR Mode is activated, the input stage accepts 16 bits of pixel information from the 8 bit pixel select lines, P_0-P_7. The lower 8 bits (B7-B0) are latched on the first edge of the pixel clock, and the upper 8 bits (B15-B8) are latched on the second edge of the pixel clock. The two bytes form a 16 bit pixel word (B15-B0) to directly drive the triple video DACs. The most significant bit of the 16 bit pixel word is ignored. The color lookup table and pixel read mask register are bypassed. The 16 bit pixel word (B15-B0) is assigned to the DACs using the following format:

B15	Ignored
B14 - B10	Red DAC
B9 - B5	Green DAC
B4 - B0	Blue DAC

* Internally the unused LSBs of all DACs are forced to zero in HiCOLOR mode.

HICOLOR Mode 1

In HiCOLOR mode 1 the least significant byte is latched on the rising edge of the pixel clock and the most significant byte is latched on the falling edge of the pixel clock. Therefore only one pixel clock period is needed to load a 16 bit word. See Figure 10.

HICOLOR Mode 2

When HiCOLOR mode 2 is activated the input stage accepts 16 bits of information by using two pixel clock cycles. The least significant byte is latched on the first rising edge of the pixel clock and the most significant byte is latched on the second rising edge of the pixel clock. They are synchronized with the $\overline{\text{BLANK}}$ signal. The first byte latched when $\overline{\text{BLANK}}$ goes high is the least significant byte. Since a pixel word

is latched in two pixel clock cycles the input clock must be twice as fast as the DACs data conversion clock. See Figure 8. The SC11482/483/484 has an internal divider to generate the data conversion clock from the pixel clock.

SENSE Output

SENSE is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This output is used to determine the presence of a CRT monitor and via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 335 mV reference has a ±5% tolerance (when using an external 1.235 V voltage reference). The tolerance is ±10% when using the internal voltage reference or an external current reference. Note that $\overline{SYNC}$ should be logical zero for SENSE to be stable.

Frame Buffer Interface

The P_0–P_7 and OL_0–OL_3 inputs are used to address the color lookup table and overlay registers, as shown in Table 3. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P_0–P_7 inputs. Bit D_0 of the pixel read mask register corresponds to pixel input P_0. The addressed location provides 24 bits (18 bits for the SC11482/483) of color information to the three D/A converters.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 1 and 2. Tables 5 and 6 detail how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = V_{AA}) blanking pedestal is to be used. Note that the SC11483 generates only a 0 IRE blanking pedestal (Figure 2).

The analog outputs of the SC11482/483/484 are capable of directly driving a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

Command Register

This register is active in all modes. It is used to set the operating mode of the device as shown in Table 2. It may be written to or read by the MPU at any time and is initialized to a logical zero after the power on reset.

In the SC11483, where the RS_2 pin is not available, the command register is accessed by using the following special sequence of events:

A flag will be set when the pixel read mask register (RS_1 = 1 & RS_0 = 0) is read four times consecutively. The next write to the pixel mask register will be directed to the command register and can be used to set the command register. A write to any address or a read from any address other than the pixel read mask register will reset the flag. This flag will also get reset after the power on reset.

D_7	D_6	D_5	D_4*	D_3*	D_2*	D_1*	D_0*	Mode
0	0	0	0	0	0	0	0	Pseudo Color (256 color)
1	0	0	0	0	0	0	0	HiCOLOR Mode 1 (32K color)
1	0	1	0	0	0	0	0	HiCOLOR Mode 2 (32K color)

*Reserved by Sierra Semiconductor.

D_7 HiCOLOR Mode Enable. A logic zero enables the Pseudo-color mode. A logic one enables the HiCOLOR modes. (Used with D_5.)

D_6 Reserved. This input must be set to logic zero.

D_5 HiCOLOR Mode Select. When HiCOLOR mode is enabled (D_7 = 1) a logic zero selects the HiCOLOR Mode 1. A logic one selects HiCOLOR mode 2. When HiCOLOR mode is disabled (D_7 = 0) this bit must be set to logic zero.

D_4–D_0 Reserved. These inputs must be set to logic zero.

Table 2. Command Register Modes

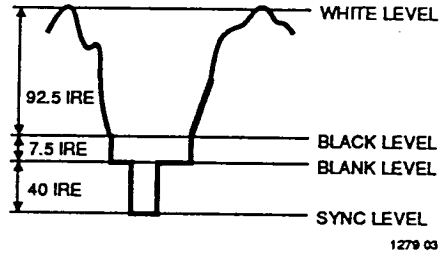
	Value	RS_2	RS_1	RS_0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				Red value Green value Blue value
ADDR0–7 (counts binary)	$00-$FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	Color lookup table Reserved Overlay Color 1 : Overlay Color 15

Table 3. Address Register (ADDR) Operation

OL_0–OL_3	P_0–P_7	Addressed by Frame Buffer
$0	$00	Color lookup table Location $00
$0	$01	Color lookup table Location $01
:	:	:
$0	$FF	Color lookup table Location $FF
$1	$xx	Overlay Color 1
:	$xx	:
$F	$xx	Overlay Color 15

Table 4. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = $FF)

SC11482/484 w/o SYNC		SC11482/484 with SYNC	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



NOTE: 75 Ω doubly-terminated load, SETUP = V_{AA}, V_{REF} = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

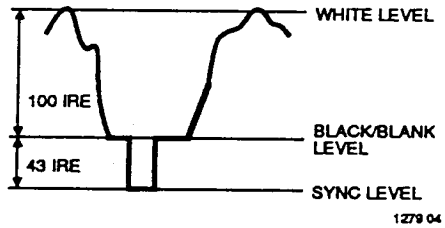
Figure 1. Composite Video Output Waveforms (SETUP = V_{AA})

Description	SC11482/484 I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	Data + 9.05	1	1	Data
DATA–SYNC	Data + 1.44	0	1	Data
BLACK	9.05	1	1	$00
BLACK–SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

NOTE: 75 Ω doubly-terminated load, SETUP = V_{AA}, V_{REF} = 1.235 V, RSET = 147 Ω.

Table 5. Video Output Truth Table (SETUP = V_{AA})

SC11483 or SC11482/484 w/o Sync		SC11482/484 with Sync	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.256
0.00	0.000	0.00	0.000



NOTE: 75 Ω doubly-terminated load, SETUP = GND, V_{REF} = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms (SETUP = GND)

Description	SC11483 I_{OUT} (mA)	SC11482/484 I_{OUT} (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	17.62	26.67	1	1	$FF
DATA	Data	Data + 8.05	1	1	Data
DATA–SYNC	Data	Data	0	1	Data
BLACK	0	8.05	1	1	$00
BLACK–SYNC	0	0	0	1	$00
BLANK	0	8.05	1	0	$xx
SYNC	0	0	0	0	$xx

NOTE: 75 Ω doubly-terminated load, SETUP = V_{AA}, V_{REF} = 1.235 V, RSET = 147 Ω.

Table 6. Video Output Truth Table (SETUP = GND)

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

The layout should be optimized for lowest noise on the SC11482/483/484 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all SC11482/483/484 ground pins, current/voltage reference circuitry, power supply bypass circuitry for the SC11482/483/484, the analog output traces, and all the digital signal traces leading up to the SC11482/483/484.

Power Planes

The SC11482/483/484 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figures 3, 4 and 5. This bead should be located within three inches of the SC11482/483/484.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all SC11482/483/484 power pins and current/voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Best performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of V_{AA} pins to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the SC11482/483/484 contain circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the SC11482/483/484 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the SC11482/483/484 should be avoided to reduce noise pickup.

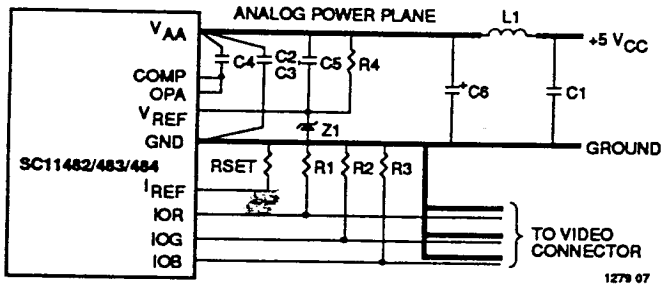
Any active termination resistors for the digital inputs should be connected to the regular PCB power plane, and not the analog power plane.

Analog Signal Interconnect

The SC11482/483/484 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

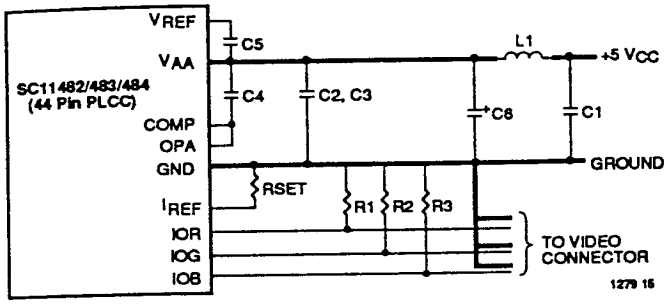
For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to GND. The connection between the current output and GND should be as close as possible to the SC11482/483/484 to minimize reflections.



NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11482/483/484.

LOCATION	DESCRIPTION
C1–C5	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C6	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
L1	Ferrite Bead (Fair-Rite 2743001111)
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)
RSET	1% Metal Film Resistor (Dale CMF-55C)
Z1	1.2 V Voltage Reference (National Semiconductor LM385BZ-1.2)
R4	1K Ω 5% Resistor

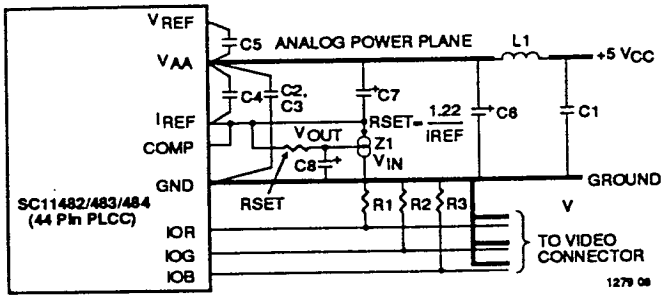
Figure 3. Typical Connection Diagram and Parts List (External Voltage Reference)



LOCATION	DESCRIPTION
C1–C5	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C6	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
L1	Ferrite Bead (Fair-Rite 2743001111)
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)
RSET	1% Metal Film Resistor (Dale CMF-55C)

NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11482/483/484.

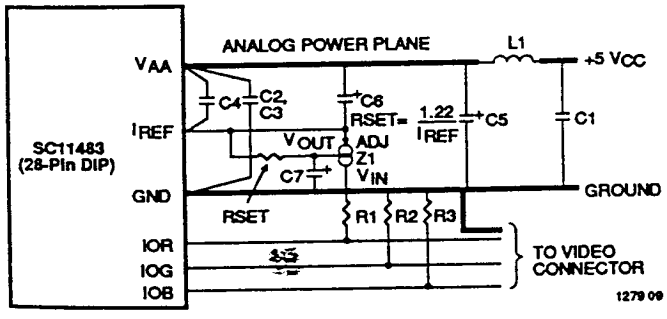
Figure 3.5. Typical Connection Diagram and Parts List (Internal Voltage Reference)



LOCATION	DESCRIPTION
C1–C5	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C6	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
C7	47 µF Tantalum Capacitor (Mallory CSR13F476KM)
C8	1 µF Capacitor (Mallory CSR13G105KM)
RSET	1% Metal Film Resistor (Dale CMF-55C)
L1	Ferrite Bead (Fair-Rite 2743001111)
Z1	Adjustable Regulator (National Semiconductor LM337LZ)
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)

NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11482/483/484.

Figure 4. Typical Connection Diagram and Parts List (External Current Reference)



LOCATION	DESCRIPTION
C1–C4	0.1 µF Ceramic Capacitor (Erie RPE112Z5U104M50V)
C5	10 µF Tantalum Capacitor (Mallory CSR13G106KM)
C6	47 µF Tantalum Capacitor (Mallory CSR13F476KM)
C7	1 µF Capacitor (Mallory CSR13G105KM)
L1	Ferrite Bead (Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% Metal Film Resistor (Dale CMF-55C)
Z1	Adjustable Regulator (National Semiconductor LM337LZ)
RSET	1% Metal Film Resistor (Dale CMF-55C)

NOTE: The vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SC11483.

Figure 5. Typical Connection Diagram and Parts List (External Current Reference)

ABSOLUTE MAXIMUM RATINGS

V_{AA} (measured to GND)	+7.0 V
Voltage on Any Digital Pin	– 0.5 V to V_{AA} + 0.5 V
Analog Output Short Circuit Duration to any Power Supply or Common (ISC)	Indefinite
Ambient Operating Temperature (TA)	–55 to +125°C
Storage Temperature (TS)	–65 to +150°C
Junction Temperature (TJ)	+150°C
Vapor Phase Soldering (2 minutes) TVSOL	TBD

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNITS
Power Supply (V_{AA})				
80, 66 MHz PRVTS	+4.75	5.0	5.25	V
50 MHz PRVTS	+4.5	5.0	5.5	V
Ambient Operating Temperature (TA)	0	25	70	°C
Output Load (RL)		37.5		Ω
Voltage Reference (V_{REF})	+1.14	1.235	1.26	V
Current Reference (I_{REF})				
Standard RS-343A	–3	–8.39	–10	mA
PS/2 Compatible	–3	–8.88	–10	mA

DC ELECTRICAL CHARACTERISTICS

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Resolution (each DAC)					
SC11484		8	8	8	Bits
SC11482/483		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	I_L				
SC11484				±1	LSB
SC11483				±1/2	LSB
SC11482				±1/4	LSB
Differential Linearity Error	D_L				
SC11484				±1	LSB
SC11483				±1/2	LSB
SC11482				±1/4	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	V_{IH}	2.0		V_{AA} + 0.5	V
Input Low Voltage	V_{IL}	GND – 0.5		0.8	V
Input High Current (V_{IN} = 2.4 V)	I_{IH}			1	µA
Input Low Current (V_{IN} = 0.4 V)	I_{IL}			–1	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}			7	pF

DC ELECTRICAL CHARACTERISTICS (continued)

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Digital Outputs					
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}			0.4	V
3-State Current	I_{OZ}			50	µA
Output Capacitance	CD_{OUT}			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SC11482/484					
SETUP = V_{AA}		0.95	1.44	1.90	mA
SETUP = GND		0	5	50	µA
SC11483		0	0	0	µA
Blank Level					
SC11482/484		6.29	7.62	8.96	mA
SC11483		0	5	50	µA
Sync Level (SC11482/484 only)		0	5	50	µA
LSB Size					
SC11484 (8/$\overline{6}$ = Logical One)			69.1		µA
SC11482/483			279.68		µA
DAC to DAC Matching			2	5	%
Output Compliance	V_{OC}	–1.0		+1.5	V
Output Impedence	RA_{OUT}		10		kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}			30	pF
Voltage Reference Input Current	IV_{REF}		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / %ΔV_{AA}

NOTE: Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, 8/$\overline{6}$ = Logical one. For 28-pin DIP version of the SC11483, I_{REF} = –8.39 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

* Since the SC11482/483 have 6-bit DACs (and the SC11484 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

ANALOG OUTPUT LEVELS—PS/2 COMPATIBILITY

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SC11482/484					
SETUP = V_{AA}		1.01	1.51	2.0	mA
SETUP = GND		0	5	50	µA
SC11483		0	5	50	µA
Blank Level					
SC11482/484		6.6	8	9.4	mA
SC11483		0	5	50	µA
Sync Level (SC11482/484 only)		0	5	50	µA

NOTE: Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, 8/$\overline{6}$ = Logical one. For 28-pin DIP version of the SC11483, I_{REF} = 8.88 mA.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	80 MHz Devices MIN	80 MHz Devices TYP	80 MHz Devices MAX	66 MHz Devices MIN	66 MHz Devices TYP	66 MHz Devices MAX	50 MHz Devices MIN	50 MHz Devices TYP	50 MHz Devices MAX	UNITS
Clock Rate Pseudo Color	F_{MAX}			80			66			50	MHz
Clock Rate HiCOLOR Mode 1	F_{MAX}			50			50			45	MHz
Clock Rate HiCOLOR Mode 2	F_{MAX}			100			100			90	MHz
RS_0–RS_2 Setup Time	1	10			10			10			ns
RS_0–RS_2 Hold Time	2	10			10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40			40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5			20			20			20	ns
Read Data Hold Time	6	5			5			5			ns
Write Data Setup	7	10			10			10			ns
Write Data Hold Time	8	10			10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	4•P13			4•P13			4•P13			ns
Pixel and Control Setup Time	11	3			3			3			ns
Pixel and Control Hold Time (Pseudo Color and HiCOLOR Mode 2)	12	3			3			3			ns
Pixel and Control Setup Time LSB HiCOLOR Mode 1	20	-1.0			-1.0			-1.0			ns
Pixel and Control Hold Time LSB HiCOLOR Mode 1	21	7.0			7.0			7.0			ns
Pixel and Control Setup Time MSB HiCOLOR Mode 1	22	-1.0			-1.0			-1.0			ns
Pixel and Control Hold Time MSB HiCOLOR Mode 1	23	7.0			7.0			7.0			ns
Clock Cycle Time	13	12.5			15.5			20			ns
Clock Pulse Width High Time	14	4			5			6			ns
Clock Pulse Width Low Time	15	4			5			6			ns
Clock Cycle Time (HiCOLOR Mode 1)	13	25			25			28			ns
Clock Pulse Width High Time HiCOLOR Mode 1	14	9			9			9			ns
Clock Pulse Width Low Time HiCOLOR Mode 1	15	9			9			9			ns
Analog Output Delay	16			30			30			30	ns
Analog Output Rise/Fall Time	17		3			3			3		ns
Analog Output Settling Time*	18		13			15			20		ns
Clock and Data Feedthrough*			-30			-30			-30		dB
Glitch Impulse*			75			75			75		pV–sec
DAC to DAC Crosstalk			-23			-23			-23		dB
Analog Output Skew				2			2			2	ns
SENSE Output Delay	19		1			1			1		µs
Pipeline Delay (Pseudo Color and HiCOLOR Mode 1)		4	4	4	4	4	4	4	4	4	Clocks
Pipeline Delay (HiCOLOR Mode 2)		8	8	8	8	8	8	8	8	8	Clocks
V_{AA} Supply Current**	I_{AA}		180	220		180	220		180	220	mA

TEST CONDITIONS: "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = V_{AA}, $8/\overline{6}$ = Logical one. For 28-pin DIP version of SC11483, I_{REF} = -8.39 mA. TTL input values are 0 to 3 V, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D_0–D7 output load ≤ 50 pF. See timing notes in Figures 6 and 7.

* Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1k Ω resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

** At F_{MAX}. I_{AA} (typ) at V_{AA} = 5.0 V. I_{AA} (max) at V_{AA} = 5.25 V.

TIMING WAVEFORMS

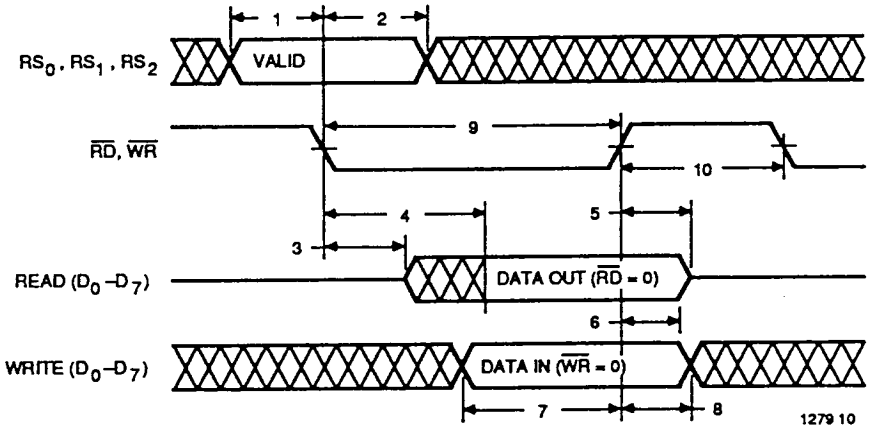


Figure 6. MPU Read/Write Timing

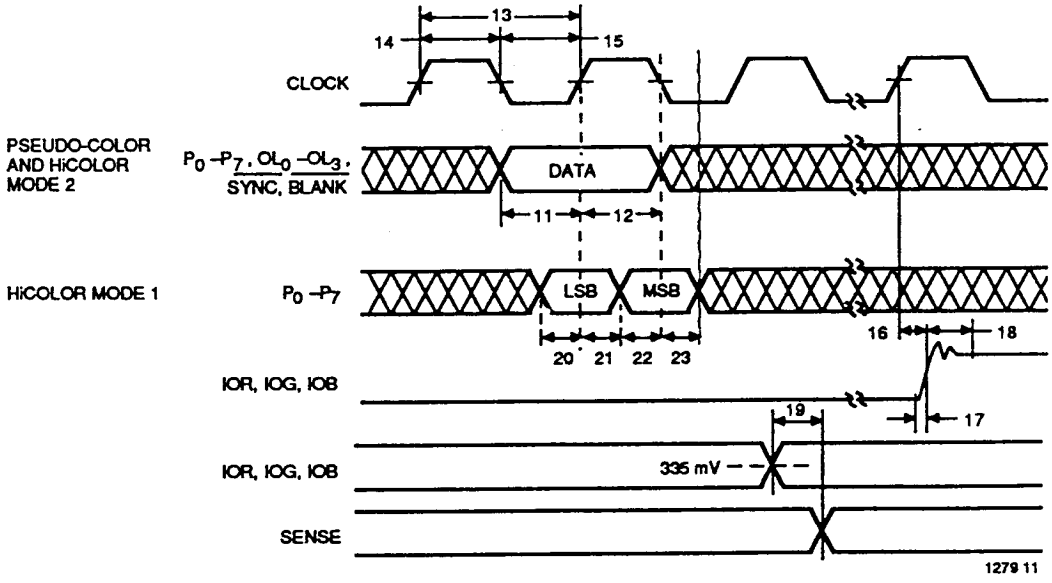


Figure 7. Video Input/Output Timing

NOTE 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

NOTE 2: Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 LSB. (SC11484), ± 1/4 LSB (SC11482), or ± 1/2 LSB (SC11483).

NOTE 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

TIMING WAVEFORMS (continued)

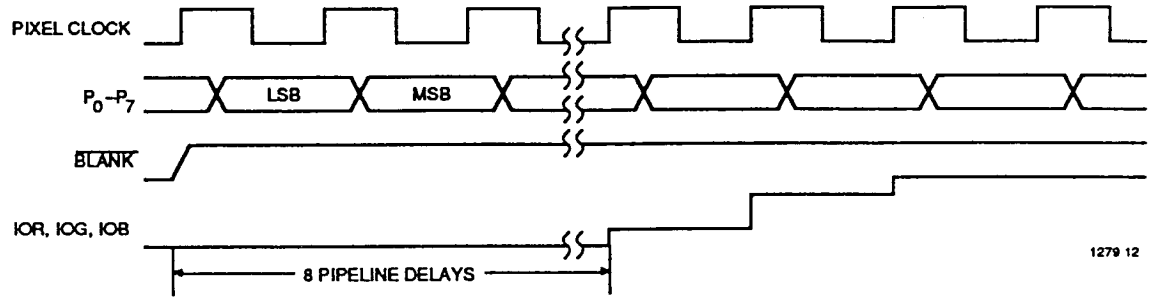


Figure 8. HiCOLOR Mode 2 Timing

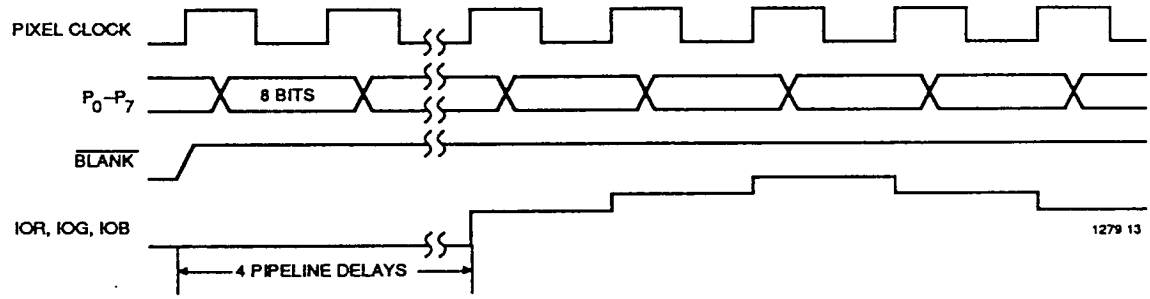


Figure 9. Pseudo Color Mode Timing

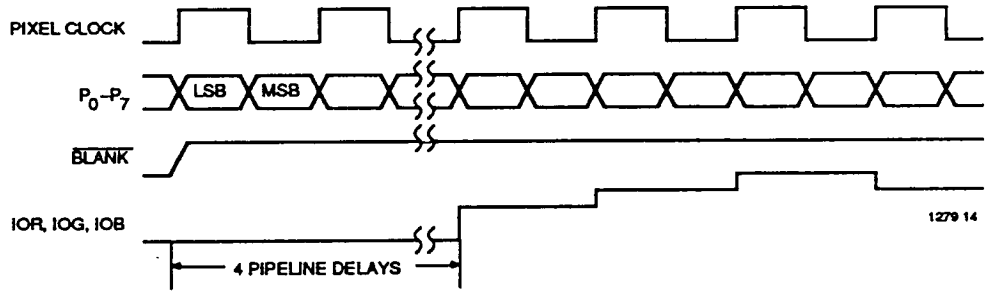


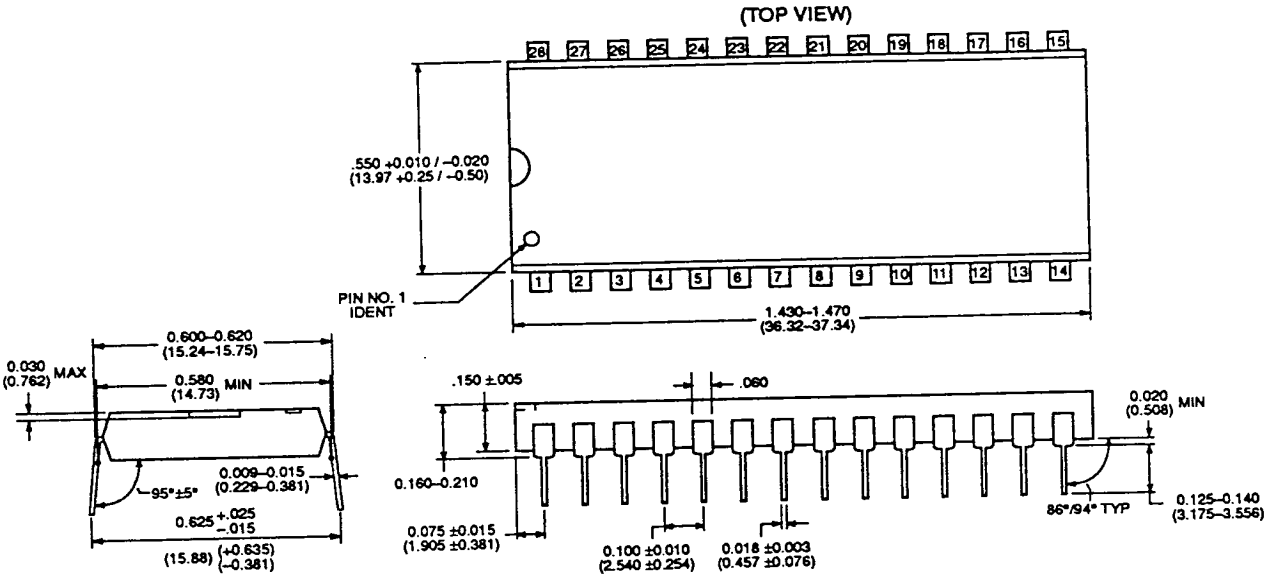
Figure 10. HiCOLOR Mode 1 Timing

ORDERING INFORMATION

PART NO.	COLOR LOOKUP TABLE	OVERLAY REGISTER	SYNC. GEN.	SPEED (MAX)			PACKAGE	AMBIENT TEMP. RANGE
				PSEUDO COLOR	HiCOLOR MODE 1	HiCOLOR MODE 2		
SC11482CV-80	256 x 18	15 x 18	yes	80 MHz	50 MHz	100 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11482CV-66	256 x 18	15 x 18	yes	66 MHz	50 MHz	100 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11482CV-50	256 x 18	15 x 18	yes	50 MHz	45 MHz	90 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11483CV-80	256 x 18	—	no	80 MHz	50 MHz	100 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11483CV-66	256 x 18	—	no	66 MHz	50 MHz	100 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11483CV-50	256 x 18	—	no	50 MHz	45 MHz	90 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11483CN-66	256 x 18	—	no	66 MHz	50 MHz	100 MHz	28-pin 0.6" Plastic DIP	0° to +70°C
SC11483CN-50	256 x 18	—	no	50 MHz	50 MHz	100 MHz	28-pin 0.6" Plastic DIP	0° to +70°C
SC11484CV-80	256 x 24	15 x 24	yes	80 MHz	50 MHz	100 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11484CV-66	256 x 24	15 x 24	yes	66 MHz	50 MHz	100 MHz	44-pin Plastic J-Lead	0° to +70°C
SC11484CV-50	256 x 24	15 x 24	yes	50 MHz	45 MHz	90 MHz	44-pin Plastic J-Lead	0° to +70°C

PHYSICAL DIMENSIONS—Inches (Millimeters)

Package 28-Lead Molded DIP



Package 44-Lead Molded PLCC