SiS300 2D/3D/Video/DVD Accelerator

Preliminary

Rev. 0.3

March 23, 1999

Content

Figures

Tables

1 SIS300 AGP 4X/2X 128-BIT 2D/3D/VIDEO/DVD GRAPHICS ACCELERATOR

1.1 INTRODUCTION

SiS300 is the first chip of the SiS 128-bit graphics accelerator family. With a 365-pin PBGA package, SiS300 integrates a 4X/2X AGP controller with full side-band support, a 128-bit 3D/2D graphics engine and a motion compensation accelerator. It offers a complete 128-bit memory data bus. Embedded with a 128-bit 2D engine, it can achieve ultra high 2D performance with the maximum memory bandwidth up to 2.3 GB/s. An optimized 3D pipeline architecture is implemented for eliminating the overhead resulted from texture read, Z-buffer read/write and destination read latencies and achieving a sustain throughput of over 90% of peak throughput even when texture, Z buffer and alpha blending functions are all enabled. SiS300 also includes a video accelerator and a high performance DVD motion compensation logic to provide very smooth DVD playback. SiS300 provides a 24-bit digital interface to support a secondary display, which is independent of primary CRT display. The digital video interface can also support different TV encoders or LCD transmitters offered by the third party vendors.

SiS301, which is an accompany chip of SiS300, integrates

- A NTSC/PAL video encoder with Macro Vision Ver. 7.0 option for TV display,
- A TMDS transmitter with Bi-Linear scaling capability for TFT LCD panel support,
- And an analog RGB port to support a secondary CRT monitor function.

All the above functions can support dual-view feature. It means that the dual views display independent resolutions, color depths and frame rates. SiS301 receives digital video signals and control signals from SiS300 then transforms them into Composite, S or Component video output for TV display, TMDS signals for LCD display and analog RGB signals for secondary CRT display. The package type of SiS301 is 100-pin TQFP.

1.2 SiS300 FEATURES

PCI Bus Interface

- **Supports 32-bit PCI local bus standard Revision 2.2 compliant**
- **Built-in write-once subsystem and subsystem-vendor ID configuration register for on board VGA or power on auto subsystem and subsystem-vendor ID fetching from BIOS for add-on VGA card.**
- **Built-in PCI power management configuration register for D0, D1, D2 and D3 modes**
- **Supports 133 MHz zero wait-state memory mapped I/O burst write**
- **Built-in 133 MHz zero wait-state 128 bits PCI post-write buffer with byte merge to enhance frame buffer write performance**
- **Built-in read buffer to enhance frame buffer read performance**
- **Supports one wait burst read cycle when read buffer hits**
- **Supports automatic disconnect or retry after wait 16 PCI clocks when read cache misses or post write buffer is full**
- **Supports four wait single I/O read/write cycle**
- **Supports full 32-bit re-locatable VGA I/O address decoding for 128 I/O ports**
- **Supports full 32-bit memory frame buffer address decoding for 128MB size**
- **Supports full 32-bit memory mapped I/O address decoding for 128KB size**
- **Supports full 32-bit ROM address decoding for 32KB, 64KB sizes**
- **Supports flash memory interface for VGA BIOS upgrade**
- **Supports RAMDAC snoop**
- **Supports fast back-to-back timing capable**
- **Supports medium/slow DEVSEL decoding timing**

AGP Interface

- **Supports AGP 2.0 compliant configuration setting**
- **Supports AGP 2X 266 MHz with maximum 32 stages pipeline full side band function**

High Performance & High Quality 3D Accelerator

- **Built-in a high performance 128-bit 3D engine**
  - Built-in 32-bit floating point format VLIW primitive setup engine

- Built-in 64K bits, texture cache
- Supports unified Turbo Queue Architecture with 2D engine to solve 3D and 2D command order problem
- Supports 64KB, 128KB, 256KB and 512KB Turbo Queue sizes
- Supports AGP 2X for texture fetch
- Supports AGP 2X for command fetch and parsing
- Peak polygon rate: 4M polygon/sec @ 1 pixel/polygon with 16 bpp, bilinear textured, Z buffered, and alpha blended
- Peak fill rate: 125M pixel/sec (with 125 MHz 3D engine clock)
- Sustained fill rate: 100 M pixel/sec @ 10,000 pixel/polygon with 16 bpp, bilinear textured, Z buffered, and alpha blended (with 143 MHz 128-bit SGRAM, 125 MHz 3D engine clock)

- **Built-in a high quality 3D engine**
  - Supports flat, and Gouraud shading
  - Supports high quality dithering
  - Supports Z-test, stencil test, alpha test, and scissors clipping test
  - Supports Z pre-test for reducing texture read DRAM bandwidth
  - Supports 256 ROPs
  - Supports individual Z-buffer and render buffer at the same time
  - Supports 16/24/32 BPP Z buffer integer/floating formats
  - Supports 16/32 BPP render buffer format
  - Supports 1/2/4/8 stencil format
  - Supports per-pixel texture/fog perspective correction
  - Supports MIPMAP with point-sampled, linear, bi-linear, and tri-linear texture filtering
  - Supports single pass two MIPMAP texture, one texture one clock
  - Supports up to 2048x2048 texture size
  - Supports 2's power of width and height structure rectangular texture
  - Supports 1/2/4/8 BPP palletize texture with 32 bit ARGB format
  - Supports palette for high performance palette look up
  - Supports 1/2/4/8 BPP luminance texture
  - Supports 1/2/4/8 BPP intensity texture
  - Supports 8/16/24/32 BPP RGB/ARGB texture formats

- Supports video YUV texture in all supported texture formats
- Supports MIP-Mapped texture transparency, blending, wrapping, mirror, and clamping
- Supports fogging, alpha blending
- Supports vertex fogging, linear fogging table and non-linear fogging table
- Supports specula lighting
- Supports sort dependent edge anti-aliasing
- Supports full scene anti-aliasing
- Supports hardware back face culling
- Internal full 32 bits ARGB format ultra pipelined architecture for ultra high performance and high rendering quality

High Performance 2D Accelerator

- **Supports Turbo Queue (Software Command Queue in off-screen memory) architecture to achieve extra-high performance** (SiS patent)
- **Built-in Direct Draw Accelerator**
- **Built-in an 1T 128-bit BITBLT graphics engine with the following functions:**
  - 256 raster operations
  - Rectangle fill
  - Trapezoid fill
  - Color expansion
  - Enhanced color expansion
  - Line-drawing with styled pattern
  - NT fractional point line-drawing with styled pattern
  - Multiple scan-line
  - Built-in 8x8 pattern registers
  - Built-in 8x8 mask registers
  - Rectangle clipping
  - Transparent BitBlt with source and destination keys
  - Hardware auto page flipping
  - 3D Z buffer clear function
- **Supports memory-mapped, zero wait-state, burst engine write**
- **Supports burst frame buffer read/write for SDRAM/SGRAM**

- **Built-in 64x64x2 bit-mapped hardware cursor**
- **Built-in 32x32x16, 32x32x32 bit-mapped color hardware cursor**
- **Maximum 64 MB frame buffer with linear addressing**
- **Supports AGP 2X mode access for all 2D engine functions**
- **Supports SGRAM block write function for Bitblt command**

MPEG-2/1 Video Decoder

- **MPEG-2 ISO/IEC 13818-2 MP@ML and MPEG-1 ISO/IEC 11172-2 standards compliant**
- **Low cost design based on MPEG macro layer decoding architecture**
  - Built-in motion compensation logic
- **Supports AGP 2X mode bus master code fetching**
- **Half pixel resolution in motion compensation**
- **Direct DVD to TV playback**

Video Accelerator

- **Supports single frame buffer architecture**
- **Supports two independent video windows with overlay function and scaling factors**
- **Supports YUV-to-RGB color space conversion**
- **Supports bi-linear video interpolation with integer increments of pixel accuracy**
- **Supports graphics and video overlay function**
  - Independent graphics and video formats
  - Independent two video formats
  - 16 color-key and/or chroma-key operations
  - Supports YUV or RGB format chroma key
  - Video only mode
  - Video CD or DVD to TV playback mode
  - Simultaneous graphics and TV video playback overlay
- **Supports current scan line of refresh read-back and interrupt**
- **Supports tearing free double/triple buffer flipping**

- **Built-in video decoder interface**
  - Philips SAA7110/SAA7111/SAA7111A
  - Brooktree BT815/817/819A/Bt829/BT835 (8-bit SPI mode 1,2)
  - CCIR656 video standard
- **Supports input video vertical blank or line interrupt**
- **Supports video capture and playback tear free auto flipping**
- **Supports independent VBI capture**
- **Supports RGB555, RGB565, YUV422, and YUV420 video capture format**
- **Supports RGB555, RGB565, YUV422, and YUV420 video playback format**
- **Supports filtered horizontal/vertical down scaling capture**
- **Supports filtered horizontal up and down scaling playback**
- **Supports filtered vertical up scaling playback**
- **Supports mirroring capture**
- **Supports DVD sub-picture playback overlay**
- **Supports DVD playback auto-flipping**
- **Built-in video capture FIFOs to support video capture**
- **Built-in two video playback line buffers**
- **Supports DCI Drivers**
- **Supports VPE Drivers**
- **Supports Direct Draw Drivers**

Display Memory Interface

- **Supports SDRAM, ESDRAM and SGRAM timing**
- **Supports 128-bit DRAM channel interface with maximum 2.3 GB/s bandwidth**
- **Supports up to 4 ranks of DRAM for DRAM interface**
- **Supports 32-bit, 64-bit and 128-bit interface with maximum 143 MHz DRAM frequency**
- **Supports 2 MB, 4 MB, 8 MB, 16 MB, 32 MB and 64MB memory configurations**
- **Supports 256Kx32, 512kx32, 1Mx32, 1Mx16 and 4Mx16 SDRAM types up to 143 MHz with 2.3 GB/s bandwidth**
- **Supports fully internal 128-bit display memory path**

- **Supports VGA BIOS auto memory size detecting**
- **Supports ping-pong banking operation by 4 bank registers**
- **Supports SGRAM block write operation**

High Integration

- **Built-in CRT FIFOs to support super high resolution graphics modes and reduce CPU wait-state**
- **Built-in programmable 24-bit true-color RAMDAC up to 270 MHz pixel clock**
  - Built-in reference voltage generator and monitor sense circuit
  - Supports down-loadable 24 bits RAMDAC for gamma correction in high color and true color modes
  - Supports programmable pedestal enable
  - Supports programmable slew rate control
- **Built-in three clock generators**
  - Integrates PLL loop filter for CRT, Engine and DRAM
- **Built-in 14.318/13.5 MHz reference clock oscillator circuits**
- **Built-in two video line buffers for MPEG II video playback**
- **Built-in standard feature connector logic support**
- **Built-in VIP 1.1, VIP 2.0 video port interface**
- **Built-in flash ROM programming interface**
- **Built-in VESA Plug & Display for CH7003, PanelLink™ and LVDS digital interface**
- **Built-in secondary CRT controller for independent secondary CRT, LCD or TV digital output**
- **Built-in Subsystem and Subsystem Vender ID auto power on auto fetch cycle**

Resolution, Color & Frame Rate

- **Supports 270 MHz pixel clock**
- **Supports VESA standard super high resolution graphics modes**
  - 640x480 16/256/32K/64K/16M colors 120 Hz NI
  - 800x600 16/256/32K/64K/16M colors 120 Hz NI
  - 1024x768 256/32K/64K/16M colors 120 Hz NI

- 1280x1024 256/32K/64K/16M colors 120 Hz NI
- 1600x1200 256/32K/64K/16M colors 100 Hz NI
- 1920x1200 256/32K/64K/16M colors 80 Hz NI
- low resolution modes

- **Supports virtual screen up to 4096x4096**

Power Management

- **Supports VESA Display Power Management Signaling (DPMS) compliant VGA monitor for power management**
- **Supports direct I/O command to force graphics controller into standby/suspend/off state**
- **Power down internal SRAM in direct color mode**
- **Supports PCI power management configuration registers for supporting ACPI power down controller**
- **Power down all internal macro cells such as SRAM, DAC, clock generator, DLL when power saving mode**
- **Supports clock stopping for video accelerator when disabled**
- **Supports auto clock throttling for 2D engine, 3D engine**

Multimedia Application

- **Supports DDC1, DDC2B and DDC 3.0 specifications**
- **Supports RAMDAC snoop for multimedia applications**

Miscellaneous

- **Supports 32K, 64K Bytes ROM decoding**
- **Supports Signature Analysis for automatic testing**
- **Supports BIST for internal memory testing**
- **Supports DRAM interface BIST for at speed non-DRAM testing**
- **Implemented by 0.25 um 1.8V CMOS technology with 3.3V/2.5V LVTTL tolerance I/O buffers**
- **365-balls 27mm x 27mm BGA package**

1.3 SiS300 BLOCK DIAGRAM

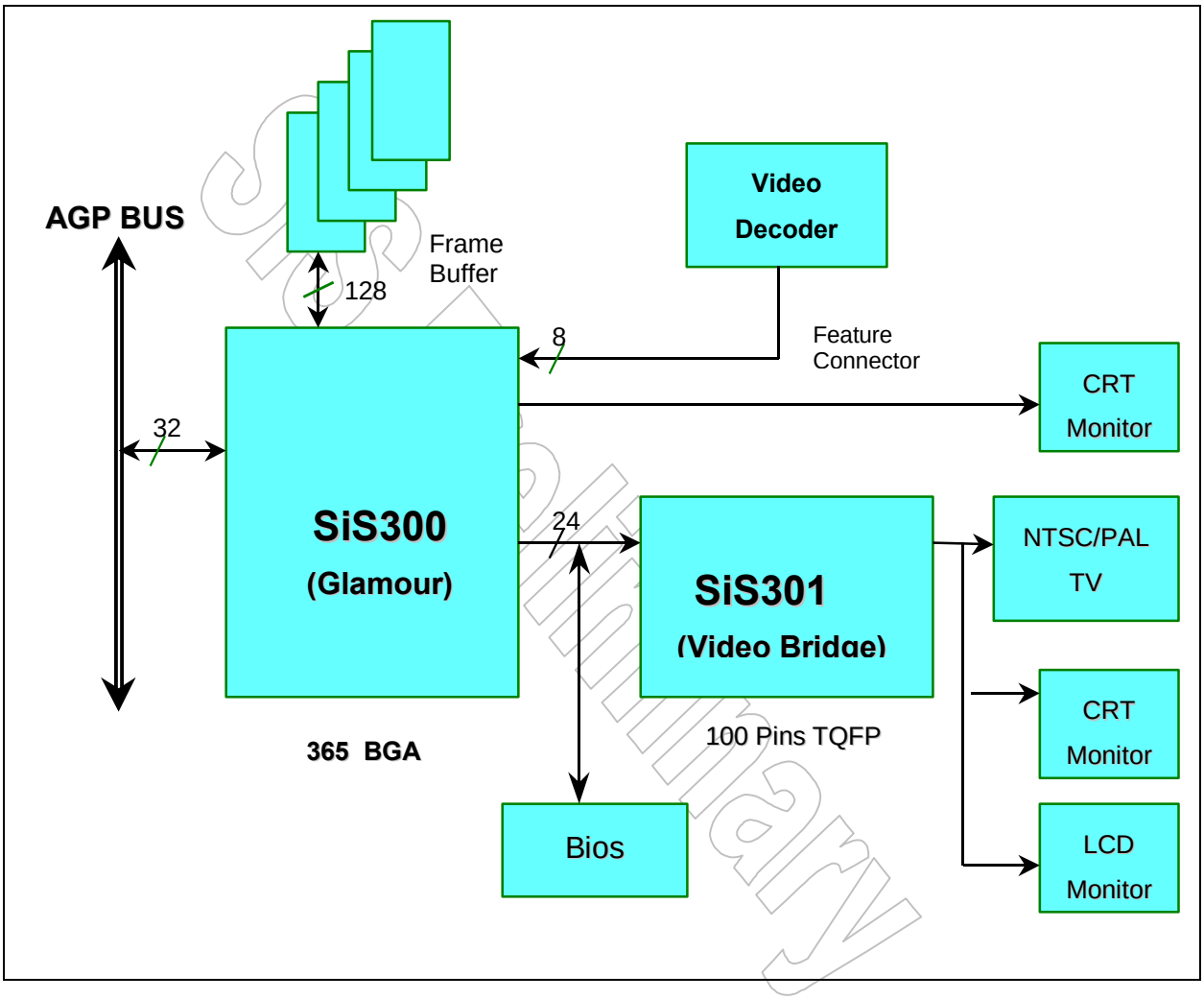

Figure 1.3-1 SiS300 System Block Diagram

2 SIS300 DESCRIPTION

2.1 2D GRAPHICS ENGINE

SiS300 integrated graphics controller supports a powerful graphics engine to enhance the performance. The functions of the graphics engine in SiS300 include BitBlt, Color Expansion, Enhanced Color Expansion, Line Drawing, Transparent BitBlt, Multiple Scan-line and Trapezoid Fill.

Basically the 2D graphics engine of SiS300 is a 128-bit BitBlt graphics engine which inherits from SiS 530 series. SiS300 supports single-cycle read/write and block-write function of SGRAM. For all enhanced 256-color (8 bpp), 32k-color, 64k-color hi-color (16 bpp), 16.8 M-color true color (32 bpp) graphics modes, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Trapezoid fill
- Color expansion
- Enhanced Color expansion
- Line drawing with styled pattern
- NT fractional point line drawing with styled pattern
- Multiple scan-line drawing
- Built-in 8x8 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt with source and destination ranged keys

The following commands are specially designed for boosting the 3D and direct draw performance.

- Clear Z-buffer
- Full scene anti-aliasing Bitblt
- Video auto-flip with synchronous to 2D and 3D engines
- Capability for using AGP memory for all 2D commands

2.2 3D ACCELERATOR

Targeting on Microsoft Direct3D and OpenGL acceleration, SiS300 achieves extremely high fill and polygon rate in superior quality with high balanced pipeline 3D architecture. The major key technologies that guarantee a high 3D performance are the integrated Turbo Queue, Setup Engine, Texture Cache, and Pipeline Render Engine.

The major technologies for the high performance and high quality 3D rendering in SiS300 are:

- Turbo Queue
- Setup Engine
- Texture Cache
- Pipelined Rendering Engine

Turbo Queue in 3D Accelerator

Using the Turbo Queue architecture (*SiS patent*) will speedup the rendering for 3D engine. The Turbo Queue length is up to 512KB, therefore 3D driver can issue commands almost without waiting. To save the high cost for building a long enough hardware command queue, SiS300 allocates a portion of the off-screen memory as the command queue buffer. Once SiS300 detects the status of the internal hardware command queue nearly full, some of the commands in the hardware queue will be temporally swapped to the off-screen area. When 2D or 3D engine finishes previous command, these off-screen commands will be read back first as the next command for execution.

In SiS300 architecture, 2D and 3D engines share the same hardware queue and off-screen command queue but only one engine is active at a time. In this way, we can guarantee a correct execution sequence.

Setup Engine

Setup Engine is one of the most critical parts in the new generation 3D design. It calculates and prepares all of the parameters for primitive drawing. All these computations need more than hundreds of addition, subtraction, multiplication, and division. If we make this setup calculation by host CPU, the sequential coding and processing form a bottleneck for 3D rendering.

To off-load this computation time from host CPU and to do it in parallel, SiS300 integrates a VLIW-like 32-bit floating point Setup Engine. It can finish all of the setup computations for a triangle within 60 memory clocks. Moreover, Setup Engine also supports line and point setup calculations with much less memory clocks than triangle setup required. This Setup Engine, specially designed to fit all the data formats in Microsoft Direct3D API, can accept vertex

values directly in floating point format. One command parser is implemented for parsing vertex format into internal hardware command format for VLIW.

Once Setup Engine finishes the setup computations for a triangle, it transfers all these parameters to Render Engine within one memory clock. While Rendering Engine is busying drawing a triangle, Setup Engine can calculate the parameters needed for the next one.

Rendering Engine

Rendering Engine is a pipelined structure engine in SiS300. This engine is formed by Shading Engine, Texture Engine, and Post Engine.

The output of Shading Engine is a series of pixels with color which represents the shade of a primitive. Texture Engine is responsible for attaching the texture color on a pixel. Then, Post Engine will do some operations such as fogging, alpha blending, dithering, and ROP for this pixel.

To support high quality texture mapping, SiS300 supports point-sampled, linear, bi-linear, and tri-linear texture filtering. With an integrated high-capacity texture cache, SiS300 can render texture pixels in the same fill rate no matter whether point-sampled, linear, or bi-linear texture filtering method is in use. For tri-linear texture mapping, full fill rate can be achieved. But better video quality is expected rendering in tri-linear texture mapping mode.

Texture Cache

Texture Cache is one of the critical part of high performance 3D design. Most of the 3D chips have not built-in texture cache and need to fetch each texture pixel again and again during the rendering process. If the texture is in use for several times, there is no reason to fetch texture from memory again and again. Built-in texture cache could significantly improve texture mapping performance.

With built-in texture cache, each time when a texture miss happens, a segment of texture will be read from texture buffer and stored in a internal texture cache line. In SiS300, eight texels texture cache is implemented with eight texels ports. That is what SiS300 can provide one tri-linear pixel rendering per cycle. Under Direct3D benchmark estimation, more than 98% hit rate has been measured with tri-linear texture mapping. The texture buffer can locate in off-screen area or AGP system memory. If you need very large texture buffer size, the location in AGP system memory is suggested.

Conclusion

The presentation of SiS300 points to the beginning of the new generation of 3D accelerator and the end of low-end, unbalanced 3D solutions. To achieve a high performance in 3D rendering, several strategies have to be utilized. Turbo Queue, Setup Engine, Rendering Engine, and Texture Cache will become the uncompromising choice in high performance 3D architecture.

2.3 DIGITAL VIDEO INTERFACE

SiS300 integrates a high speed 135MHz digital interface video encoder with the capability of independently displaying the video data on both digital video interface and VGA monitor. The output signal formats include RGB888, RGB666 and dithered RGB666 video format. SiS301 video encoder supports NTSC and PAL standards and integrates video DACs, anti-flicker circuits, composite and S video sense circuits. And supports RGB format output and scaled TMDS flat panel signals. Independent display of digital video interface can be supported.

The secondary CRT can have simultaneous display with primary CRT. It can have independent display with primary CRT by different frame rates, different display buffers and different display color depths. It can have under scan scaling for TV and over scan scaling for LCD display. Also it can have horizontal and vertical position adjustment functions.

The SiS300 and SiS301 dual view functions can support the following combinations:

PRIMARY	SECONDARY	VGA MODE	SIMULTANEOUS	INDEPENDENT	UNDER/ OVERSCAN	H/V POSITION ADJUST
CRT1	CRT2	Standard	Yes	No	No	Yes
CRT1	CRT2	Enhanced	Yes	Yes	No	Yes
CRT1	TV	Standard	Yes	No	No	Yes
CRT1	TV	Enhanced	Yes	Yes	Yes	Yes
CRT1	LCD	Standard	Yes	No	Yes	Yes
CRT1	LCD	Enhanced	Yes	Yes	Yes	Yes
Disabled	LCD only	Standard	-	-	Yes	Yes
Disabled	LCD only	Enhanced	-	-	Yes	Yes
Disabled	TV only	Standard	-	-	Yes	Yes
Disabled	TV only	Enhanced	-	-	Yes	Yes

2.4 MPEG-2 MOTION COMPENSATION

SiS300 integrates an MPEG video decoder that supports MPEG-2 video standards. Basically, this MPEG video decoder is a motion compensation decoder that takes about 40% MPEG video decoding computing power and leaves the rest of 60% done by CPU. Therefore the scheme applied in SiS300 is the most economic and efficient approach and retains considerable design flexibility. DVD video standard is under the sustain of this silicon design. It takes not much silicon area but more significantly reduces CPU loading than that

in pure software MPEG video decoder. What CPU has to do in video decoding are syntax parsing, variable-length decoding, inverse quantization and IDCT transform. All of the other video tasks will be done by SiS300.

For MPEG or AC3 audio decoding, it will count on the computation of CPU or an external MPEG or AC3 audio decoder option.

In the process of MPEG video decoding, SiS300 will allocate four image buffers in off-screen area. These four image buffers are for I-picture, P-picture, B-picture (under rendering), and one additional B-picture (under displaying). For MPEG-2 decoding, it takes at least 1980K bytes off-screen memory.

To support MPEG-2 video overlay, SiS300 doubles its video line buffer length and supports up to 1920 pixels width of video playback.

2.5 VIDEO ACCELERATOR

SiS300 video accelerator can work in three different modes: standard FC (feature connector) mode, direct video mode, and PCI multimedia mode.

In standard FC mode, SiS300 supports standard VESA FC standard.

In direct video mode, SiS300 can work with the Philips SAA7110 / SAA7111, Samsung Ks0127 and Brooktree Bt815/817/819A/835 (8-bit SPI mode 1, 2) and CCIR656 video interface format to provide the PC-Video solution. Almost all vendors' video decoders can connect to SiS300 video interface. After receiving the video data, SiS300 will perform scaling and store these video data to display memory. Furthermore SiS300 will perform filtering, and scaling on the stored video data before overlaying with graphics data for final display.

The video input interface can capture RGB565, YUV422 and YUV420 video formats and store the video data into the video frame buffer. The new YUV420 mode can reduce the video capture bandwidth and video capture frame buffer size. The video input unit also provide the horizontal and vertical downscaling filter to generate better video capture quality. The vertical downscaling filter is implemented by video capture frame buffer read back operation, there is no line buffer needed.

In PCI multimedia mode, SiS300 supports PCI multimedia design specification to catch up future potential trend.

The SiS300 can provide dual video windows with independent video data format, window size, independent horizontal and vertical scaling factor and video overlaying. Both video windows can have horizontal and vertical filtering at the same time. The supported video formats includes RGB555, RGB565, YUYV, YVYU, UYVY, VYUY, and YUV420 modes. A horizontal downscaling filter is implemented before each video line buffer. It can perform video downscaling filtering. The pre-scaling filter can be 2-tap, 4-tap and 8-tap.

A sub-picture overlaying video stream is implemented with primary video window for DVD sub-picture display. The sub-picture data is stored in off-screen memory and the sub-picture video data read back is independent of video data read. A 16 entries color palette register is implemented for sub-picture color lookup. A 4-bit blending unit is implemented for combining

the video data and the sub-picture data. The scaling factors of sub-picture should be the same with the video window and the sub-picture scaling will match with the playback video. Only primary video window can support sub-picture blending.

The video overlay is performed by video color key. The color key can be a range of RGB or YUV formats. If the video data passed to the color key test and then the video data would be overlay upon the graphics data. Each video window can have its own video color key. The video windows have priority for two video window overlayings.

Both primary and secondary video windows can overlayprimary graphics and secondary graphics (digital video interface). It supports more convenience about these four video streams usages. That is these two video windows can run at different clock frequency and be totally independent.

2.6 AGP/PCI BUS INTERFACE

SiS300 connects directly to the PCI or AGP bus with no glue logic, and it decodes the 32-bit address and responds to the applicable control lines. It could execute both of the I/O and memory access as an 8-, 16-, and 32-bit device.

In AGP bus interface, SiS300 implements full Side-band feature of AGP 2X mode. One 32-stage command FIFO is implemented for reducing the latency time of AGP read access. The AGP interface is used by MPEG commands read, 3D engine texture read, 3D engine vertex data read and all 2D source data read. The AGP of SiS300 is properly designed to achieve up to 133MHz AGP clock for maximum 1000MB/sec bandwidth.

2.7 DISPLAY MEMORY CONTROLLER

The Display Memory Controller of SiS300 generates timing for display memory. It can support the following DRAM timing:

- SDRAM
- SGRAM
- ESDRAM

For SGRAM, it can support 256Kx32, 512Kx32, and 1Mx32 SGRAM

For SDRAM, it can support 1Mx16, 4Mx16, 2Mx8 SDRAM

For ESDRAM, it can support 1Mx16 and 4Mx16 ESDRAM

The maximum frequency of SiS300 DRAM controller is 143Mhz. It can support up to 2.3 GB/s high bandwidth, with 128-bit DRAM interface. The DRAM capacity can be up to 64MB frame buffer size which can support highest bandwidth for texture buffer instead of texture buffer in AGP memory with lower bandwidth. The DRAM controller is pipeline designed: Optimized DRAM arbiter and SDRAM ping-pong bank operation are also implemented to reduce DRAM pre-charge time for achieving the maximum utilization rate of SDRAM. Thorough 128-bit external and internal data buses make the data throughput meeting the maximum of 128-bit DRAM efficiency.

2.8 OTHER FUNCTION BLOCKS

2.8.1 ATTRIBUTE CONTROLLER

The Attribute Controller formats the display for the screen. Display color selection, text blinking, alternate font selection, and underlining are performed by the Attribute Controller.

2.8.2 CRT CONTROLLER

The CRT Controller generates the HSYNC and VSYNC signals required for the monitor, as well as BLANK signals required by the Attribute Controller.

2.8.3 CRT FIFO

The CRT FIFO allows the Display Memory Controller to access the display memory for screen refresh at maximum memory speed rather than at the screen refresh rate. It provides 3 programmable thresholds - CRT/CPU Threshold Low, CRT/CPU Threshold High, and CRT/Engine Threshold High. With adequate setting these three thresholds, the CPU wait-time would be reduced to improve the graphics performance.

2.8.4 DDC CONTROLLER

The DDC Controller provides two different channels to communicate with the monitor which supports DDC level 1 or DDC level 2B. One is DDC CLK channel which is bi-directional and provides the clock for DDC. The other is DDC DATA channel which is bi-directional and can query some information from monitor.

With the advantage of DDC, VGA BIOS can realize the capability of the connected monitor and take adequate action (such as to program the parameters for higher frame rate, ..., etc.) to make end users feel more comfortable.

2.8.5 DPMS

It provides some registers to control the CRT timing to be compatible with the VESA DPMS specification.

2.8.6 GRAPHICS CONTROLLER

It performs text manipulation, data rotation, color mapping, and miscellaneous operations.

2.8.7 GRAPHICS & VIDEO RAMDAC

The RAMDAC contains the color palette and 24-bit true color DAC. The maximum frequency of the RGB DAC is 270 MHz. It can support 1920x1200 video mode.

The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue.

The 24-bit true color DAC is designed for direct color graphics mode. It converts each digital

color value to three analog voltages for red, green, and blue.

2.8.8 READ-AHEAD CACHE

With read-ahead cache, the times of the operation of display memory read will be reduced, thus enhance the performance.

2.8.9 POST WRITE BUFFER

The post write buffer contains a buffer of CPU write accesses to display memory that have not been executed because of memory arbitration. With this buffer, the SiS300 will release CPU as soon as it records the address and data, and then write into display memory when the display memory is available. Thus CPU performance is increased.

2.8.10 INTERNAL TRIPLE-CLOCK SYNTHESIZER

SiS300 has built-in a triple-clock synthesizer to generate the MCLK, ECLK and VCLK. This clock synthesizer can generate several variable frequencies, thus it can provide the flexibility for selecting the working frequency.

The Triple-Clock Synthesizer generates MCLK, ECLK and VCLK with single external reference clock.(14.318MHz) With this characteristic, we can set the MCLK at the maximum speed which the display memory can work normally, thus it takes the advantage of the real peak memory bandwidth and improves the graphics performance. And we can set the ECLK at the maximum speed which the 3D engine can work normally, thus it takes the advantage of the real peak 3D engine bandwidth and improves the graphics performance. The ECLK frequency can be dynamically reduced when the 3D engine is not busy for reducing the whole chip power consumption.

The following block diagram is for clock synthesizer.

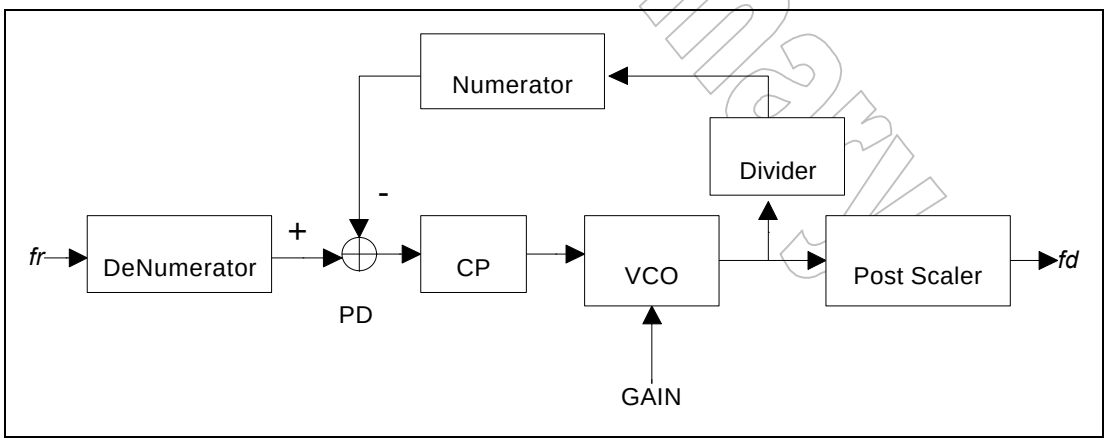

Figure 2.8-1 Block Diagram of Clock Synthesizer

where PD is phase detection,

CP is charge pump,

VCO is voltage controlled oscillator,

fr is reference frequency, and

fd is desired frequency.

The operation of clock synthesizer is described as follows:

When the synthesizer outputs the steady frequency, it means that

*fd=fr**((Numerator+1))/(DeNumerator+1))*(Divider/Post Scalar)

With this formula, we can select adequate values for Numerator, DeNumerator, Divider, and Post Scalar to obtain the desired frequency.

2.8.11 COMPATIBILITY

The SiS300 is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA, and Hercules modes.

2.8.12 PROCESS AND SUPPLY VOLTAGES

SiS300 is manufactured by 1.8 volts CMOS process. No 5 volts VDD pin is required for the reference of voltage tolerance. The supply voltage for internal logic should be within 1.8 volts ± 5%. The supply voltage for DRAM I/O pads should be within 2.5 volts ± 5% or 3.3 volts ± 5%. The supply voltage for AGP I/O pads should be within 3.3 volts ± 5% or 1.5 volts ± 5%. The supply voltage for all analog VDD pins should be within 3.3 volts ± 5%. All other I/O pad supply voltage should be within 3.3 volts ± 5%.

In non-AGP configuration, all the AGP pins must be tight to the ground.

2.8.13 SOFTWARE SUPPORT

To fully utilize and support the SiS300 hardware features, SiS has developed a high-performance VESA extension compliant BIOS.

Extended graphics and text modes are supported by software application drivers which developed by SiS. The following applications are currently supported:

- 3D Studio Version 3.0
- AutoCAD/386 Release 12, 13
- Auto Shade/386 Version 2.0
- Microsoft Windows 3.1 & 3.11
- Microsoft Windows 95

- Microsoft Windows 98
- Microsoft Windows NT Version 4.0 and 5.0
- OS/2 Presentation Manager 3.0, and 4.0

Video operation is supported by software application which drivers developed by SiS. The following applications are currently supported:

- Microsoft Video For Windows
- DCI driver
- Direct Draw driver
- WDM Driver

3D operation are supported by software application drivers developed by SiS. The following applications are currently supported:

- Microsoft Direct3D for Windows 95,Windows 98 and Windows NT 5.0
- OpenGL in Windows 95, Windows 98 and Windows NT

3 MODE TABLES

3.1 STANDARD VGA MODES

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
0	A/N	320x200	16	40x25	B800	8x8	8
0*	A/N	320x350	16	40x25	B800	8x14	8
0+	A/N	360x400	16	40x25	B800	9x16	8
1	A/N	320x200	16	40x25	B800	8x8	8
1*	A/N	320x350	16	40x25	B800	8x14	8
1+	A/N	360x400	16	40x25	B800	9x16	8
2	A/N	640x200	16	80x25	B800	8x8	8
2*	A/N	640x350	16	80x25	B800	8x14	8
2+	A/N	720x400	16	80x25	B800	9x16	8
3	A/N	640x200	16	80x25	B800	8x8	8
3*	A/N	640x350	16	80x25	B800	8x14	8
3+	A/N	720x400	16	80x25	B800	9x16	8
4	APA	320x200	4	40x25	B800	8x8	1
5	APA	320x200	4	40x25	B800	8x8	1
6	APA	640x200	2	80x25	B800	8x8	1
7	A/N	720x350	4	80x25	***B000***	9x14	8
7+	A/N	720x400	4	80x25	***B000***	9x16	8
0D	APA	320x200	16	40x25	A000	8x8	8
0E	APA	640x200	16	80x25	A000	8x8	4
0F	APA	640x350	2	80x25	***B000***	8x14	2
10	APA	640x350	16	80x25	A000	8x14	2
11	APA	640x480	2	80x30	A000	8x16	1
12	APA	640x480	16	80x30	A000	8x16	1
13	APA	320x200	256	40x25	A000	8x8	1

NOTE: 1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphics)

MODE	DISPLAY SIZE	COLORS SHADES	FRAME RATE.	H-SYNC.	VIDEO FREQ.
0	320x200	16	70	31.5 K	25.1 M
0*	320x350	16	70	31.5 K	25.1 M
0+	360x400	16	70	31.5 K	28.3 M
1	320x200	16	70	31.5 K	25.1 M
1*	320x350	16	70	31.5 K	25.1 M
1+	360x400	16	70	31.5 K	28.3 M
2	640x200	16	70	31.5 K	25.1 M
2*	640x350	16	70	31.5 K	25.1 M
2+	720x400	16	70	31.5 K	28.3 M
3	640x200	16	70	31.5 K	25.1 M
3*	640x350	16	70	31.5 K	25.1 M
3+	720x400	16	70	31.5 K	28.3 M
4	320x200	4	70	31.5 K	25.1 M
5	320x200	4	70	31.5 K	25.1 M
6	640x200	2	70	31.5 K	25.1 M
7*	720x350	4	70	31.5 K	28.3 M
7+	720x400	4	70	31.5 K	28.3 M
0D	320x200	16	70	31.5 K	25.1 M
0E	640x200	16	70	31.5 K	25.1 M
0F	640x350	2	70	31.5 K	25.1 M
10	640x350	16	70	31.5 K	25.1 M
11	640x480	2	60	31.5 K	25.1 M
12	640x480	16	60	31.5 K	25.1 M
13	320x200	256	70	31.5 K	25.1 M

NOTE: i - interlaced mode

n - noninterlaced mode

Enhanced video modes

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
25	APA	640x480	16	80x60	A000	8x8	1
29	APA	800x600	16	100x37	A000	8x16	1
2D	APA	640x350	256	80x25	A000	8x14	1
2E	APA	640x480	256	80x30	A000	8x16	1
2F	APA	640x400	256	80x25	A000	8x16	1
30	APA	800x600	256	100x37	A000	8x16	1
31	APA	640x400	64K	80x50	A000	8x16	1
38	APA	1024x768	256	128x48	A000	8x16	1
3A	APA	1280x1024	256	160x64	A000	8x16	1
3C	APA	1600x1200	256	200x75	A000	8x16	1
3D	APA	1600x1200	64K	200x75	A000	8x16	1
3E	APA	1600x1200	16.8M	200x75	A000	8x16	1
40	APA	320x200	32K	40x25	A000	8x8	1
41	APA	320x200	64K	40x25	A000	8x8	1
42	APA	320x200	16.8M	40x25	A000	8x8	1
43	APA	640x480	32K	80x30	A000	8x16	1
44	APA	640x480	64K	80x30	A000	8x16	1
45	APA	640x480	16.8M	80x30	A000	8x16	1
46	APA	800x600	32K	100x37	A000	8x16	1
47	APA	800x600	64K	100x37	A000	8x16	1
48	APA	800x600	16.8M	100x37	A000	8x16	1
49	APA	1024x768	32K	128x48	A000	8x16	1
4A	APA	1024x768	64K	128x48	A000	8x16	1
4B	APA	1024x768	16.8M	128x48	A000	8x16	1
4C	APA	1280x1024	32K	160x64	A000	8x16	1
4D	APA	1280x1024	64K	160x64	A000	8x16	1
4E	APA	1280x1024	16.8M	160x64	A000	8x16	1

62	APA	640x480	32bpp	80x30	A000	8x16	1
63	APA	800x600	32bpp	100x37	A000	8x16	1
64	APA	1024x768	32bpp	128x48	A000	8x16	1
65	APA	1280x1024	32bpp	160x64	A000	8x16	1
66	APA	1600x1200	32bpp	200x75	A000	8x16	1
67	APA	1920x1200	256	240x75	A000	8x16	1
68	APA	1920x1200	64K	240x75	A000	8x16	1
69	APA	1920x1200	32bpp	240x75	A000	8x16	1

NOTE: APA: All Point Addressable (Graphics)

MODE	DISPLAY SIZE	COLORS SHADES	FRAME RATE.	H-SYNC.	VIDEO FREQ.
25	640x480	16	60	31.5 K	25.1 M
29	800x600	16	56	35.1 K	30.0 M
29*	800x600	16	60	37.9 K	40.0 M
29+	800x600	16	72	48.0 K	50.0 M
29#	800x600	16	75	46.8 K	50.0 M
29##	800x600	16	85	53.7 K	56.3 M
2D	640x350	256	70	31.5 K	25.1 M
2E	640x480	256	60	31.5 K	25.1 M
2E*	640x480	256	72	37.9 K	31.5 M
2E+	640x480	256	75	37.5 K	31.5 M
2E++	640x480	256	85	43.4 K	36.0 M
2F	640x400	256	70	31.5 K	25.1 M
30	800x600	256	56	35.1 K	36.0 M
30*	800x600	256	60	37.9 K	40.0 M
30+	800x600	256	72	48.0 K	50.0 M
30#	800x600	256	75	46.8 K	50.0 M
30##	800x600	256	85	53.7 K	56.3 M
31	640x400	64K	70	31.5 K	25.1 M
38i	1024x768	256	87	35.5 K	44.9 M
38n	1024x768	256	60	48.4 K	65.0 M
38n+	1024x768	256	70	56.5 K	75.0 M
38n#	1024x768	256	75	60.2 K	80.0 M
38n##	1024x768	256	85	68.7 K	94.5 M
3Ai	1280x1024	256	87	48.8 K	80.0 M
3An	1280x1024	256	60	65.0 K	110.0 M
3An+	1280x1024	256	75	80.0 K	135.0 M

3Ci	1600x1200	256	87	75.6 K	135.0 M
3C	1600x1200	256	60	75.6 K	162.0 M
3C*	1600x1200	256	65	75.6 K	175.5 M
3Di	1600x1200	64K	87	75.6 K	135.0 M
3D	1600x1200	64K	60	75.6 K	162.0 M
3D*	1600x1200	64K	65	75.6 K	175.5 M
3Ei	1600x1200	16.8M	87	75.6 K	135.0 M
3E	1600x1200	16.8M	60	75.6 K	162.0 M
3E*	1600x1200	16.8M	65	75.6 K	175.5 M
40	320x200	32K	70	31.5 K	25.1 M
41	320x200	64K	70	31.5 K	25.1 M
42	320x200	16.8M	70	31.5 K	25.1 M
43	640x480	32K	60	31.5 K	25.1 M
43*	640x480	32K	72	37.9 K	31.5 M
43+	640x480	32K	75	37.5 K	31.5 M
43++	640x480	32K	85	43.4 K	36.0 M
44	640x480	64K	60	31.5 K	25.1 M
44*	640x480	64K	72	37.9 K	31.5 M
44+	640x480	64K	75	37.5 K	31.5 M
44++	640x480	64K	85	43.4 K	36.0 M
45	640x480	16.8M	60	31.5 K	25.1 M
45*	640x480	16.8M	72	37.9 K	31.5 M
45+	640x480	16.8M	75	37.5 K	31.5 M
45++	640x480	16.8M	85	43.4 K	36.0 M
46	800x600	32K	56	35.1 K	36.0 M
46*	800x600	32K	60	37.9 K	40.0 M
46+	800x600	32K	72	48.0 K	50.0 M
46#	800x600	32K	75	46.8 K	50.0 M

46##	800x600	32K	85	53.7 K	56.3 M
47	800x600	64K	56	35.1 K	36.0 M
47*	800x600	64K	60	37.9 K	40.0 M
47+	800x600	64K	72	48.0 K	50.0 M
47#	800x600	64K	75	46.8 K	50.0 M
47##	800x600	64K	85	53.7 K	56.3 M
48	800x600	16.8M	56	35.1 K	36.0 M
48*	800x600	16.8M	60	37.9 K	40.0 M
48+	800x600	16.8M	72	48.0 K	50.0 M
48#	800x600	16.8M	75	46.8 K	50.0 M
48##	800x600	16.8M	85	53.7 K	56.3 M
49i	1024x768	32K	87	35.5 K	44.9 M
49n	1024x768	32K	60	48.4 K	65.0 M
49n+	1024x768	32K	70	56.5 K	75.0 M
49n#	1024x768	32K	75	60.2 K	80.0 M
49n##	1024x768	32K	85	68.7 K	94.5 M

4Ai	1024x768	64K	87	35.5 K	44.9 M
4An	1024x768	64K	60	48.4 K	65.0 M
4An+	1024x768	64K	70	56.5 K	75.0 M
4An#	1024x768	64K	75	60.2 K	80.0 M
4An##	1024x768	64K	85	68.7 K	94.5 M
4Bi	1024x768	16.8M	87	35.5 K	44.9 M
4Bn	1024x768	16.8M	60	48.4 K	65.0 M
4Bn+	1024x768	16.8M	70	56.5 K	75.0 M
4Bn#	1024x768	16.8M	75	60.2 K	80.0 M
4Bn##	1024x768	16.8M	85	68.7 K	94.5 M
4Ci	1280x1024	32K	89	48.8 K	80.0 M
4Cn	1280x1024	32K	60	65.0 K	110.0 M

4Cn#	1280x1024	32K	75	80.0 K	135.0 M
4Cn##	1280x1024	32K	85	91.1K	157.5M
4Di	1280x1024	64K	89	48.8 K	80.0 M
4Dn	1280x1024	64K	60	65.0 K	110.0 M
4Dn#	1280x1024	64K	75	80.0 K	135.0 M
4Dn##	1280x1024	64K	85	91.1K	157.5M
4Ei	1280x1024	16.8M	89	48.8 K	80.0 M
4En	1280x1024	16.8M	60	65.0 K	110.0 M
4En#	1280x1024	16.8M	75	80.0 K	135.0 M
4En##	1280x1024	16.8M	85	91.1K	157.5M
62	640x480	32BPP	60	31.5 K	25.1 M
62*	640x480	32BPP	72	37.9 K	31.5 M
62+	640x480	32BPP	75	37.5 K	31.5 M
62++	640x480	32BPP	85	43.4 K	36.0 M
63	800x600	32BPP	56	35.1 K	36.0 M
63*	800x600	32BPP	60	37.9 K	40.0 M
63+	800x600	32BPP	72	48.0 K	50.0 M
63#	800x600	32BPP	75	46.8 K	50.0 M
63##	800x600	32BPP	85	53.7 K	56.3 M
64i	1024x768	32BPP	87	35.5 K	44.9 M
64n	1024x768	32BPP	60	48.4 K	65.0 M
64n+	1024x768	32BPP	70	56.5 K	75.0 M
64n#	1024x768	32BPP	75	60.2 K	80.0 M
64n##	1024x768	32BPP	85	68.7 K	94.5 M
65i	1280x1024	32BPP	89	48.8 K	80.0 M
65n	1280x1024	32BPP	60	65.0 K	110.0 M
65n#	1280x1024	32BPP	75	80.0 K	135.0 M
65n##	1280x1024	32BPP	85	91.1K	157.5M
66i	1600x1200	32BPP	87	75.6 K	135.0 M

66n	1600x1200	32BPP	60	75.6 K	162.0 M
66n+	1600x1200	32BPP	65	81.3 K	175.5 M
66n#	1600x1200	32BPP	75	93.8K	202.5M
66n##	1600x1200	32BPP	85	106.3K	229.5M
67	1920x1200	256	60	75.6 K	195.0M
67n	1920x1200	256	75	93.8K	245.0M
67n#	1920x1200	256	80	106.3K	27.0M
68	1920X1200	64K	60	75.6 K	195.0M
68n	1920X1200	64K	75	93.8K	245.0M
68n#	1920x1200	64K	85	106.3K	275.0M
69	1920x1200	16.8M	60	75.6 K	195.0M
69n	1920X1200	16.8M	75	93.8K	245.0M
69n#	1920X1200	16.8M	80	106.3K	270.0M

NOTE: i - interlaced mode

n - noninterlaced mode

3.2 LOW RESOLUTION MODES

MODE	TYPE	DISPLAY SIZE	COLORS SHADES	ALPHA FORMAT	BUFFER START	BOX SIZE	MAX. PAGES
50	APA	320x240	256	40x30	A000	8x8	1
53	APA	320x240	32K	40x30	A000	8x8	1
56	APA	320x240	64K	40x30	A000	8x8	1
51	APA	400x300	256	50x38	A000	8x8	1
54	APA	400x300	32K	50x38	A000	8x8	1
57	APA	400x300	64K	50x38	A000	8x8	1
52	APA	512x384	256	64x48	A000	8x8	1
55	APA	512x384	32K	64x48	A000	8x8	1
58	APA	512x384	64K	64x48	A000	8x8	1

NOTE: 1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphics)

Supported Enhanced CRT Mode and Memory Configuration Table

MODE	DCLK	PAGE SIZE	BAND WIDTH	MINIMAL DRAM REQUIREMENT
640x480x8@60NI	25.1Mhz	300KB	25MB/s	1MB 64-bit SDRAM/SGRAM
640x480x16@60NI	25.1Mhz	600KB	50MB/s	1MB 64-bit SDRAM/SGRAM
640x480x24@60NI	25.1Mhz	900KB	75MB/s	1MB 64-bit SDRAM/SGRAM
640x480x32@60NI	25.1Mhz	1.2MB	100MB/s	2MB 64-bit SDRAM/SGRAM
640x480x8@72NI	31.5Mhz	300KB	31.5MB/s	1MB 64-bit SDRAM/SGRAM
640x480x16@72NI	31.5Mhz	600KB	63MB/s	1MB 64-bit SDRAM/SGRAM
640x480x24@72NI	31.5Mhz	900KB	94.5MB/s	1MB 64-bit SDRAM/SGRAM
640x480x32@72NI	31.5Mhz	1.2MB	126MB/s	2MB 64-bit SDRAM/SGRAM
640x480x8@75NI	31.5Mhz	300KB	31.5MB/s	1MB 64-bit SDRAM/SGRAM
640x480x16@75NI	31.5Mhz	600KB	63MB/s	1MB 64-bit SDRAM/SGRAM
640x480x24@75NI	31.5Mhz	900KB	94.5MB/s	1MB 64-bit SDRAM/SGRAM
640x480x32@75NI	31.5Mhz	1.2MB	126MB/s	2MB 64-bit SDRAM/SGRAM
640x480x8@85NI	36Mhz	300KB	36MB/s	1MB 64-bit SDRAM/SGRAM
640x480x16@85NI	36Mhz	600KB	72MB/s	1MB 64-bit

				SDRAM/SGRAM
640x480x24@85NI	36Mhz	900KB	108MB/s	1MB 64-bit SDRAM/SGRAM
640x480x32@85NI	36Mhz	1.2MB	144MB/s	2MB 64-bit SDRAM/SGRAM
640x480x8@100NI	44.9Mhz	300KB	45MB/s	1MB 64-bit SDRAM/SGRAM
640x480x16@100NI	44.9Mhz	600KB	90MB/s	1MB 64-bit SDRAM/SGRAM
640x480x24@100NI	44.9Mhz	900KB	135MB/s	1MB 64-bit SDRAM/SGRAM
640x480x32@100NI	44.9Mhz	1.2MB	180MB/s	2MB 64-bit SDRAM/SGRAM
640x480x8@120NI	56Mhz	300KB	56MB/s	1MB 64-bit SDRAM/SGRAM
640x480x16@120NI	56Mhz	600KB	112MB/s	1MB 64-bit SDRAM/SGRAM
640x480x24@120NI	56Mhz	900KB	168MB/s	1MB 64-bit SDRAM/SGRAM
640x480x32@120NI	56Mhz	1.2MB	224MB/s	2MB 64-bit SDRAM/SGRAM
800x600x8@60NI	40Mhz	468KB	40MB/s	1MB 64-bit SDRAM/SGRAM
800x600x16@60NI	40Mhz	938KB	80MB/s	1MB 64-bit SDRAM/SGRAM
800x600x24@60NI	40Mhz	1.4MB	120MB/s	2MB 64-bit SDRAM/SGRAM
800x600x32@60NI	40Mhz	1.857MB	160MB/s	2MB 64-bit SDRAM/SGRAM
800x600x8@72NI	50Mhz	468KB	50MB/s	1MB 64-bit SDRAM/SGRAM
800x600x16@72NI	50Mhz	938KB	100MB/s	1MB 64-bit SDRAM/SGRAM
800x600x24@72NI	50Mhz	1.4MB	150MB/s	2MB 64-bit SDRAM/SGRAM
800x600x32@72NI	50Mhz	1.857MB	200MB/s	2MB 64-bit

				SDRAM/SGRAM
800x600x8@75NI	50Mhz	468KB	50MB/s	1MB 64-bit SDRAM/SGRAM
800x600x16@75NI	50Mhz	938KB	100MB/s	1MB 64-bit SDRAM/SGRAM
800x600x24@75NI	50Mhz	1.4MB	150MB/s	2MB 64-bit SDRAM/SGRAM
800x600x32@75NI	50Mhz	1.857MB	200MB/s	2MB 64-bit SDRAM/SGRAM
800x600x8@85NI	56.3Mhz	468KB	56.3MB/s	1MB 64-bit SDRAM/SGRAM
800x600x16@85NI	56.3Mhz	938KB	112.6MB/s	1MB 64-bit SDRAM/SGRAM
800x600x24@85NI	56.3Mhz	1.4MB	168.9MB/s	2MB 64-bit SDRAM/SGRAM
800x600x32@85NI	56.3Mhz	1.857MB	225.2MB/s	2MB 64-bit SDRAM/SGRAM
800x600x8@100NI	67Mhz	468KB	67MB/s	1MB 64-bit SDRAM/SGRAM
800x600x16@100NI	67Mhz	938KB	134MB/s	1MB 64-bit SDRAM/SGRAM
800x600x24@100NI	67Mhz	1.4MB	201MB/s	2MB 64-bit SDRAM/SGRAM
800x600x32@100NI	67Mhz	1.857MB	268MB/s	2MB 64-bit SDRAM/SGRAM
800x600x8@120NI	80Mhz	468KB	80MB/s	1MB 64-bit SDRAM/SGRAM
800x600x16@120NI	80Mhz	938KB	160MB/s	1MB 64-bit SDRAM/SGRAM
800x600x24@120NI	80Mhz	1.4MB	240MB/s	2MB 64-bit SDRAM/SGRAM
800x600x32@120NI	80Mhz	1.857MB	320MB/s	2MB 64-bit SDRAM/SGRAM
1024x768x8@60NI	65Mhz	0.768MB	65MB/s	1MB 64-bit SDRAM/SGRAM
1024x768x16@60NI	65Mhz	1.536MB	130MB/s	2MB 64-bit

				SDRAM/SGRAM
1024x768x24@60NI	65Mhz	2.304MB	195MB/s	4MB 64-bit SDRAM/SGRAM
1024x768x32@60NI	65Mhz	3.072MB	260MB/s	4MB 64-bit SDRAM/SGRAM
1024x768x8@75NI	78.75Mhz	0.768MB	78.75MB/s	1MB 64-bit SDRAM/SGRAM
1024x768x16@75NI	78.75Mhz	1.536MB	157.5MB/s	2MB 64-bit SDRAM/SGRAM
1024x768x24@75NI	78.75Mhz	2.304MB	236.25MB/s	4MB 64-bit SDRAM/SGRAM
1024x768x32@75NI	78.75Mhz	3.072MB	315MB/s	4MB 64-bit SDRAM/SGRAM
1024x768x8@85NI	94.5Mhz	0.768MB	94.5MB/s	1MB 64-bit SDRAM/SGRAM
1024x768x16@85NI	94.5Mhz	1.536MB	189MB/s	2MB 64-bit SDRAM/SGRAM
1024x768x24@85NI	94.5Mhz	2.304MB	283.5MB/s	4MB 64-bit SDRAM/SGRAM
1024x768x32@85NI	94.5Mhz	3.072MB	398MB/s	4MB 64-bit SDRAM/SGRAM
1024x768x8@100NI	110Mhz	0.768MB	110MB/s	1MB 64-bit SDRAM/SGRAM
1024x768x16@100NI	110Mhz	1.536MB	220MB/s	2MB 64-bit SDRAM/SGRAM
1024x768x24@100NI	110Mhz	2.304MB	330MB/s	4MB 64-bit SDRAM/SGRAM
1024x768x32@100NI	110Mhz	3.072MB	440MB/s	4MB 64-bit SDRAM/SGRAM
1024x768x8@120NI	132Mhz	0.768MB	132MB/s	1MB 64-bit SDRAM/SGRAM
1024x768x16@120NI	132Mhz	1.536MB	264MB/s	2MB 64-bit SDRAM/SGRAM
1024x768x24@120NI	132Mhz	2.304MB	396MB/s	4MB 64-bit SDRAM/SGRAM
1024x768x32@120NI	132Mhz	3.072MB	528MB/s	4MB 64-bit

				SDRAM/SGRAM
1280x1024x8@60NI	110Mhz	1.28MB	110MB/s	2MB 64-bit SDRAM/SGRAM
1280x1024x16@60NI	110Mhz	2.56MB	220MB/s	4MB 64-bit SDRAM/SGRAM
1280x1024x24@60NI	110Mhz	3.84MB	330MB/s	4MB 64-bit SDRAM/SGRAM
1280x1024x32@60NI	110Mhz	5.12MB	440MB/s	8MB 64-bit SDRAM/SGRAM
1280x1024x8@75NI	135Mhz	1.28MB	135MB/s	2MB 64-bit SDRAM/SGRAM
1280x1024x16@75NI	135Mhz	2.56MB	270MB/s	4MB 64-bit SDRAM/SGRAM
1280x1024x24@75NI	135Mhz	3.84MB	405MB/s	4MB 64-bit SDRAM/SGRAM
1280x1024x32@75NI	135Mhz	5.12MB	540MB/s	8MB 64-bit SDRAM/SGRAM
1280x1024x8@85NI	157.5Mhz	1.28MB	157.5MB/s	2MB 64-bit SDRAM/SGRAM
1280x1024x16@85NI	157.5Mhz	2.56MB	315MB/s	4MB 64-bit SDRAM/SGRAM
1280x1024x24@85NI	157.5Mhz	3.84MB	472.5MB/s	4MB 64-bit SDRAM/SGRAM
1280x1024x32@85NI	157.5Mhz	5.12MB	630MB/s	8MB 128-bit SDRAM/SGRAM
1280x1024x8@100NI	183.5Mhz	1.28MB	157.5MB/s	2MB 64-bit SDRAM/SGRAM
1280x1024x16@100NI	183.5Mhz	2.56MB	315MB/s	4MB 64-bit SDRAM/SGRAM
1280x1024x24@100NI	183.5Mhz	3.84MB	472.5MB/s	4MB 64-bit SDRAM/SGRAM
1280x1024x32@100NI	183.5Mhz	5.12MB	630MB/s	8MB 128-bit SDRAM/SGRAM
1280x1024x8@120NI	220Mhz	1.28MB	157.5MB/s	2MB 64-bit SDRAM/SGRAM
1280x1024x16@120NI	220Mhz	2.56MB	315MB/s	4MB 64-bit

				SDRAM/SGRAM
1280x1024x24@120NI	220Mhz	3.84MB	472.5MB/s	4MB 64-bit SDRAM/SGRAM
1280x1024x32@120NI	220Mhz	5.12MB	630MB/s	8MB 128-bit SDRAM/SGRAM
1600x1200x8@60NI	162Mhz	1.875MB	162MB/s	4MB 64-bit SDRAM/SGRAM
1600x1200x16@60NI	162Mhz	3.75MB	324MB/s	4MB 64-bit SDRAM/SGRAM
1600x1200x24@60NI	162Mhz	5.625MB	486MB/s	8MB 64-bit SDRAM/SGRAM
1600x1200x32@60NI	162Mhz	7.5MB	648MB/s	8MB 128-bit SDRAM/SGRAM
1600x1200x8@75NI	202.5Mhz	1.875MB	202.5MB/s	4MB 64-bit SDRAM/SGRAM
1600x1200x16@75NI	202.5Mhz	3.75MB	405MB/s	4MB 64-bit SDRAM/SGRAM
1600x1200x24@75NI	202.5Mhz	5.625MB	607.5MB/s	8MB 128-bit SDRAM/SGRAM
1600x1200x32@75NI	202.5Mhz	7.5MB	910MB/s	8MB 128-bit SDRAM/SGRAM
1600x1200x8@85NI	230Mhz	1.875MB	230MB/s	4MB 64-bit SDRAM/SGRAM
1600x1200x16@85NI	230Mhz	3.75MB	460MB/s	4MB 64-bit SDRAM/SGRAM
1600x1200x24@85NI	230Mhz	5.625MB	690MB/s	8MB 128-bit SDRAM/SGRAM
1600x1200x32@85NI	230Mhz	7.5MB	920MB/s	8MB 128-bit SDRAM/SGRAM
1600x1200x8@100NI	270Mhz	1.875MB	270MB/s	4MB 64-bit SDRAM/SGRAM
1600x1200x16@100NI	270Mhz	3.75MB	540MB/s	4MB 64-bit SDRAM/SGRAM
1600x1200x24@100NI	270Mhz	5.625MB	810MB/s	8MB 128-bit SDRAM/SGRAM
1600x1200x32@100NI	270Mhz	7.5MB	1.08GB/s	8MB 128-bit

				SDRAM/SGRAM
1920x1200x8@60NI	195Mhz	2.25MB	195MB/s	4MB 64-bit SDRAM/SGRAM
1920x1200x16@60NI	195Mhz	4.5MB	390MB/s	8MB 64-bit SDRAM/SGRAM
1920x1200x24@60NI	195Mhz	6.75MB	585MB/s	8MB 64-bit SDRAM/SGRAM
1920x1200x32@60NI	195Mhz	9MB	780MB/s	16MB 128-bit SDRAM/SGRAM
1920x1200x8@75NI	240Mhz	2.25MB	240MB/s	4MB 64-bit SDRAM/SGRAM
1920x1200x16@75NI	240Mhz	4.5MB	480MB/s	8MB 64-bit SDRAM/SGRAM
1920x1200x24@75NI	240Mhz	6.75MB	720MB/s	8MB 128-bit SDRAM/SGRAM
1920x1200x32@75NI	240Mhz	9MB	960MB/s	16MB 128-bit SDRAM/SGRAM
1920x1200x8@80NI	270Mhz	2.25MB	275MB/s	4MB 64-bit SDRAM/SGRAM
1920x1200x16@80NI	270Mhz	4.5MB	550MB/s	8MB 64-bit SDRAM/SGRAM
1920x1200x24@80NI	270Mhz	6.75MB	825MB/s	8MB 128-bit SDRAM/SGRAM
1920x1200x32@80NI	270Mhz	9MB	1.1GB/s	16MB 128-bit SDRAM/SGRAM

4 SiS300 PIN LIST AND ASSIGNMENT

AGP/PCI Bus

BALL NO.	SIGNAL NAME	TYPE	DESCRIPTION
B1	RST#	I	PCI Reset is used to bring PCI-specific registers, sequencer, and signals to a consistent state.
E3	BCLK	I	PCI Bus Clock provides timing for all transactions on PCI bus.
**	AD[31:0]	I/O	PCI Address/Data Bus are multiplexed on the same pins. The Address phase is the clock cycle in which FRAME* is asserted and the data phase immediately follows the address phase.
K5, N2, R1, R4	C/BE#[3:0]	I/O	PCI Command/Byte Enable Bus are multiplexed on the same pins. During the address phase of a transaction, C/BE define the bus command, and during the data phase C/BE are used as Byte Enables.
N5	PAR	I/O	PCI Parity Bit is even parity across AD[31:0] and C/BE[3:0].
M5	FRAME#	I/O	PCI Frame Cycle is driven by the current master to indicate the beginning and duration of an access.
N3	TRDY#	I/O	PCI Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
P1	IRDY#	I/O	PCI Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction
N4	STOP#	I/O	PCI Stop indicates the current target is requesting the master to stop the current transaction.
P2	DEVSEL#	I/O	PCI Initialization Device Select is used as a chip select during configuration read and write transactions.
E4	INTA#	I/O	PCI Interrupt indicates the interrupt signal generated by SiS300.
F5	GNT#	I	PCI Master Request indicates to the arbiter that

			this agent desires the use of the bus.
E2	REQ#	I/O	PCI Master Grant indicates to the agent that accesses to the bus has been granted.
F2, F3, E1	ST[2:0]	I	AGP Status bus provides information from the arbiter to a Master on what it may do.
F1	RBF#	I	AGP Read Buffer Full indicates if the master is ready to accept previously requested low priority read data or not.
G5	WBF#	I/O	Reserved for AGP 4X, IDSEL muxed with WBF
L2, U2	AD_STB[1:0]	I	AGP AD Bus Strobe provides timing for 2x data transfer mode on the AD[15:0] and AD[31:16].
K4, R5	AD_STB#[1:0]	I	Reserved for AGP 4X
H2	SB_STB	I/O	AGP STB bus strobe provides timing for 2x data transfer mode on the SBA[7:0]
H5	SB_STB#	I/O	Reserved for AGP 4X
H3, J1, H4, H1, G3, G1, G4, G2	SBA[7:0]	I/O	AGP Sideband bus.
T5	AGPVREF		Reference Voltage for AGP AD[31:0] and AD_STB[1:0] I/O pads.

DRAM Bus

BALL NO.	SIGNAL NAME	TYPE	DESCRIPTION
F17, P18, U12, V6	SCLK[3:0]	I/O	Clock output
**	DQ[127:0]	I/O	Memory data bus
C17, F20, F16, C18, J18, P20, N17, K18, U16, Y10,	DQM#[15:0]	I/O	Memory byte input/output mask

T12, V14, U9, Y2, U5, V5			
R18, T19	CS#[1:0]	I/O	Memory chip select
R20	WE#	I/O	Memory write enable
T20	SRAS#	I/O	SDRAM Row address asserted, bank enable
R19	SCAS#	I/O	SDRAM Column address asserted
P16, P17, U20, U19, R16, R17, T17, T18, U18, W20, V18, V19, V20	MA[12:0]	I/O	Memory address bus
N16	CKE#/DSF#	I/O	Memory clock enable, when using SDRAM DSF, when using SGRAM

FC /Video Port Bus

BALL NO.	SIGNAL NAME	TYPE	DESCRIPTION
D12	PCLK/ VDCLK	I/O	FC pixel clock/ Video port clock input
A12, B12, C12,A13, B13, C13, A14, B14	VIDEO[7:0]	I/O	Video data bus
E12	BLANK#/ VDHSYNC	I/O	Blank video signal/ Video port horizontal sync.
E13	ESYNC/ VDFIELD	I	Enable sync input/ Video port field

C14	EVIDEO	I	Enable video data input
D13	EVDCLK/ VDVSYNC	I	Enable video clock input/ Video port vertical sync.
A6, B6, B7, A7, B8, C8, A8, C7	ROMMA[15:8]/ VBRGB[15:8]	I/O	ROM address bit [15:8]/ Digital video data bit [15:0]
A9, B9, C9, A10, B10, C10, A11	ROMMA[7:0]/ VBRGB[7:0]	I/O	ROM address bit [7:0] Digital video data bit [7:0]
D8, E8, D9, D9, D10, E11, D11, E10	ROMMD[7:0]/ VBRGB[23:16]	I/O	ROM data bit [7:0]/ Digital video data bit [23:16]
B5	VBHSYNC	I/O	Digital video horizontal sync.
C5	VBVSYNC	I/O	Digital video vertical sync.
A5	VBBLANK#	I/O	Digital video display enable
E5	VBRCLK	I/O	Reference clock output to VB
D6	VBCLK	I/O	Digital video clock input
C6	VGCLK	I/O	Digital video clock output
B4	VBCAD	I/O	Control command, address, data
A4	VBHCLK	I/O	Control clock output

VGA OUT

BALL NO.	SIGNAL NAME	TYPE	DESCRIPTION
D1	R	AO	DAC analog R output
D2	G	AO	DAC analog G output
C1	B	AO	DAC analog B output
B1	RSET	A	DAC reference resistor
C2	VREF	A	DAC voltage reference

C3	COMP	A	DAC compensation
D5	HSYNC	I/O	Horizontal sync
E6	VSYNC	I/O	Vertical sync
D7	DDCDATA	I/O	Display data channel data line
C4	DDCCLK	I/O	Display data channel clock line

Misc.

BALL NO.	SIGNAL NAME	TYPE	DESCRIPTION
A1	REFOSCI	AI	Reference clock oscillator input
B2	REFOSCO	AO	Reference clock oscillator output
E7	ROMCS#	I/O	ROM chip select
A3	ROMWE#	I/O	ROM chip write enable
B3	ENTEST#	I	Enable internal test

5 SiS300 CONFIGURATION DEFINITIONS HARDWARE TRAP LIST

PIN NAME	VALUE	REGISTER	DESCRIPTION
ROMMD[2:0]	000 001 010 others	SR3A-D[2:0]	SDR SDRAM SDR SGRAM ESDRAM reserved
ROMMD3	-	SR3A-D3	reserved
ROMMD[5:4]	00 01 10 11	SR3A-D[5:4]	AGP 2X support AGP 1X support reserved PCI bus interface
ROMMD6	0 1	SR3A-D6	Select internal clock generator Select external clock input for ECLK, MCLK, DCLK for testing mode
ROMMD7	0 1	SR3A-D7	BCLK PLL enable BCLK PLL disable
ROMMA0	0 1	SR38-D0	NTSC PAL
ROMMA[2:1]	00 01 10 11	SR38-D[2:1]	64KB ROM decoding 32KB ROM decoding reserved BIOS ROM decoding disable
ROMMA3	0 1	SR38-D3	Interrupt request disable Interrupt request enable
ROMMA4	0 1	SR38-D4	Software Programming Sub-system Vender ID Power On Auto Fetch Sub System Vender ID
ROMMA5	0 1	SR38-D5	Disable SiS301 Enable SiS301

ROMMA6	0 1	SR38-D6	1.5V AGP(Direct connect to AGP slot pin Typedef# 3.3V AGP
ROMMA7	0 1	SR38-D7	Back to back disable Back to back enable
ROMMA8	0 1	SR39-D0	Multiple function disable Multiple function enable
ROMMA9	0 1	SR39-D1	Multiple function selection 0 Multiple function selection 1
ROMMA10	0 1	SR39-D2	PCI medium decoding PCI slow decoding
ROMMA11	0 1	SR39-D3	PCI/AGP I/O low drive PCI/AGP I/O high drive
ROMMA [13:12]	-	SR39-D[5:4]	DLL parameter setting
ROMMA14	0 1	SR39-D6	PCI/AGP I/O low slew rate PCI/AGP I/O high slew rate

Note: Value 0 means No pull high resistor

Value 1 means connect to pull high resistor to pin

5.1 GENERAL REGISTERS

5.1.1 MISCELLANEOUS OUTPUT REGISTERS

Register Type: Read/Write
Read Port: 3CC
Write Port: 3C2
Default: 00h

D7 Vertical Sync Polarity
- 0: Select 'positive vertical sync'
- 1: Select 'negative vertical sync'

D6 Horizontal Sync Polarity
- 0: Select 'positive horizontal sync'
- 1: Select 'negative horizontal sync'

Table 5.1-1 Sync Polarity vs. Vertical Screen Resolution

D7	D6	EGA	VGA
0	0	200 Lines	Invalid
0	1	350 Lines	400 Lines
1	0	Invalid	350 Lines
1	1	Invalid	480 Lines

D5 Odd/Even Page
0: Select low page of memory
1: Select high page of memory
D4 Reserved
D[3:2] Clock Select

Table 5.1-2 Table for Video Clock Selection

D3	D2	DCLK
0	0	25.175 MHz
0	1	28.322 MHz
1	0	Don't Care
1	1	For internal clock generator.

D1 Display RAM Enable
0: Disable processor access to video RAM
1: Enable processor access to video RAM
D0 I/O Address Select
0: Sets addresses for monochrome emulation
1: Sets addresses for color graphics emulation

5.1.2 FEATURE CONTROL REGISTER

Register Type: Read/Write
Read Port: 3CA
Write Port: 3BA/3DA
Default: 00h
D[7:4] Reserved (0)
D3 Vertical Sync Select
0: Normal Vertical Sync output to monitor
1: [Vertical Sync OR Vertical Display Enable] output to monitor
D[2:0] Reserved (0)

5.1.3 INPUT STATUS REGISTER 0

Register Type: Read only
Read Port: 3C2
Default: 00h
D7 Vertical Retrace Interrupt Pending
0: Cleared
1: Pending
D[6:5] Reserved
D4 Switch Sense
D[3:0] Reserved

5.1.4 INPUT STATUS REGISTER 1

Register Type: Read only
Read Port: 3BA/3DA
Default: 00h
D[7:6] Reserved
D[5:4] Diagnostic

Table 5.1-3 Table for Video Read-back Through Diagnostic Bit (I)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
D5	**D4**	**D5**	**D4**
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table 5.1-4 Table for Video Read-back Through Diagnostic Bit (II)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
D5	**D4**	**D5**	**D4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D3 Vertical Trace
0: Inactive
1: Active

D[2:1] Reserved
D0 Display Enable Not
0: Display period
1: Retrace period

5.1.5 VGA ENABLE REGISTER

Register Type: Read/Write
Read/Write Port: 3C3
Default: 00h
D0 VGA Enable
0: Disable
1: Enable

5.1.6 SEGMENT SELECTION REGISTER 0

Register Type: Read/Write
Read/Write Port: 3CD
Default: 00h
D[7:0] Segment Selection Write Bit[7:0]

5.1.7 SEGMENT SELECTION REGISTER 1

Register Type: Read/Write
Read/Write Port: 3CB
Default: 00h
D[7:0] Segment Selection Read Bit[7:0]

5.2 CRT CONTROLLER REGISTERS

5.2.1 CRT CONTROLLER INDEX REGISTER

Register Type: Read/Write
Read/Write Port: 3B4/3D4
Default: 00h
D[7:0] CRT Controller Index
- 00h ~ 18h for standard VGA
- 19h ~ 26h for SiS extended CRT registers

Table 5.2-1 Table of CRT Controller Registers

INDEX (3B4/3D4)	CRT CONTROLLER REGISTERS (3B5/3D5)
00h	Horizontal Total
01h	Horizontal Display Enable End
02h	Horizontal Blank Start
03h	Horizontal Blank End

04h	Horizontal Retrace Start
05h	Horizontal Retrace End
06h	Vertical Total
07h	Overflow Register
08h	Preset Row Scan
09h	Max Scan Line/Text Character Height
0Ah	Text Cursor Start
0Bh	Text Cursor End
0Ch	Screen Start Address High
0Dh	Screen Start Address Low
0Eh	Text Cursor Location High
0Fh	Text Cursor Location Low
10h	Vertical Retrace Start
11h	Vertical Retrace End
12h	Vertical Display Enable End
13h	Screen Offset
14h	Underline Location
15h	Vertical Blank Start
16h	Vertical Blank End
17h	Mode Control
18h	Line Compare
1Bh	CRT horizontal counter read-back
1Ch	CRT vertical counter read back
1Dh	CRT overflow counter read back
22h	Graphics Data Latch Read-back Register
24h	Attribute Controller Toggle Read-back Register
26h	Attribute Controller Index Read-back Register

5.2.2 CR0: HORIZONTAL TOTAL

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 00h
Default: 00h
D[7:0] Horizontal Total Bit[7:0]

5.2.3 CR1: HORIZONTAL DISPLAY ENABLE END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 01h
Default: 00h
D[7:0] Horizontal Display Enable End Bit[7:0]

5.2.4 CR2: HORIZONTAL BLANK START

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 02h
Default: 00h
D[7:0] Horizontal Blank Start Bit[7:0]

5.2.5 CR3: HORIZONTAL BLANK END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 03h
Default: 00h
D7 Reserved
D[6:5] Display Skew Control Bit[1:0]
00: No skew
01: Skew 1 character
10: Skew 2 characters
11: Skew 3 characters
D[4:0] Horizontal Blank End Bit[4:0]

5.2.6 CR4: HORIZONTAL RETRACE START

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 04h
Default: 00h
D[7:0] Horizontal Retrace Start Bit[7:0]

5.2.7 CR5: HORIZONTAL RETRACE END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 05h
Default: 00h
D7 Horizontal Blank End Bit[5]
D[6:5] Horizontal Retrace Delay Bit[1:0]
00: Skew 0 character clock
01: Skew 1 character clock
10: Skew 2 character clocks
11: Skew 3 character clocks
D[4:0] Horizontal Retrace End Bit[4:0]

5.2.8 CR6: VERTICAL TOTAL

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 06h
Default: 00h
D[7:0] Vertical Total Bit[7:0]

5.2.9 CR7: OVERFLOW REGISTER

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 07h
Default: 00h
D7 Vertical Retrace Start Bit[9]
D6 Vertical Display Enable End Bit[9]
D5 Vertical Total Bit[9]
D4 Line Compare Bit[8]
D3 Vertical Blank Start Bit[8]
D2 Vertical Retrace Start Bit[8]
D1 Vertical Display Enable End Bit[8]
D0 Vertical Total Bit[8]

5.2.10 CR8: PRESET ROW SCAN

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 08h
Default: 00h
D7 Reserved
D[6:5] Byte Panning Control Bit[1:0]
D[4:0] Preset Row Scan Bit[4:0]

5.2.11 CR9: MAXIMUM SCAN LINE/TEXT CHARACTER HEIGHT

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 09h
Default: 00h
D7 Double Scan
0: Disable
1: Enable 400 lines display
D6 Line Compare Bit[9]
D5 Vertical Blank Start Bit[9]
D[4:0] Character Cell Height Bit[4:0]

5.2.12 CRA: TEXT CURSOR START

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ah
Default: 00h
D[7:6] Reserved
D5 Text Cursor Off
0: Text Cursor On
1: Text Cursor Off
D[4:0] Text Cursor Start Bit[4:0]

5.2.13 CRB: TEXT CURSOR END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Bh
Default: 00h
D7 Reserved
D[6:5] Text Cursor Skew
00: No skew
01: Skew one character clock
10: Skew two character clocks
11: Skew three character clocks
D[4:0] Text Cursor End Bit[4:0]

5.2.14 CRC: SCREEN START ADDRESS HIGH

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ch
Default: 00h
D[7:0] Screen Start Address Bit[15:8]

5.2.15 CRD: SCREEN START ADDRESS LOW

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Dh
Default: 00h
D[7:0] Screen Start Address Bit[7:0]

5.2.16 CRE: TEXT CURSOR LOCATION HIGH

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Eh
Default: 00h
D[7:0] Text Cursor Location Bit[15:8]

5.2.17 CRF: TEXT CURSOR LOCATION LOW

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Fh
Default: 00h
D[7:0] Text Cursor Location Bit[7:0]

5.2.18 CR10: VERTICAL RETRACE START

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 10h
Default: 00h
D[7:0] Vertical Retrace Start Bit[7:0]

5.2.19 CR11: VERTICAL RETRACE END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 11h
Default: 00h

D7	Write Protect for CR0 to CR7 0: Disable Write Protect 1: Enable Write Protect
D6	Alternate Refresh Rate 0: Selects three refresh cycles per scanline 1: Selects five refresh cycles per scanline
D5	Vertical Interrupt Enable 0: Enable 1: Disable
D4	Vertical Interrupt Clear 0: Clear 1: Not Clear
D[3:0]	Vertical Retrace End Bit[3:0]

5.2.20 CR12: VERTICAL DISPLAY ENABLE END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 12h
Default: 00h

D[7:0]	Vertical Display Enable End Bit[7:0]

5.2.21 CR13: SCREEN OFFSET

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 13h
Default: 00h

D[7:0]	Screen Offset Bit[7:0]

5.2.22 CR14: UNDERLINE LOCATION REGISTER

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 14h
Default: 00h

D7	Reserved
D6	Double-word Mode Enable 0: Disable 1: Enable
D5	Count by 4 0: Disable 1: Enable
D[4:0]	Underline Location Bit[4:0]

5.2.23 CR15: VERTICAL BLANK START

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 15h
Default: 00h

D[7:0]	Vertical Blank Start Bit[7:0]

5.2.24 CR16: VERTICAL BLANK END

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 16h
Default: 00h
D[7:0] Vertical Blank End Bit[7:0]

5.2.25 CR17: MODE CONTROL REGISTER

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 17h
Default: 00h
D7 Hardware Reset
0: Disable horizontal and vertical retrace outputs
1: Enable horizontal and vertical retrace outputs
D6 Word/Byte Address Mode
0: Set the memory address mode to word
1: Set the memory address mode to byte

D5 Address Wrap
0: Disable the full 256K of memory
1: Enable the full 256K of memory
D4 Reserved
D3 Count by Two
0: Byte refresh
1: Word refresh
D2 Horizontal Retrace Select
0: Normal
1: Double Scan
D1 RA1 replace MA14
0: Enable
1: Disable
D0 RA0 replace MA13
0: Enable
1: Disable

5.2.26 CR18: LINE COMPARE REGISTER

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 18h
Default: 00h
D[7:0] Line Compare Bit[7:0]

5.2.27 CR1B: CRT HORIZONTAL COUNTER READ BACK

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Bh
Default: xxh
D[7:0] CRT horizontal counter bit[7:0]

5.2.28 CR1C: CRT VERTICAL COUNTER READ BACK

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Ch
Default: xxh
D[7:0] CRT vertical counter bit[7:0]

5.2.29 CR1D: CRT OVERFLOW COUNTER READ BACK

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Dh
Default: xxh
D[7:5] Reserved
D4 CRT horizontal counter bit 8
D3 Reserved
D[2:0] CRT vertical counter bit[10:8]

Note: The horizontal and vertical counter value will be latched when read register CR20. So the three registers value should be read after read CR20.

5.2.30 CR1E: EXTENDED SIGNATURE READ-BACK REGISTER 2

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Eh
Default: xxh
D[7:0] Signature read-back bit[23:16]

5.2.31 CR20: CRT COUNTER TRIGGER PORT

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 20h
Default: xxh
D[7:0] Reserved

5.2.32 CR24: ATTRIBUTE CONTROLLER TOGGLE READ-BACK REGISTER

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 24h
Default: xxh
D7 Attribute Controller Toggle
D[6:0] Reserved

5.2.33 CR26: ATTRIBUTE CONTROLLER INDEX READ-BACK REGISTER

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 26h
Default: xxh
D[7:6] Reserved
D5 Video Enable
D[4:0] Attribute Controller Index bit[8:4]

5.3 SEQUENCER REGISTERS

5.3.1 SEQUENCER INDEX REGISTER

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h
D[7:6] Reserved
D[5:0] Sequencer Index Bit[5:0]

Table 5.3-1 Table of Sequencer Registers

INDEX (3C4)	SEQUENCER REGISTER (3C5)
00	Reset Register
01	Clock Mode
02	Color Plane Write Enable
03	Character Generator Select
04	Memory Mode

5.3.2 SR0: RESET REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 00h
Default: 00h
D[7:2] Reserved
D1 Synchronous reset
0: Reset
1: Normal
D0 Asynchronous reset
0: Reset
1: Normal

5.3.3 SR1: CLOCK MODE REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 01h
Default: 00h
D[7:6] Reserved
D5 Screen Off
0: Display On
1: Display Off
D4 Shifter Load 32 enable
0: Disable
1: Data shifter loaded every 4th Character Clock
D3 Dot Clock Divide by 2 enable
0: Disable
1: Video Clock is divided by 2 to generate Dot Clock

D2 Shifter Load 16 (while D4=0)
0: Disable
1: Data shifter loaded every 2nd Character Clock
D1 Reserved
D0 8/9 Dot Clock
0: Dot Clock is divided by 9 to generate Character Clock
1: Dot Clock is divided by 8 to generate Character Clock

5.3.4 SR2: COLOR PLANE WRITE ENABLE REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 02h
Default: 00h
D[7:4] Reserved
D3 Plane 3 write enable
0: Disable
1: Enable
D2 Plane 2 write enable
0: Disable
1: Enable
D1 Plane 1 write enable
0: Disable
1: Enable
D0 Plane 0 write enable
0: Disable
1: Enable

5.3.5 SR3: CHARACTER GENERATOR SELECT REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 03h
Default: 00h
D[7:6] Reserved
D5 Character generator table B select Bit[2]
D4 Character generator table A select Bit[2]
D[3:2] Character generator table B select Bit[1:0]
D[1:0] Character generator table A select Bit[1:0]

Table 5.3-2 Table of Selecting Active Character Generator

D5	D3	D2	USED WHEN TEXT ATTRIBUTE BIT 3 IS 1
D4	D1	D0	USED WHEN TEXT ATTRIBUTE BIT 3 IS 0
0	0	0	Character Table 1
0	0	1	Character Table 2
0	1	0	Character Table 3
0	1	1	Character Table 4

1	0	0	Character Table 5 (VGA only)
1	0	1	Character Table 6 (VGA only)
1	1	0	Character Table 7 (VGA only)
1	1	1	Character Table 8 (VGA only)

5.3.6 SR4: MEMORY MODE REGISTER

Register Type: Read/Write
Read/Write Port: 3C5, Index 04h
Default: 00h
D[7:4] Reserved
D3 Chain-4 Mode enable
0: Disable
1: Enable
D2 Odd/Even Mode enable
0: Enable
1: Disable
D1 Extended Memory
0: Select 64K
1: Select 256K
D0 Reserved

5.4 GRAPHICS CONTROLLER REGISTERS

5.4.1 GRAPHICS CONTROLLER INDEX REGISTER

Register Type: Read/Write
Read/Write Port: 3CE
Default: 00h
D[7:4] Reserved
D[3:0] Graphics Controller Index Bit[3:0]

Table 5.4-1 Table of Graphics Controller Registers

INDEX (3CE)	GRAPHICS CONTROLLER REGISTER (3CF)
00	Set/Reset Register
01	Set/Reset Enable Register
02	Color Compare Register
03	Data Rotate & Function Select
04	Read Plane Select Register
05	Mode Register

06	Miscellaneous Register
07	Color Don't Care Register
08	Bit Mask Register

5.4.2 GR0: SET/RESET REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 00h
Default: 00h
D[7:4] Reserved
D3 Set/Reset Map for plane 3
D2 Set/Reset Map for plane 2
D1 Set/Reset Map for plane 1
D0 Set/Reset Map for plane 0

5.4.3 GR1: SET/RESET ENABLE REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 01h
Default: 00h
D[7:4] Reserved
D3 Enable Set/Reset for plane 3
0: Disable
1: Enable
D2 Enable Set/Reset for plane 2
0: Disable
1: Enable
D1 Enable Set/Reset for plane 1
0: Disable
1: Enable
D0 Enable Set/Reset for plane 0
0: Disable
1: Enable

5.4.4 GR2: COLOR COMPARE REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 02h
Default: 00h
D[7:4] Reserved
D3 Color Compare Map for plane 3
D2 Color Compare Map for plane 2
D1 Color Compare Map for plane 1
D0 Color Compare Map for plane 0

5.4.5 GR3: DATA ROTATE/FUNCTION SELECT REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 03h
Default: 00h
D[7:5] Reserved
D[4:3] Function Select

Table 5.4-2 Table of Function Select

D4	D3	FUNCTION
0	0	write data unmodified
0	1	write data AND processor latches
1	0	write data OR processor latches
1	1	write data XOR processor latches

D[2:0] Rotate Count

Table 5.4-3 Table of Rotate Count

D2	D1	D0	RIGHT ROTATION
0	0	0	none
0	0	1	1 bits
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

5.4.6 GR4: READ PLANE SELECT REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 04h
Default: 00h
D[7:2] Reserved
D[1:0] Read Plane Select bit 1, 0
00: Plane 0
01: Plane 1
10: Plane 2
11: Plane 3

5.4.7 GR5: MODE REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 05h
Default: 00h
D7 Reserved
D6 256-color Mode
0: Disable
1: Enable

D5 Shift Register Mode
0: Configure shift register to be EGA compatible
1: Configure shift register to be CGA compatible
D4 Odd/Even Addressing Mode enable
0: Disable
1: Enable
D3 Read Mode
0: Map Select Read
1: Color Compare Read
D2 Reserved
D[1:0] Write mode

Table 5.4-4 Table for Write Mode

D1	D0	MODE SELECTED
0	0	Write Mode 0: Direct processor write (Data Rotate, Set/Reset may apply).
0	1	Write Mode 1: Use content of latches as write data.
1	0	Write Mode 2: Color Plane n(0-3) is filled with the value of bit m in the processor write data.
1	1	Write Mode 3: Color Plane n(0-3) is filled with 8 bits of the color value contained in the Set/Reset Register for that plane. The Enable Set/Reset Register is not effective. Processor data will be AND with Bit Mask Register content to form new bit mask pattern. (data rotate may apply).

5.4.8 GR6: MISCELLANEOUS REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 06h
Default: 00h
D[7:4] Reserved
D[3:2] Memory Address Select

Table 5.4-5 Table of Memory Address Select

D3	D2	ADDRESS RANGE
0	0	A0000 to BFFFF
0	1	A0000 to AFFFF
1	0	B0000 to B7FFF
1	1	B8000 to BFFFF

D1 Chain Odd And Even Maps
0: Disable
1: Enable

D0 Graphics Mode Enable
0: Select alphanumeric mode
1: Select graphics mode

5.4.9 GR7: COLOR DON'T CARE REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 07h
Default: 00h

D[7:4] Reserved

D3 Plane 3 Don't Care
0: Disable color comparison
1: Enable color comparison

D2 Plane 2 Don't Care
0: Disable color comparison
1: Enable color comparison

D1 Plane 1 Don't Care
0: Disable color comparison
1: Enable color comparison

D0 Plane 0 Don't Care
0: Disable color comparison
1: Enable color comparison

5.4.10 GR8: BIT MASK REGISTER

Register Type: Read/Write
Read/Write Port: 3CF, Index 08h
Default: 00h

D[7:0] Bit Mask Enable Bit[7:0]

5.5 ATTRIBUTE CONTROLLER AND VIDEO DAC REGISTERS

5.5.1 ATTRIBUTE CONTROLLER INDEX REGISTER

Register Type: Read/Write
Read Port: 3C0
Write Port: 3C0
Default: 00h
D[7:6] Reserved
D5 Palette Address Source
0: From CPU
1: From CRT
D[4:0] Attribute Controller Index Bit[4:0] (00h-14h)

Table 5.5-1 Table of Attribute Controller Registers

INDEX (3C0)	ATTRIBUTE CONTROLLER REGISTER (3C0)
00h	Color Palette Register 0
01h	Color Palette Register 1
02h	Color Palette Register 2
03h	Color Palette Register 3
04h	Color Palette Register 4
05h	Color Palette Register 5
06h	Color Palette Register 6
07h	Color Palette Register 7
08h	Color Palette Register 8
09h	Color Palette Register 9
0Ah	Color Palette Register 10
0Bh	Color Palette Register 11
0Ch	Color Palette Register 12
0Dh	Color Palette Register 13
0Eh	Color Palette Register 14
0Fh	Color Palette Register 15
10h	Mode Control Register
11h	Screen Border Color
12h	Color Plane Enable Register

13h	Pixel Panning Register
14h	Color Select Register (VGA)

5.5.2 AR0~ARF: PALETTE REGISTERS

Register Type: Read/Write
Read Port: 3C1, Index 00h ~ 0Fh
Write Port: 3C0, Index 00h ~ 0Fh
Default: 00h
D[7:6] Reserved
D[5:0] Palette Entries

5.5.3 AR10: MODE CONTROL REGISTER

Register Type: Read/Write
Read Port: 3C1, Index 10h
Write Port: 3C0, Index 10h
Default: 00h
D7 P4, P5 Source Select
0: AR0-F Bit[5:4] are used as the source for the Lookup Table Address Bit[5:4]
1: AR14 Bit[1:0] are used as the source for the Lookup Table Address Bit[5:4]
D6 Pixel Double Clock Select
0: The pixels are clocked at every clock cycle
1: The pixels are clocked at every other clock cycle
D5 PEL Panning Compatibility with Line Compare
0: Disable
1: Enable
D4 Reserved
D3 Background Intensity or Blink enable (while the Character Attribute D7=1)
0: Background Intensity attribute enable
1: Background Blink attribute enable
D2 Line Graphics enable
0: The ninth bit of nine-bit-wide character cell will be the same as the background.
1: The ninth bit of nine-bit-wide character cell will be made be the same as the eighth bit for character codes in the range C0h through DFh.
D1 Display Type
0: The contents of the Attribute byte are treated as color attribute.
1: The contents of the Attribute byte are treated as MDA-compatible attribute.
D0 Graphics/Text Mode
0: The Attribute Controller will function in text mode.
1: The Attribute Controller will function in graphics mode.

5.5.4 AR11: SCREEN BORDER COLOR

Register Type: Read/Write
Read Port: 3C1, Index 11h
Write Port: 3C0, Index 11h
Default: 00h
D[7:6] Reserved
D[5:0] Palette Entry

5.5.5 AR12: COLOR PLANE ENABLE REGISTER

Register Type: Read/Write
Read Port: 3C1, Index 12h
Write Port: 3C0, Index 12h
Default: 00h
D[7:6] Reserved
D[5:4] Display Status MUX Bit[1:0]
These bits select two of the eight bits color outputs to be available in the status register. The output color combinations available on the status bits are as follows:

Table 5.5-2 Table for Video Read-back Through Diagnostic Bit (I)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1 (REFER TO 7.1.4)	
D5	D4	D5	D4
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Unused	Unused

Table 5.5-3 Table for Video Read-back Through Diagnostic Bit (II)

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1 (REFER TO 7.1.4)	
D5	D4	D5	D4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

D[3:0] Enable Color Plane Bit[3:0]

5.5.6 AR13: PIXEL PANNING REGISTER

Register Type: Read/Write
Read Port: 3C1, Index 13h
Write Port: 3C0, Index 13h
Default: 00h
D[7:4] Reserved
D[3:0] Pixel Pan Bit[3:0]
This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

Table 5.5-4 Table of Pixel Panning

D3	D2	D1	D0	MONOCHROME TEXT	VGA MODE 13	ALL OTHERS
0	0	0	0	8	0	0
0	0	0	1	0	Invalid	1
0	0	1	0	1	1	2
0	0	1	1	2	Invalid	3
0	1	0	0	3	2	4
0	1	0	1	4	Invalid	5
0	1	1	0	5	3	6
0	1	1	1	6	Invalid	7
1	0	0	0	7	Invalid	Invalid
1	0	0	1	Invalid	Invalid	Invalid
1	0	1	0	Invalid	Invalid	Invalid
1	0	1	1	Invalid	Invalid	Invalid
1	1	0	0	Invalid	Invalid	Invalid
1	1	0	1	Invalid	Invalid	Invalid
1	1	1	0	Invalid	Invalid	Invalid
1	1	1	1	Invalid	Invalid	Invalid

5.5.7 AR14: COLOR SELECT REGISTER

Register Type: Read/Write
Read Port: 3C1, Index 14h
Write Port: 3C0, Index 14h
Default: 00h
D[7:4] Reserved

D[3:2] Color Bit[7:6]
These two bits are concatenated with the six bits from the Palette Register to form the address into the LUT and to drive P[7:6].
D[1:0] Color Bit[5:4]
If AR10 D7 is programmed to a '1', these two bits replace the corresponding two bits from the Palette Register to form the address into the LUT and to drive P[5:4]. If AR10 D7 is programmed to a '0', these two bits are ignored.

5.6 COLOR REGISTERS

5.6.1 DAC STATUS REGISTER

Register Type: Read Only
Read Port: 3C7
Default: 00h
D[7:2] Reserved
D[1:0] DAC State Bit[1:0]
00: Write Operation in progress
11: Read Operation in progress

5.6.2 DAC INDEX REGISTER (READ MODE)

Register Type: Write Only
Write Port: 3C7
Default: 00h
D[7:0] DAC Index Bit[7:0]

5.6.3 DAC INDEX REGISTER (WRITE MODE)

Register Type: Read/Write
Read/Write Port: 3C8
Default: 00h
D[7:0] DAC Index Bit[7:0]

5.6.4 DAC DATA REGISTER

Register Type: Read/Write
Read/Write Port: 3C9
Default: 00h
When SR7 D2 = 1
D[7:6] Reserved
D[5:0] DAC Data [5:0]
Before writing to this register, 3C8h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue values for the DAC entry are written. After the third value is written, the values are transferred to the LUT and the DAC index is incremented in case new values for the next DAC index are to be written.
Before reading from this register, 3C7h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue value for the DAC entry may be read from this DAC index. After the third value is read, the

DAC index is incremented in case the value for the next DAC index to be read.
When SR7 D2 = 0

D[7:0] DAC Data [7:0]

When SR7 D2 = 0, the 24-bit LUT is enabled. This LUT can translate the R, G, B values into new R, G, B values independently. This LUT can be used for performing GAMMA correction function. The programming procedure is same as standard LUT when SR7 D2 = 1.

5.6.5 PEL MASK REGISTER

Register Type: Read/Write
Read/Write Port: 3C6
Default: 00h
D[7:0] Pixel Mask Bit[7:0]
This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.

5.7 EXTENDED REGISTERS

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h
D[7:6] Reserved
D[5:0] Extended Register Index Bit[5:0] (05h ~ 3Fh)

Table 5.7-1 Table of Extended Registers

INDEX (3C4)	EXTENDED ENHANCED REGISTER (3C5)
05h	Extended Password/Identification Register
06h	Extended graphics mode register
07h	RAMDAC control register
08h	CRT threshold register I
09h	CRT threshold register II
0Ah	Extended vertical overflow register
0Bh	Extended horizontal overflow register I
0Ch	Extended horizontal overflow register II
0Dh	Extended CRT starting address register
0Eh	Extended CRT pitch register

0Fh	CRT misc. control register
10h	Display line width register
11h	DDC register
12h	Feature connector control register
13h	DRAM configuration setting register
14h	DRAM sizing register
15h	DRAM state machine control register
16h	DRAM refresh queue setting
17h	DRAM I/O pads setting register I
18h	DRAM timing setting register I
19h	DRAM timing setting register II
1Ah	DRAM feedback SCLK delay compensation register I
1Bh	DRAM feedback SCLK delay compensation register II
1Ch	DRAM I/O pads setting register II
1Dh	Segment Selection Overflow Register
1Eh	Module enable register
1Fh	Power management register
20h	PCI address decoder setting register
21h	AGP/PCI state machine setting register
22h	PCI controller timing register
23h	PCI timer register I
24h	PCI timer register II
25h	AGP timing register
26h	Turbo Queue base address register
27h	Turbo Queue control register
28h	Extended MCLK clock generator register I
29h	Extended MCLK clock generator register II
2Ah	Extended MCLK clock generator register III
2Bh	Extended DCLK clock generator register I

2Ch	Extended DCLK clock generator register II
2Dh	Extended DCLK clock generator register III
2Eh	Extended ECLK clock generator register I
2Fh	Extended ECLK clock generator register II
30h	Extended ECLK clock generator register III
31h	Extended clock generator misc. register
32h	Extended clock source selection register
33h	Reserved
34h	Interrupt status register
35h	Interrupt enable register
36h	Interrupt reset register
37h	Reserved
38h	Power on trapping register I
39h	Power on trapping register II
3Ah	Power on trapping register III
3Bh	Bounding option read back
3Ch	Synchronous reset register
3Dh	Testing enabling register
3Eh	Reserved
3Fh	Reserved

5.8 SiS300 EXTENDED REGISTERS

The following list is the registers of SiS300 relocate I/O:

THE INDEX PORT OF SiS300 VIDEO CAPTURE REGISTERS IS RIO+00H
THE DATA PORT OF SiS300 VIDEO CAPTURE REGISTERS IS RIO+01H
THE INDEX PORT OF SiS300 VIDEO PLAYBACK REGISTERS IS RIO+02H
THE DATA PORT OF SiS300 VIDEO PLAYBACK REGISTERS IS RIO+03H
THE INDEX PORT OF SiS300 DIGITAL VIDEO INTERFACE REGISTERS IS RIO+04H
THE DATA PORT OF SiS300 DIGITAL VIDEO INTERFACE REGISTERS IS RIO+05H
THE INDEX PORT OF SiS301 TV ENCODER REGISTERS IS RIO+10H
THE DATA PORT OF SiS301 TV ENCODER REGISTERS IS RIO+11H
THE INDEX PORT OF SiS301 MACROVISON™ REGISTERS IS RIO+12H
THE DATA PORT OF SiS301 MACROVISON™ REGISTERS IS RIO+13H

THE INDEX PORT OF SiS301 VGA2 REGISTERS IS RIO+0014H
THE DATA PORT OF SiS301 VGA2 REGISTERS IS RIO+0015H
THE SiS301 PALETTE ADDRESS PORT REGISTER IS RIO+0016H
THE SiS301 PALETTE DATA PORT REGISTER IS RIO+0017H
"RIO" IS THE CONFIGURATION SPACE BASE ADDRESS REGISTER CNFG18 D[15:0] VALUE

5.9 VIDEO CAPTURE INDEX REGISTER

Register Type: Read/Write
Read/Write Port: 0000
Default: RIO+00h
D[7:0] Video capture register index Bit[7:0] (00h ~ 43h)

Table 5.9-1 Table of Video Capture Registers

INDEX (RIO+00)	VIDEO CAPTURE REGISTER (RIO+01)
00h	Video Capture Horizontal Start Register
01h	Video Capture Horizontal End Register
02h	Video Capture Horizontal Display Overflow Register
03h	Vertical Blanking Interval Horizontal Start Register
04h	Vertical Blanking Interval Horizontal End Register
05h	Vertical Blanking Interval Horizontal Display Overflow Register
06h	Video Capture Vertical Start Register
07h	Video Capture Vertical End Register
08h	Video Capture Vertical Display Overflow Register
09h	Vertical Blanking Interval Vertical Start Register
0Ah	Vertical Blanking Interval Vertical End Register
0Bh	Video Blanking Interval Vertical Display Overflow Register
0Ch	Video Capture Horizontal Down Scaling Factor Register
0Dh	Vertical Blanking Interval Horizontal Down Scaling Factor Register
0Eh	Video Capture Horizontal Down Scaling Factor Overflow Register
0Fh	Video Capture Vertical Down Scaling Factor Register

10h	Video Capture Vertical Down Scaling Factor Overflow Register
11h	Vertical Blanking Interval Vertical Down Scaling Factor Register
12h	Video Capture Y Frame Buffer Offset Register
13h	Video Capture UV Frame Buffer Offset Register
14h	Vertical Blanking Interval Frame Buffer Offset Register
15h	Video Capture Frame Buffer Offset Overflow Register
16h	Video Capture Frame Buffer Y1 Starting Address Low Register
17h	Video Capture Frame Buffer Y1 Starting Address Middle Register
18h	Video Capture Frame Buffer Y1 Starting Address High Register
19h	Video Capture Frame Buffer Y2 Starting Address Low Register
1Ah	Video Capture Frame Buffer Y2 Starting Address Middle Register
1Bh	Video Capture Frame Buffer Y2 Starting Address High Register
1Ch	Video Capture Frame Buffer Y3 Starting Address Low Register
1Dh	Video Capture Frame Buffer Y3 Starting Address Middle Register
1Eh	Video Capture Frame Buffer Y3 Starting Address High Register
1Fh	Video Capture Frame Buffer U1 Starting Address Low Register
20h	Video Capture Frame Buffer U1 Starting Address Middle Register
21h	Video Capture Frame Buffer U1 Starting Address High Register
22h	Video Capture Frame Buffer U2 Starting Address

	Low Register
23h	Video Capture Frame Buffer U2 Starting Address Middle Register
24h	Video Capture Frame Buffer U2 Starting Address High Register
25h	Video Capture Frame Buffer U3 Starting Address Low Register
26h	Video Capture Frame Buffer U3 Starting Address Middle Register
27h	Video Capture Frame Buffer U3 Starting Address High Register
28h	Video Capture Frame Buffer V1 Starting Address Low Register
29h	Video Capture Frame Buffer V1 Starting Address Middle Register
2Ah	Video Capture Frame Buffer V1 Starting Address High Register
2Bh	Video Capture Frame Buffer V2 Starting Address Low Register
2Ch	Video Capture Frame Buffer V2 Starting Address Middle Register
2Dh	Video Capture Frame Buffer V2 Starting Address High Register
2Eh	Video Capture Frame Buffer V3 Starting Address Low Register
2Fh	Video Capture Frame Buffer V3 Starting Address Middle Register
30h	Video Capture Frame Buffer V3 Starting Address High Register
31h	Video Capture Frame Buffer VBI1 Starting Address Low Register
32h	Video Capture Frame Buffer VBI1 Starting Address Middle Register
33h	Video Capture Frame Buffer VBI1 Starting Address High Register

34h	Video Capture Frame Buffer VBI2 Starting Address Low Register
35h	Video Capture Frame Buffer VBI2 Starting Address Middle Register
36h	Video Capture Frame Buffer VBI2 Starting Address High Register
37h	Video Capture Frame Buffer Starting Address Low Register
38h	Video Capture Frame Buffer Starting Address High Register
39h	Video Capture Frame Buffer End Address Low Register
3Ah	Video Capture Frame Buffer End Address High Register
3Bh	Video Capture Assigned Interrupt Line Register
3Ch	Video Capture FIFO Threshold High Register
3Dh	Video Capture I/O Format Register
3Eh	Frame Buffer Number Select and Video Control Register
3Fh	Video Capture Internal Field Counter Low Register
40h	Video Capture Internal Field Counter Middle Register
41h	Video Capture Internal Field Counter High Register
42h	Video Capture Current Line Counter Register
43h	Video Capture Read Back Register

5.10 VIDEO PLAYBACK INDEX REGISTER

Register Type: Read/Write
Read/Write Port: RIO+02
Default: 00h
D[7:0] Video playback register index Bit[7:0] (00h ~ 65h)

Table 5.10-1 Table of Video Playback Registers

INDEX (RIO+02)	VIDEO PLAYBACK REGISTER (RIO+03)
00h	Password/Identification Register
01h	Video Window Horizontal Display Start Low Register
02h	Video Window Horizontal Display End Low Register
03h	Video Window Horizontal Display Start/End High Register
04h	Video Window Vertical Display Start Low Register
05h	Video Window Vertical Display End Low Register
06h	Video Window Vertical Display Start/End High Register
07h	Video Display/Y Plane Frame Buffer Starting Address Low Register
08h	Video Display/Y Plane Frame Buffer Starting Address Middle Register
09h	Video Display/Y Plane Frame Buffer Starting Address High Register
0Ah	Video U Plane Frame Buffer Starting Address Low Register
0Bh	Video U Plane Frame Buffer Starting Address Middle Register
0Ch	Video U Plane Frame Buffer Starting Address High Register
0Dh	Video V Plane Frame Buffer Starting Address Low Register
0Eh	Video V Plane Frame Buffer Starting Address Middle Register
0Fh	Video V Plane Frame Buffer Starting Address High Register
10h	Video Display/Y Plane Frame Buffer Pitch Low Register
11h	Video UV Plane Frame Buffer Pitch Low Register
12h	Video Display/Y Plane/UV Plane Frame Buffer Pitch High Register
13h	Video Display/Y Plane Frame Buffer Preset Low Register

14h	Video Display/Y Plane Frame Buffer Preset Middle Register
15h	Video UV Plane Frame Buffer Preset Low Register
16h	Video UV Plane Frame Buffer Preset Middle Register
17h	Video Display/Y Plane/UV Plane Frame Buffer Preset High Register
18h	Video Horizontal Post Scaling Factor Fraction Low Register
19h	Video Horizontal Post Scaling Factor Fraction High Register
1Ah	Video Vertical Scaling Factor Fraction Low Register
1Bh	Video Vertical Scaling Factor Fraction High Register
1Ch	Video Horizontal/Vertical Scaling Control Register
1Dh	Video Playback Threshold Low Value Register
1Eh	Video Playback Threshold High Value Register
1Fh	Video Playback Line Buffer Maximum Size Register
20h	Video Overlay Color Key Red Minimum Value Register
21h	Video Overlay Color Key Green Minimum Value Register
22h	Video Overlay Color Key Blue Minimum Value Register
23h	Video Overlay Color Key Red Maximum Value Register
24h	Video Overlay Color Key Green Maximum Value Register
25h	Video Overlay Color Key Blue Maximum Value Register
26h	Video Chroma Key Red/Y Minimum Value Register
27h	Video Chroma Key Green/U Minimum Value Register
28h	Video Chroma Key Blue/V Minimum Value Register
29h	Video Chroma Key Red/Y Maximum Value Register
2Ah	Video Chroma Key Green/U Maximum Value Register
2Bh	Video Chroma Key Blue/V Maximum Value Register
2Ch	Video Contrast Enhancement Mean Value Sampling Rate Factor Register

2Dh	Video Brightness Value Register
2Eh	Video Contrast Enhancement Control Register
2Fh	Video Key Overlay Operation Mode Register
30h	Video Control Miscellaneous Register 0
31h	Video Control Miscellaneous Register 1
32h	Video Control Miscellaneous Register Register 2
33h	Subpicture Frame Buffer Starting Address Low Register
34h	Subpicture Frame Buffer Starting Address Middle Register
35h	Subpicture Frame Buffer Starting Address/Preset High Register
36h	Subpicture Frame Buffer Preset Low Register
37h	Subpicture Frame Buffer Preset Middle Register
38h	Subpicture Frame Buffer Pitch Register
39h	Subpicture Horizontal Scaling Factor Fraction Low Register
3Ah	Subpicture Horizontal Scaling Factor Fraction High Register
3Bh	Subpicture Vertical Scaling Factor Fraction Low Register
3Ch	Subpicture Vertical Scaling Factor Fraction High Register
3Dh	Subpicture Horizontal/Vertical Scaling Factor Integer Register
3Eh	Subpicture Threshold Value Register
3Fh	Subpicture FIFO Maximum Size Register
40h	Subpicture Color Palette Color0 Low Register
41h	Subpicture Color Palette Color0 High Register
42h	Subpicture Color Palette Color1 Low Register
43h	Subpicture Color Palette Color1 High Register
44h	Subpicture Color Palette Color2 Low Register
45h	Subpicture Color Palette Color2 High Register

46h	Subpicture Color Palette Color3 Low Register
47h	Subpicture Color Palette Color3 High Register
48h	Subpicture Color Palette Color4 Low Register
49h	Subpicture Color Palette Color4 High Register
4Ah	Subpicture Color Palette Color5 Low Register
4Bh	Subpicture Color Palette Color5 High Register
4Ch	Subpicture Color Palette Color6 Low Register
4Dh	Subpicture Color Palette Color6 High Register
4Eh	Subpicture Color Palette Color7 Low Register
4Fh	Subpicture Color Palette Color7 High Register
50h	Subpicture Color Palette Color8 Low Register
51h	Subpicture Color Palette Color8 High Register
52h	Subpicture Color Palette Color9 Low Register
53h	Subpicture Color Palette Color9 High Register
54h	Subpicture Color Palette ColorA Low Register
55h	Subpicture Color Palette ColorA High Register
56h	Subpicture Color Palette ColorB Low Register
57h	Subpicture Color Palette ColorB High Register
58h	Subpicture Color Palette ColorC Low Register
59h	Subpicture Color Palette ColorC High Register
5Ah	Subpicture Color Palette ColorD Low Register
5Bh	Subpicture Color Palette ColorD High Register
5Ch	Subpicture Color Palette ColorE Low Register
5Dh	Subpicture Color Palette ColorE High Register
5Eh	Subpicture Color Palette ColorF Low Register
5Fh	Subpicture Color Palette ColorF High Register
60h	MPEG Auto-Flipping Control Read-Back Register 0
61h	MPEG Auto-Flipping Control Read-Back Register 1
62h	MPEG Auto-Flipping Control Read-Back Register 2

63h	MPEG Auto-Flipping Control Read-Back Register 3
64h	MPEG Auto-Flipping Field Display Vertical Scaling Factor Fraction Low Register
65h	MPEG Auto-Flipping Field Display Vertical Scaling Factor Fraction High Register

5.11 DIGITAL VIDEO INTERFACE REGISTER

Register Type: Read/Write
Read/Write Port: RIO+04
Default: 00h
D[5:0] Digital Video Interface Register Index Bit[7:0] (00h ~ 28h)

Table 5.11-1 Table of digital video interface registers

INDEX (RIO+04)	DIGITAL VIDEO INTERFACE REGISTER (RIO+05)
00h	Function Control Register
01h	Mode Selection and FIFO Threshold High
02h	Mode Selection, PCI Bus Clock and FIFO Threshold Low
03h	FIFO Stop Operation
04h	Access Memory Starting Address High
05h	Access Memory Starting Address Median
06h	Access Memory Starting Address Low
07h	Access Memory Line Offset
08h	CRT2 Horizontal Total
09h	Overflow Register
0Ah	CRT2 Horizontal Display Enable End
0Bh	CRT2 Horizontal Retrace Start
0Ch	Overflow Register
0Dh	CRT2 Horizontal Retrace End
0Eh	CRT2 Vertical Total
0Fh	CRT2 Vertical Display Enable End
10h	CRT2 Vertical Retrace Start
11h	CRT2 Vertical Retrace End and Enable CRC Check and

	Overflow Register
12h	Hardware Cursor Test Mode and Overflow Register
13h	Software Command Reset, Panel Link Delay Compensation, Power Saving
14h	Panel Link Horizontal Retrace Start
15h	Panel Link Horizontal Retrace End/Skew
16h	Panel Link Horizontal Display Enable Start
17h	Panel Link Horizontal Display Enable End
18h	Panel Link Vertical Retrace Start
19h	Panel Link Vertical Retrace End/Misc.
1Ah	Panel Link Control Signal and Vertical Retrace Start
1Bh	Panel Link Vertical Display Enable Start
1Ch	Panel Link Vertical Display Enable End
1Dh	Panel Link Control Signal / High Bits of Vertical Display Control
1Eh	Panel Link Vertical Scaling Factor
1Fh	Panel Link DDA Operational Number In Each Horizontal Line
20h	Overflow Register
21h	Panel Link Vertical Accumulator Length
22h	Panel Link Horizontal Scaling Factor High
23h	Panel Link Horizontal Scaling Factor Low
24h	CRT2 Enable Write Register
25h	CRT2 Vertical Retrace /Display Enable
26h	CRT2 Horizontal Counter Read Back
27h	CRT2 Vertical Counter Read Back
28h	CRT2 Horizontal Display Enable and Counter Overflow Read Back

5.12 PCI CONFIGURATION REGISTERS

5.12.1 CNFG00: CONFIGURATION REGISTER 00H

Register Type: Read
Read Port: 0000h
Default: 03001039h
D[31:16] Device ID
SiS300 Device ID is 0300h
D[15:0] Vendor ID
SiS Vendor ID is 1039h

5.12.2 CNFG04: CONFIGURATION REGISTER 04H

Register Type: Read/Write
Read Port: 0004h
Default: 02200004h
If I/O pin ROMMA10 is trapped high, then
D[26:25] DEVSEL* timing (= 10, Read Only)
If I/O pin ROMMA10 is trapped low, then
D[26:25] DEVSEL* timing (= 01, Read Only)
00: fast
01: medium (fixed at this value)
10: slow
If I/O pin ROMMA7 is trapped high, then
D23 Fast back-to-back capable (=1 read only)
If I/O pin ROMMA7 is trapped low, then
D23 Fast back-to-back capable (=0 read only)
0: capable
1: not capable
D21 66 MHz Capable
0: Support 33MHz
1: Support 66 MHz (fixed at this value)
D12 Capabilities List
0: does not implement a list of capabilities
1: implements a list of capabilities
D9 Fast back-to-back enable
0: disable
1: enable
D5 VGA Palette Snoop
0: Disable
1: Enable
D3 Bus Master
0: Device is not a bus master (fixed at this value)
1: Device is a bus master
D1 Memory Space
0: Disable
1: Enable
D0 I/O Space
0: Disable

1: Enable

5.12.3 CNFG08: CONFIGURATION REGISTER 08H

Register Type: Read
Read Port: 0008h
Default: 0300000Xh
D[31:8] Class Code (= 030000h)
D[7:0] Revision ID (= 0xh)

5.12.4 CNFG10: CONFIGURATION REGISTER 10H

Register Type: Read/Write
Read Port: 0010h
Default: 00000008h
D[31:0] 32-bit memory base register for 128MB linear frame buffer

5.12.5 CNFG14: CONFIGURATION REGISTER 14H

Register Type: Read/Write
Read Port: 0014h
Default: 00000000h
D[31:0] 32-bit memory base register for 128KB memory mapped I/O

5.12.6 CNFG18: CONFIGURATION REGISTER 18H

Register Type: Read/Write
Read Port: 0018h
Default: 00000001h
D[31:0] 32-bit I/O base register for 128 I/O space

5.12.7 CNFG2C: CONFIGURATION REGISTER 2CH

Register Type: Read/Write Once Only
Read Port: 002Ch
Default: 00000000h
D[31:16] Subsystem ID
D[15:0] Subsystem Vendor ID

5.12.8 CNFG30: CONFIGURATION REGISTER 30H

Register Type: Read/Write
Read Port: 0030h
Default: 000C0000h
D[31:11] Expansion ROM Base Address
D0 ROM Enable Bit
0: Disable
1: Enable

5.12.9 CNFG3C: CONFIGURATION REGISTER 3CH

Register Type: Read/Write
Read Port: 003Ch
Default: 00000100h
If I/O pin ROMMA3 is trapped high, then
D[15:8] Interrupt Pin (= 01h, Read Only)
D[7:0] Interrupt Line (= 00h)
If I/O pin ROMMA3 is trapped low, then
D[15:8] Interrupt Pin (= 00h, Read Only)
D[7:0] Interrupt Line (= 00h)

5.13 AGP CONFIGURATION REGISTERS

Note: All the registers described in this section can be accessed only when AGP is enable.

5.13.1 CNFG34: CONFIGURATION REGISTER 34H

Register Type: Read Only
Read Port: 0034h
Default: 00000050h
D[7:0] Capabilities list offset pointer (Read Only)

5.13.2 CNFG50: CONFIGURATION REGISTER 50H

Register Type: Read Only
Read Port: 0050h
Default: 00105c02h
D[23:20] Major revision number
D[19:16] Minor revision number
D[15:8] Pointer to next item
D[7:0] Cap_ID: value 02h identifies the list item as pertaining to AGP register

5.13.3 CNFG54: CONFIGURATION REGISTER 54H

Register Type: Read Only
Read Port: 0054h
Default: 01000003h
D[31:24] Maximum number of AGP command requests
D9 Side band addressing support
0: Not support
1: Support
D1 2X mode support
0: Not support
1: Support
D0 1X mode support
0: Not support
1: Support

5.13.4 CNFG58: CONFIGURATION REGISTER 58H

Register Type: Read/Write
Read Port: 0058h
Default: 00000000h

D[31:24]	Maximum number of AGP requests can be enqueued
D9	1: sideband address mode enable 0: sideband address mode disable
D8	1: AGP enable 0: AGP disable
D1	1: 2X mode enable 0: 2X mode disable
D0	1: 1X mode enable 0: 1X mode disable

5.13.5 CNFG5C: CONFIGURATION REGISTER 5CH

Register Type: Read
Read Port: 005Ch
Default: 00000000h

D[15:8]	NULL: 00h indicates final item in the capability list

6 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Table 6.1-1 Table of Absolute Maximum Ratings

PARAMETER	MIN.	MAX.	UNIT
Ambient operation temperature	0	70	^0C
Storage temperature	-40	125	^0C
Input voltage	-0.3	OVDD+10%	V
Output voltage	-0.5	3.6	V

NOTE:

Stressing these listed above may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

6.2 DC CHARACTERISTICS1

T_A = 0 - 70 ^{0}C, OV_{DDA} = 3.3 V ± 5 %, IV_{DD} 5= 1.8 V ± 5 %,GND = 0 V

Table 6.2-1 Table of DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage	2.2	OVDD+10%	V	
V_{OL}	Output low voltage	-	0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH} = -1.0 mA
I_{IL}	Input leakage current	-	± 10	uA	
I_{OZ}	tristate leakage current	-	± 20	uA	0.45 < V_{OUT} < V_{DD}

6.3 DC CHARACTERISTICS FOR DAC (ANALOG OUTPUT CHARACTERISTICS)

Table 6.3-1 Table of DC Characteristics for DAC

DESCRIPTION	MIN	TYPICAL	MAX	UNIT
Black Level	-	0	-	V
White Level	-	700	-	mV
ILE	-1.0	-	+1.0	LSB
DLE	-0.5	-	+0.5	LSB
1 LSB	-	2.734	-	mV
Iref	-	8.40	-	mA

6.4 AC CHARACTERISTICS FOR DAC (ANALOG OUTPUT CHARACTERISTICS)

Table 6.4-1 Table of AC Characteristics for DAC

DESCRIPTION	PARAMETER	CONDITION	TYPICAL	MAX.	UNIT
Settling Time	Tsett	R=37.5 ohm C1=30 pF	-	6	ns

6.5 AC CHARACTERISTICS

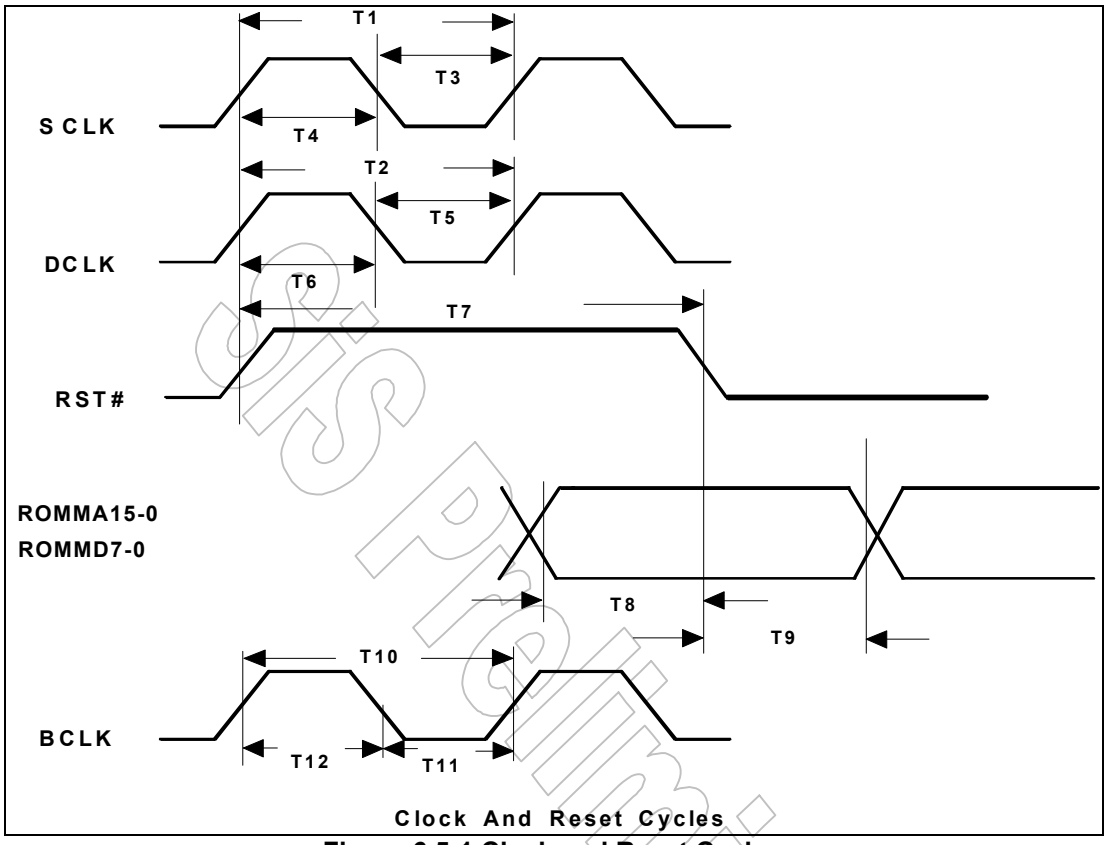

Figure 6.5-1 Clock and Reset Cycles

Table 6.5-1 Clock and Reset Timing Table

SYMBOL	PARAMETER	MIN	MAX
T_1	MCLK Period	7	
T_2	VCLK Period	3.3	
T_3	MCLK Low Time	3	
T_4	MCLK High Time	3	
T_5	VCLK Low Time	1.4	
T_6	VCLK High Time	1.4	
T_7	Reset High Time	400	
T_8	System Configuration Data Setup Time	20	
T_9	System Configuration Data Hold Time	20	
T_{10}	BCLK Period (33MHz / 66MHz)	30 /15	
T_{11}	BCLK High Time (33MHz /66MHz)	11 / 6	
T_{12}	BCLK Low Time (33MHz /66MHz)	11 / 6	

(Units: ns)

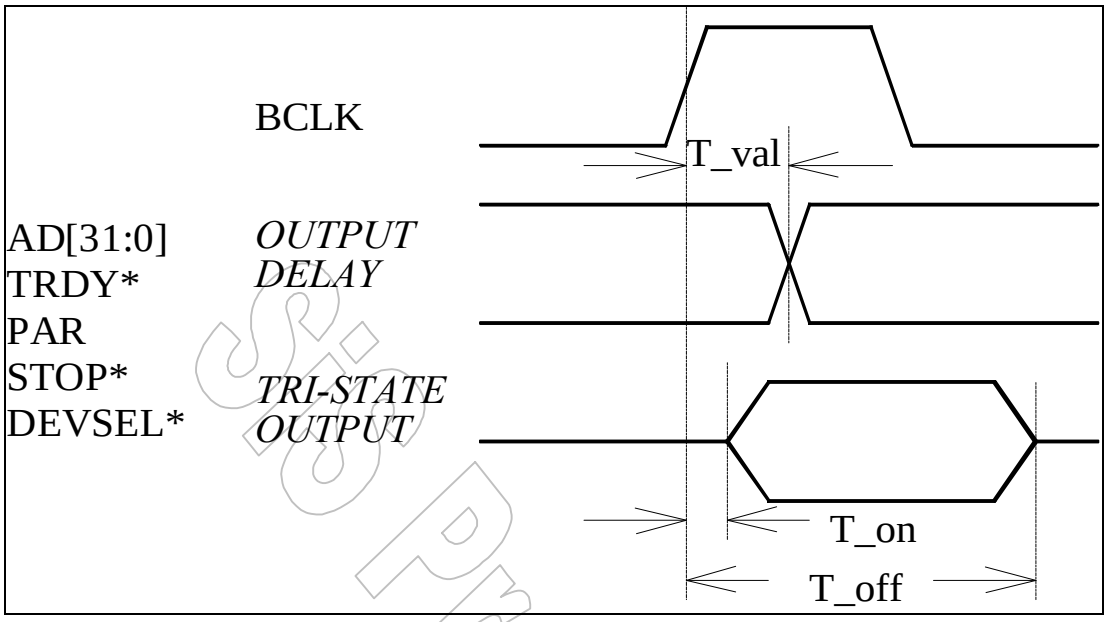

Figure 6.5-2 PCI/AGP Output and Tri-state Timing

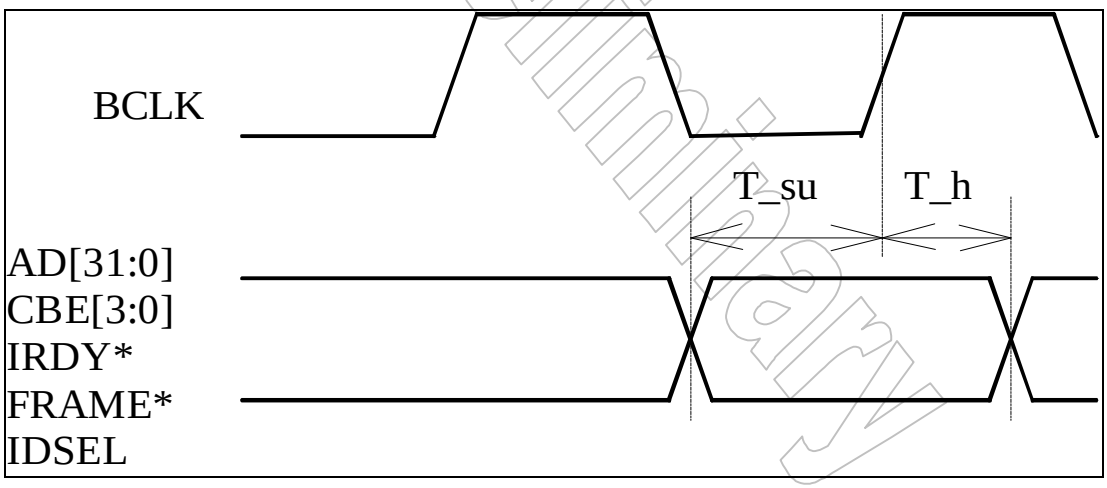

Figure 6.5-3 PCI/AGP Input Timing

Table 6.5-2 PCI Timing Table

SYMBOL	PARAMETER	66MHZ		33MHZ		UNITS
		MIN	MAX	MIN	MAX	
Tval	BCLK to Signal Valid Delay	2	6	2	11	ns
Ton	Float to Active Delay	2	-	2	-	ns
Toff	Active to Float Delay	-	14	-	28	ns
Tsu	Input Setup Time to BCLK	3	-	7	-	ns
Th	Input Hold Time from BCLK	0	-	0	-	ns

Table 6.5-3 AGP 1X Timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
Tcyc	BCLK Cycle Time	15	30	ns
Tval	BCLK to Signal Valid Delay	1.5	6	ns
Ton	Float to Active Delay	1.5	6	ns
Toff	Active to Float Delay	1	14	ns
Tsu	Input Setup Time to BCLK	5	-	ns
Th	Input Hold Time from BCLK	0.5	-	ns

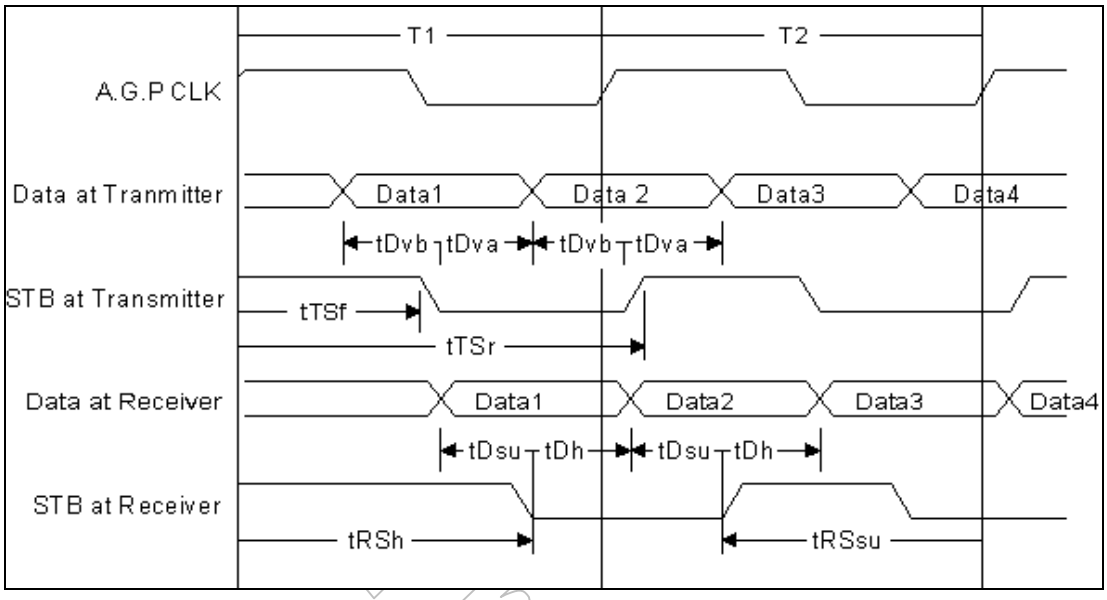

Figure 6.5-4 AGP 133 Timing Diagram

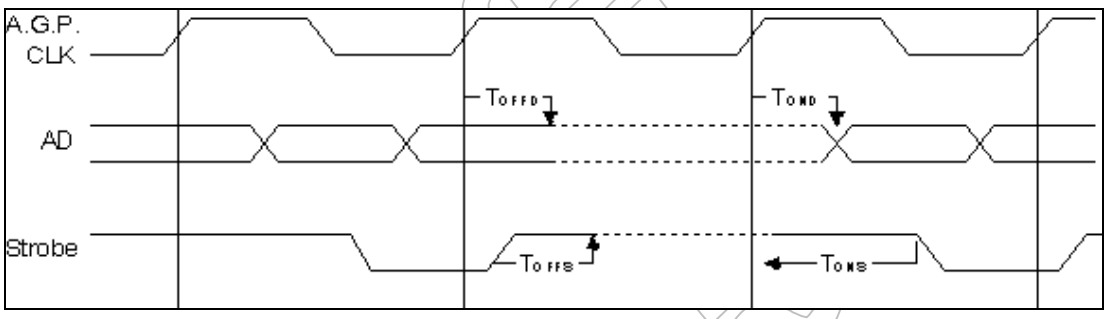

Figure 6.5-5 Strobe/Data Turnaround Timings

Table 6.5-4 AGP 2X Timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
Transmitter Output Signals:					
tTSf	CLK to transmit strobe falling	2	12	ns	
tTSr	CLK to transmit strobe rising		20	ns	
tDvb	Data valid before strobe	1.7		ns	
tDva	Data valid after strobe	1.7		ns	
tONd	Float to Active Delay	-1	9	ns	
tOFFd	Active to Float Delay	1	12	ns	
tONS	Strobe active to strobe falling edge setup	6	10	ns	
tOFFS	Strobe rising edge to strobe float delay	6	10	ns	
Receiver Input Signals:					
tRSsu	Receive strobe setup time to CLK	6		ns	
tRSh	Receive strobe hold time hold time from CLK	1		ns	
tDsu	Data to strobe setup time	1		ns	
tDh	Strobe to data hold time	1		Ns	

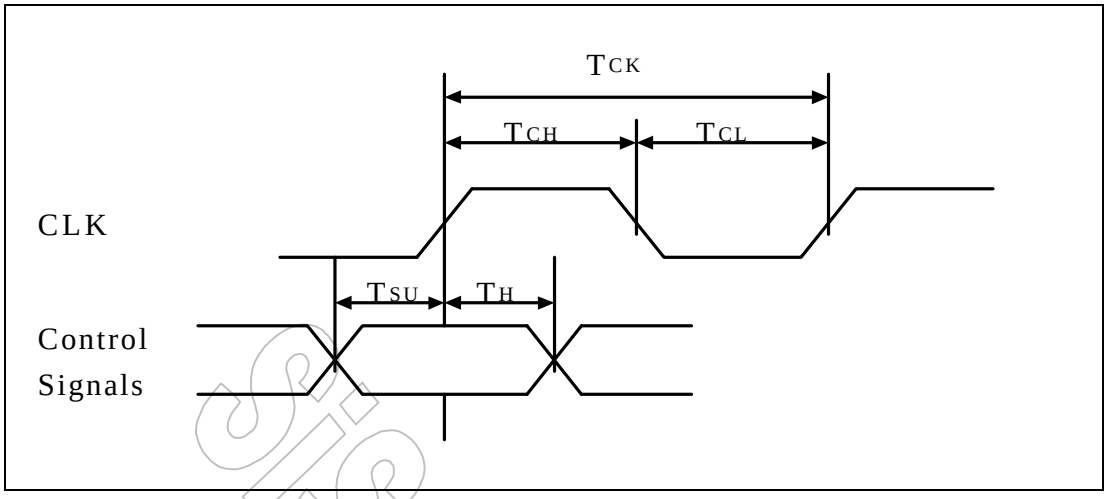

Figure 6.5-6 SDRAM/SGRAM input/output Timing

Table 6.5-5 SDRAM/SGRAM Timing Table

SYMBOL	PARAMETER		MIN	MAX.	UNITS
T_{CK}	Clock Cycle Time	latency= 3	7 (143 MHz)		ns
		latency= 2	10 (100 MHz)		ns
T_{CH}	CLK high level width		3		ns
T_{CL}	CLK low level width		3		ns
T_{SU}	Setup Timing		3.5		ns
T_H	Hold Timing		1.0		ns

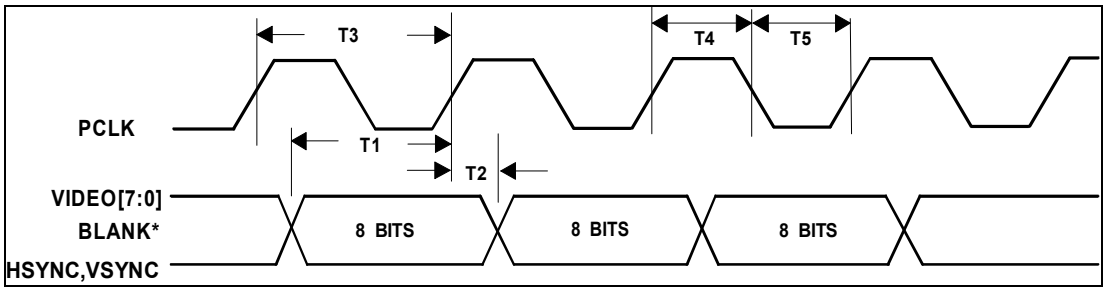

Figure 6.5-7 Video Timing 4, 8, and 16 Bits/Pixel Modes

Table 6.5-6 4, 8, and 16 BPP Video AC Timing Table

SYMBOL	PARAMETER	MIN.	MAX.	NOTES
T_1	VIDEO[7:0], BLANK*, SYNC Setup Time	10	-	
T_2	VIDEO[7:0], BLANK*, SYNC Hold Time	2	-	
T_3	PCLK Period	20	-	
T_4	PCLK High Time	7	-	
T_5	PCLK Low Time	7	-	

(Units: ns)

Digital interface signals timing

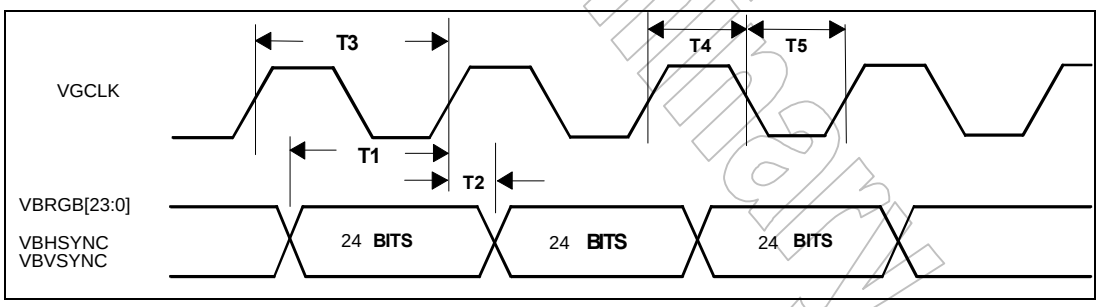

Figure 6.5-8 Figure Digital Video Timing

Table 6.5-7 Table Digital Video Interface AC Timing Table

SYMBOL	PARAMETER	MIN.	MAX.	NOTES
T_1	VBRGB[23:0], VBHSYNC, VBVSYNC Setup Time	3.0	-	-
T_2	VBRGB[23:0], VBHSYNC, VBVSYNC Hold Time	2.0	-	-
T_3	VGCLK Period	7.4	-	-
T_4	VGCLK High Time	3.0	-	-
T5	VGCLK Low Time	3.0	-	-

(Unit: ns)

7 APPENDIX A. RECOMMENDED MEMORY CONFIGURATION

Table 7-1 128-bit 4M Byte Display Memory Using 128Kx32x2-bank SGRAM

	U1	U2	U3	U4
CLK	SCLK0	SCLK1	SCLK2	SCLK3
CS#	CS#0	CS#0	CS#0	CS#0
RAS#	SRAS#	SRAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#	SCAS#	SCAS#
WE#	WE#	WE#	WE#	WE#
DQM	DQM[0:3]	DQM[4:7]	DQM[8:11]	DQM[12:15]
ADDR	MA[0:9]	MA[0:9]	MA[0:9]	MA[0:9]
DATA	DQ[0:31]	DQ[32:63]	DQ[64:95]	DQ[96:127]
CKE	VDD	VDD	VDD	VDD
DSF	DSF	DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3	0,1,2,3	0,1,2,3
Bank	0,1	0,1	0,1	0,1

Table 7-2 64-bit 2M Byte Display Memory Using 128Kx32x2-bank SGRAM

	U1	U2
CLK	SCLK0	SCLK1
CS#	CS#0	CS#0
RAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#
WE#	WE#	WE#
DQM	DQM[0:3]	DQM[4:7]
ADDR	MA[0:9]	MA[0:9]
DATA	DQ[0:31]	DQ[32:63]
CKE	VDD	VDD
DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3
Bank	0,1	1,1

Table 7-3 128-bit 8M Byte Display Memory Using 256Kx32x2-bank SGRAM

	U1	U2	U3	U4
CLK	SCLK0	SCLK1	SCLK2	SCLK3
CS#	CS#0	CS#0	CS#0	CS#0
RAS#	SRAS#	SRAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#	SCAS#	SCAS#
WE#	WE#	WE#	WE#	WE#
DQM	DQM[0:3]	DQM[4:7]	DQM[8:11]	DQM[12:15]
ADDR	MA[0:10]	MA[0:10]	MA[0:10]	MA[0:10]
DATA	DQ[0:31]	DQ[32:63]	DQ[64:95]	DQ[96:127]
CKE	VDD	VDD	VDD	VDD
DSF	DSF	DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3	0,1,2,3	0,1,2,3
Bank	0,1	0,1	0,1	0,1

Table 7-4 64-bit 4M Byte Display Memory Using 256Kx32x2-bank SGRAM

	U1	U2
CLK	SCLK0	SCLK1
CS#	CS#0	CS#0
RAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#
WE#	WE#	WE#
DQM	DQM[0:3]	DQM[4:7]
ADDR	MA[0:10]	MA[0:10]
DATA	DQ[0:31]	DQ[32:63]
CKE	VDD	VDD
DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3
Bank	0,1	1,1

Table 7-5 128-bit 16M Byte Display Memory Using 2x256Kx32x2-bank SGRAM

	U1	U2	U3	U4
CLK	SCLK0	SCLK1	SCLK2	SCLK3
CS#	CS#0,CS#1	CS#0,CS#1	CS#0,CS#1	CS#0,CS#1
RAS#	SRAS#	SRAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#	SCAS#	SCAS#
WE#	WE#	WE#	WE#	WE#
DQM	DQM[0:3]	DQM[4:7]	DQM[8:11]	DQM[12:15]
ADDR	MA[0:10]	MA[0:10]	MA[0:10]	MA[0:10]
DATA	DQ[0:31]	DQ[32:63]	DQ[64:95]	DQ[96:127]
CKE	VDD	VDD	VDD	VDD
DSF	DSF	DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3	0,1,2,3	0,1,2,3
Bank	0,1	0,1	0,1	0,1

Table 7-6 64-bit 8M Byte Display Memory Using 2x256Kx32x2-bank SGRAM

	U1	U2
CLK	SCLK0	SCLK1
CS#	CS#0,CS#1	CS#0,CS#1
RAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#
WE#	WE#	WE#
DQM	DQM[0:3]	DQM[4:7]
ADDR	MA[0:10]	MA[0:10]
DATA	DQ[0:31]	DQ[32:63]
CKE	VDD	VDD
DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3
Bank	0,1	1,1

Table 7-7 128-bit 16M Byte Display Memory Using 256Kx32x4-bank SGRAM

	U1	U2	U3	U4
CLK	SCLK0	SCLK1	SCLK2	SCLK3
CS#	CS#0	CS#0	CS#0	CS#0
RAS#	SRAS#	SRAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#	SCAS#	SCAS#
WE#	WE#	WE#	WE#	WE#
DQM	DQM[0:3]	DQM[4:7]	DQM[8:11]	DQM[12:15]
ADDR	MA[0:11]	MA[0:11]	MA[0:11]	MA[0:11]
DATA	DQ[0:31]	DQ[32:63]	DQ[64:95]	DQ[96:127]
CKE	VDD	VDD	VDD	VDD
DSF	DSF	DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3	0,1,2,3	0,1,2,3
Bank	0,1	0,1	0,1	0,1

Table 7-8 64-bit 8M Byte Display Memory Using 256Kx32x4-bank SGRAM

	U1	U2
CLK	SCLK0	SCLK1
CS#	CS#0	CS#0
RAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#
WE#	WE#	WE#
DQM	DQM[0:3]	DQM[4:7]
ADDR	MA[0:11]	MA[0:11]
DATA	DQ[0:31]	DQ[32:63]
CKE	VDD	VDD
DSF	DSF	DSF
PLANE	0,1,2,3	0,1,2,3
Bank	0,1	1,1

Table 7-9 128-bit 16M Byte Display Memory Using 512Kx16x2-bank SDRAM

	U1	U2	U3	U4	U5	U6	U7	U8
CLK	SCLK0	SCLK0	SCLK1	SCLK1	SCLK2	SCLK2	SCLK3	SCLK3
CS#	CS#0	CS#0	CS#0	CS#0	CS#0	CS#0	CS#0	CS#0
RAS#	SRAS#	SRAS#	SRAS#	SRAS#	SRAS#	SRAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#	SCAS#	SCAS#	SCAS#	SCAS#	SCAS#	SCAS#
WE#	WE#	WE#	WE#	WE#	WE#	WE#	WE#	WE#
DQM	DQM[0:1]	DQM[2:3]	DQM[4:5]	DQM[6:7]	DQM[8:9]	DQM[10:11]	DQM[12:13]	DQM[14:15]
ADDR	MA[0:11]	MA[0:11]	MA[0:11]	MA[0:11]	MA[0:11]	MA[0:11]	MA[0:11]	MA[0:11]
DATA	DQ[0:15]	DQ[16:31]	DQ[32:47]	DQ[48:63]	DQ[64:79]	DQ[80:95]	DQ[96:111]	DQ[112:127]
CKE	CKE	CKE	CKE	CKE	CKE	CKE	CKE	CKE
PLANE	0,1	2,3	0,1	2,3	0,1	2,3	0,1	2,3
Bank	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1

Table 7-10 64-bit 8M Byte Display Memory Using 512Kx16x2-bank SDRAM

	U1	U2	U3	U4
CLK	SCLK0	SCLK0	SCLK1	SCLK1
CS#	CS#0	CS#0	CS#0	CS#0
RAS#	SRAS#	SRAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#	SCAS#	SCAS#
WE#	WE#	WE#	WE#	WE#
DQM	DQM[0:1]	DQM[2:3]	DQM[4:5]	DQM[6:7]
ADDR	MA[0:11]	MA[0:11]	MA[0:11]	MA[0:11]
DATA	DQ[0:15]	DQ[16:31]	DQ[32:47]	DQ[48:63]
CKE	CKE	CKE	CKE	CKE
PLANE	0,1	2,3	0,1	2,3
Bank	0,1	0,1	0,1	0,1

Table 7-11 128-bit 64M Byte Display Memory Using 1Mx16x4-bank SDRAM

	U1	U2	U3	U4	U5	U6	U7	U8
CLK	SCLK 0	SCLK 0	SCLK 1	SCLK 1	SCLK 2	SCLK 2	SCLK 3	SCLK 3
CS#	CS#0	CS#0	CS#0	CS#0	CS#0	CS#0	CS#0	CS#0
RAS#	SRAS #	SRAS #	SRAS #	SRAS #	SRAS #	SRAS #	SRAS #	SRAS #
CAS#	SCAS #	SCAS #	SCAS #	SCAS #	SCAS #	SCAS #	SCAS #	SCAS #
WE#	WE#	WE#	WE#	WE#	WE#	WE#	WE#	WE#
DQM	DQM [0:1]	DQM [2:3]	DQM [4:5]	DQM [6:7]	DQM [8:9]	DQM [10:11]	DQM [12:13]	DQM [14:15]
ADDR	MA[0:12] CS#1	MA[0:12] CS#1	MA[0:12] CS#1	MA[0:12] CS#1	MA[0:12] CS#1	MA[0:12] CS#1	MA[0:12] CS#1	MA[0:12] CS#1
DATA	DQ [0:15]	DQ [16:31]	DQ [32:47]	DQ [48:63]	DQ [64:79]	DQ [80:95]	DQ [96:111]	DQ [112:127]
CKE	CKE	CKE	CKE	CKE	CKE	CKE	CKE	CKE
PLANE	0,1	2,3	0,1	2,3	0,1	2,3	0,1	2,3
Bank	0,1	0,1	0,1	0,1	0,1	0,1	0,1	0,1

Table 7-12 64-bit 32M Byte Display Memory Using 1Mx16x4-bank SDRAM

	U1	U2	U3	U4
CLK	SCLK0	SCLK0	SCLK1	SCLK1
CS#	CS#0	CS#0	CS#0	CS#0
RAS#	SRAS#	SRAS#	SRAS#	SRAS#
CAS#	SCAS#	SCAS#	SCAS#	SCAS#
WE#	WE#	WE#	WE#	WE#
DQM	DQM[0:1]	DQM[2:3]	DQM[4:5]	DQM[6:7]
ADDR	MA[0:12] CS#1	MA[0:12] CS#1	MA[0:12] CS#1	MA[0:12] CS#1
DATA	DQ[0:15]	DQ[16:31]	DQ[32:47]	DQ[48:63]
CKE	CKE	CKE	CKE	CKE
PLANE	0,1	2,3	0,1	2,3
Bank	0,1	0,1	0,1	0,1

8 APPENDIX B. SIS300 MECHANICAL DIMENSION

SiS300 365 balls BGA package Unit: mm

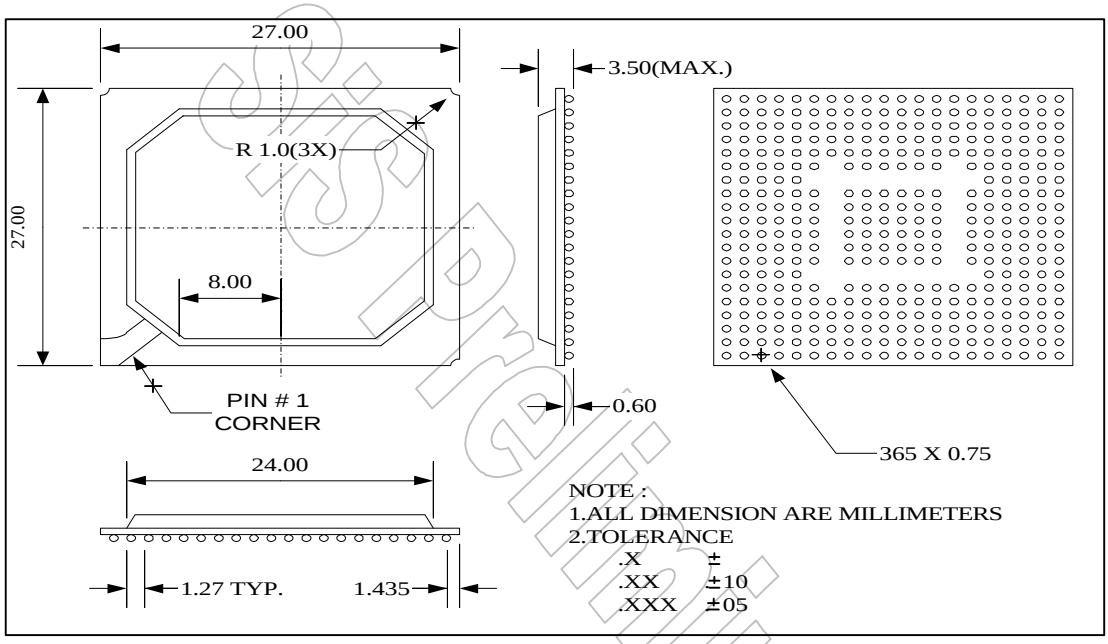

Figure 8-3 SiS300 365 balls BGA package

9 FIG SiS300 PIN NAME LOCATION AND BALL MAP

	1	2	3	4	5	6	7	8	9	10
A	REFOS	VBRCLK	ROMW	VBHCLK	VBBLANK#	ROMMA1	ROMMA	ROMMA	ROMM	ROMM
B	RSET	REFOSC	ENTEST	VBCAD	VBHSYNC	ROMMA1	ROMMA	ROMMA	ROMM	ROMM
C	B	VREF	COMP	DDCCLK	VBVSYNC	VGCLK	ROMMA	ROMMA	ROMM	ROMM
D	R	G	AVDD4	AVDD1	HSYNC	VBCLK	DDCDA	ROMMD	ROMM	ROMM
E	ST0	REQ#	BCLK	INTA#	AVDD3	VSYNC	ROMCS	ROMMD	ROMM	ROMM
F	RBF#	ST2	ST1	RST#	GNT#	P5		P4	P4	P1
G	SBA2	SBA0	SBA3	SBA1	WBF#					
H	SBA4	SB_STB	SBA7	SBA5	SB_STB#	P1		VSS	VSS	VSS
J	SBA6	AD31	AD30	AD28	AD26	P2		VSS	VSS	VSS
K	AD29	AD27	AD24	AD_STB	C/BE#3	P2		VSS	VSS	VSS
L	AD25	AD_STB1	AD22	AD20	AD18	P1		VSS	VSS	VSS
M	AD23	AD21	AD19	AD16	FRAME#	P2		VSS	VSS	VSS
N	AD17	C/BE#2	TRDY#	STOP#	PAR	P1		VSS	VSS	VSS
P	IRDY#	DEVSEL#	AD15	AD13	AD11	P1				
R	C/BE#1	AD14	AD9	C/BE#0	AD_STB#0	P5		P3	P1	P3
T	AD12	AD10	AD6	AD4	AGPVREF	AVDD5	DQ11	DQ14	DQ24	DQ27
U	AD8	AD_STB0	AD2	AD0	DQM#1	DQ8	DQ10	DQ13	DQM#3	DQ26
V	AD7	AD5	AVDD2	DQ20	DQM#0	SCLK0	DQ9	DQ12	DQ15	DQ25
W	AD3	AD1	DQ22	DQ19	DQ17	DQ7	DQ5	DQ3	DQ1	DQ55
Y	DQM#2	DQ23	DQ21	DQ18	DQ16	DQ6	DQ4	DQ2	DQ0	DQM#6

11	12	13	14	15	16	17	18	19	20
ROMM	VIDEO7	VIDEO4	VIDEO1	DQ127	DQ124	DQ121	DQ96	DQ97	DQ98
ROMM	VIDEO6	VIDEO3	VIDEO0	DQ126	DQ123	DQ120	DQ99	DQ100	DQ101
ROMO	VIDEO5	VIDEO2	EVIDEO	DQ125	DQ122	DQM#15	DQM#12	DQ102	DQ103
ROMM	PCLK	EVDCLK	DQ111	DQ109	DQ107	DQ105	DQ112	DQ113	DQ114
ROMM	BLANK#	ESYNC	DQ110	DQ108	DQ106	DQ104	DQ115	DQ116	DQ117
P4	P1	P4		P5	DQM#13	SCLK3	DQ118	DQ119	DQM#14
					DQ95	DQ94	DQ93	DQ64	DQ65
VSS	VSS	VSS		P1	DQ92	DQ91	DQ90	DQ66	DQ67
VSS	VSS	VSS		P3	DQ89	DQ88	DQM#11	DQ68	DQ69
VSS	VSS	VSS		P1	DQ78	DQ79	DQM#8	DQ70	DQ71
VSS	VSS	VSS		P3	DQ76	DQ77	DQ80	DQ81	DQ82
VSS	VSS	VSS		P1	DQ73	DQ74	DQ75	DQ83	DQ84
VSS	VSS	VSS		P3	CKE#	DQM#9	DQ72	DQ85	DQ86
					MA12	MA11	SCLK2	DQ87	DQM#10
P1	P3	P1		P5	MA8	MA7	CS1#	SCAS#	WE#
DQ30	DQM#5	DQ41	DQ43	DQ46	DQ56	MA6	MA5	CS0#	SRAS#
DQ29	SCLK1	DQ40	DQ42	DQ45	DQM#7	DQ58	MA4	MA9	MA10
DQ28	DQ31	DQ48	DQM#4	DQ44	DQ47	DQ57	MA2	MA1	MA0
DQ53	DQ51	DQ49	DQ38	DQ36	DQ34	DQ32	DQ60	DQ62	MA3
DQ54	DQ52	DQ50	DQ39	DQ37	DQ35	DQ33	DQ59	DQ61	DQ63

P1: IVDD (1.8V)

P2: OVDDA (AGP QVDD power)(3.3V/1.5V)

P3: OVDDM (DRAM power) (3.3V/2.5V)

P4: OVDD3 (3.3V)

P5: PVDD (3.3V)

AVDD1, AVDD2, AVDD3, AVDD4, AVDD5: analog power (3.3V)

Total: 300 signals + 36 VSS + 29 VDD = 365 balls