TC160G CMOS Gate Array

0.8 micron

MAY 8 1991

Description

The TC160G series of double-layer* metal, 0.8 micron gate arrays has a 0.3ns gate speed and up to 120K** useable gates—one of the highest in the industry.

— Achieve a higher gate density in plastic packages
— Compatible with the TC110G, TC120G, TC140G and TC150G gate arrays

The TC160G is formed with a sea-of-gates architecture that when used in conjunction with our double-layer wiring technology makes highly efficient use of silicon.

The TC160G is supported by the Toshiba Design Environment which embraces popular EWS and CAE systems. Toshiba has ASIC design centers around the United States and Canada to provide in-depth technical support.

* Triple layer metal is under development

** Gate utilization is dependent on design.

Features

- Process: 0.8 micron (drawn) CMOS Si-gate double layer metal
- Raw gates: 33K to 302K
- Usable gates: up to 120K
- Gate speed: 0.3ns (2-input NAND gate, fanout - 2, tpd.) equivalent to 100K ECL
- Maximum toggle frequency: >250 MHz, ultra-high speed
- I/O pads: up to 416 wire bond
- Output drive: up to 24mA
- Advanced packaging techniques: I/O cells are TAB compatible
- More flexible utilization of I/O: so even a high current driver only takes one bonding position
- Programmable I/O cells: with slew rate control
- Functional blocks of megacells and megafunctions
  - — Multiplier, barrelshifter, ALU
  - — LSI/VLSI CPU peripheral
  - — 2900 family
- Building-block memory (32 to 16K bit)
  - — RAMs
  - — ROMs

Product Lines

Part Number	Gate [1] Complexity	Estimated [2] Usable Gates	Maximum I/O Pads [3] Wire bond
TC160GU2	302,000	120,000	416 [4]
TC160GN5	235,000	94,000	368 [4]
TC160GH7	177,000	71,000	320 [4]
TC160GD2	132,000	53,000	280 [4]
TC160GA8	108,000	43,000	256
TC160G70	70,000	28,000	208
TC160G54	54,000	22,000	184
TC160G41	41,000	17,000	160
TC160G33	33,000	13,000	144

Notes: 1. Raw-gates.
2. Based on 40% array utilization. Actual utilization varies, depending on circuit configuration.
3. Additional I/O pads may be configured as V_{DD}/V_{SS}, subject to number and drive of output buffers.
4. I/O signals presently limited to 256 by tester capability. Special test methodologies are available for higher pin count.

TAEC

Absolute Maximum Ratings (V_{SS} = 0V)

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	– 0.3 to +7.0	V
V_{IN}	DC input voltage	– 0.3 to V_{DD} +0.3	V
I_{IN}	DC input current	± 10	mA
T_{stg}	Storage temperature	– 40 to +125	°C

Recommended Commercial Operating Conditions (V_{SS} = 0V)

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	4.75 to 5.25	V
T_a	Ambient temperature	0 to +70	°C

DC Electrical Characteristics

Specified at V_{DD} = 5V ±5%, ambient temperature 0 to +70°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage					V
	TTL level		2.2			
	TTL level SCHMITT trigger		2.2			
	CMOS level		3.5			
	CMOS level SCHMITT trigger		4.0			
V_{IL}	Low level input voltage					V
	TTL level				0.8	
	TTL level SCHMITT trigger				0.8	
	CMOS level				1.5	
	CMOS level SCHMITT trigger				1.0	
I_{IH}	High level input current	$V_{IN} = V_{DD}$	– 10		10	µA
	Input buffer with pull-down	$V_{IN} = V_{DD}$	10		200	
I_{IL}	Low level input current	$V_{IN} = V_{SS}$	– 10		10	µA
	Input buffer with pull-up	$V_{IN} = V_{SS}$	– 200		– 10	
V_{OH}	High level output voltage					V
	Type B1	I_{OH} = – 1mA	2.4			
	Type B2	I_{OH} = – 2mA	2.4			
	Type B4	I_{OH} = – 4mA	2.4			
	Type B8	I_{OH} = – 8mA	2.4			
	Type B16	I_{OH} = – 16mA	2.4			
	Type B24	I_{OH} = – 24mA	2.4			
		I_{OH} = – 1µA	V_{DD} – 0.05			
V_{OL}	Low level output voltage					V
	Type B1	I_{OL} = 1mA			0.4	
	Type B2	I_{OL} = 2mA			0.4	
	Type B4	I_{OL} = 4mA			0.4	
	Type B8	I_{OL} = 8mA			0.4	
	Type B16	I_{OL} = 16mA			0.4	
	Type B24	I_{OL} = 24mA			0.4	
		I_{OL} = 1µA			V_{SS} + 0.05	
I_{OZ}	High impedance leakage current		– 10		10	µA
	Output buffer with pull-up	$V_{OUT} = V_{DD}$ or V_{SS}	– 200		– 10	
	Output buffer with pull-down	$V_{OUT} = V_{DD}$ or V_{SS}	10		200	
VH	SCHMITT trigger hysteresis voltage					V
	TTL level			0.3		
	CMOS level			1.4		
I_{DD}	Quiescent supply current	$V_{IN} = V_{DD}$ or V_{SS}			100(1)	µA

Note: (1) Customer-design dependent.

TC160G Series Library (Preliminary)

TC110G, TC120G, TC140G, TC150G series-compatible macrocells and macrofunctions
- Macrocell performance optimization (standard/high drive)
- Macrocell equivalent to SSI/MSI

Functional blocks of Megacells, Megafunctions
- Multiplier, Barrelshifter, ALU
- LSI/VLSI CPU peripheral
- 2900 family

Building-block memory (32 to 16K bit)
- RAM cell
- ROM cell
- Customer-defined architecture

Macrocells

Two drive options, standard drive and power drive, are available

Logic gate	62
Inverter/internal buffer	24
Tri-state internal buffer	6
Delay buffer	6
Latch	21
Flip-flop	50
Decoder	8
Multiplexer	14
Adder	6
Input buffer	66
Output buffer	34
Bidirectional buffer	432
Oscillator	8
Total	**737**

Macrofunction List

Function	Types	
	74HC Series Compatible	Other
Adders	1	4
Comparators	2	6
Counters	11	19
Decoders	4	10
Flip-Flops	6	—
Gates	16	—
Multiplexers	10	11
Registers	16	19
Others	7	8
Total	**73**	**77**

RAM

RAM-C single port RAM
- Asynchronous
- Separated I/O, 3 state output
- Max. 4608 bit/block (8 ~ 256 word × 4 ~ 36 bit)
- Read access time (t_{ACC}) 6ns typ.

RAM-E triple port RAM
- Asynchronous
- 2 read 1 write
- Max. 2304 bit/block (16 ~ 64 word × 4 ~ 36 bit)
- Read access time (t_{ACC}) 5ns typ.

ROM

ROM-A/B single port ROM
- Asynchronous
- Max. 16384 bit/block (64 ~ 1024 word × 2 ~ 32 bit)
- Read access time (t_{ACC}) 10ns/14ns typ.

Megafunction (under development)

XADD32
- 32-bit binary full adder
- 830 gates (max.)

XALU32
- 32-bit ALU
- 1090 gates (max.)

XMPY8
- 8 x 8 bit parallel multiplier
- 980 gates (max.)

XMPY16
- 16 x 16 bit parallel multiplier
- 3020 gates (max.)

XBRL16
- 16-bit barrel shifter
- 320 gates (max.)

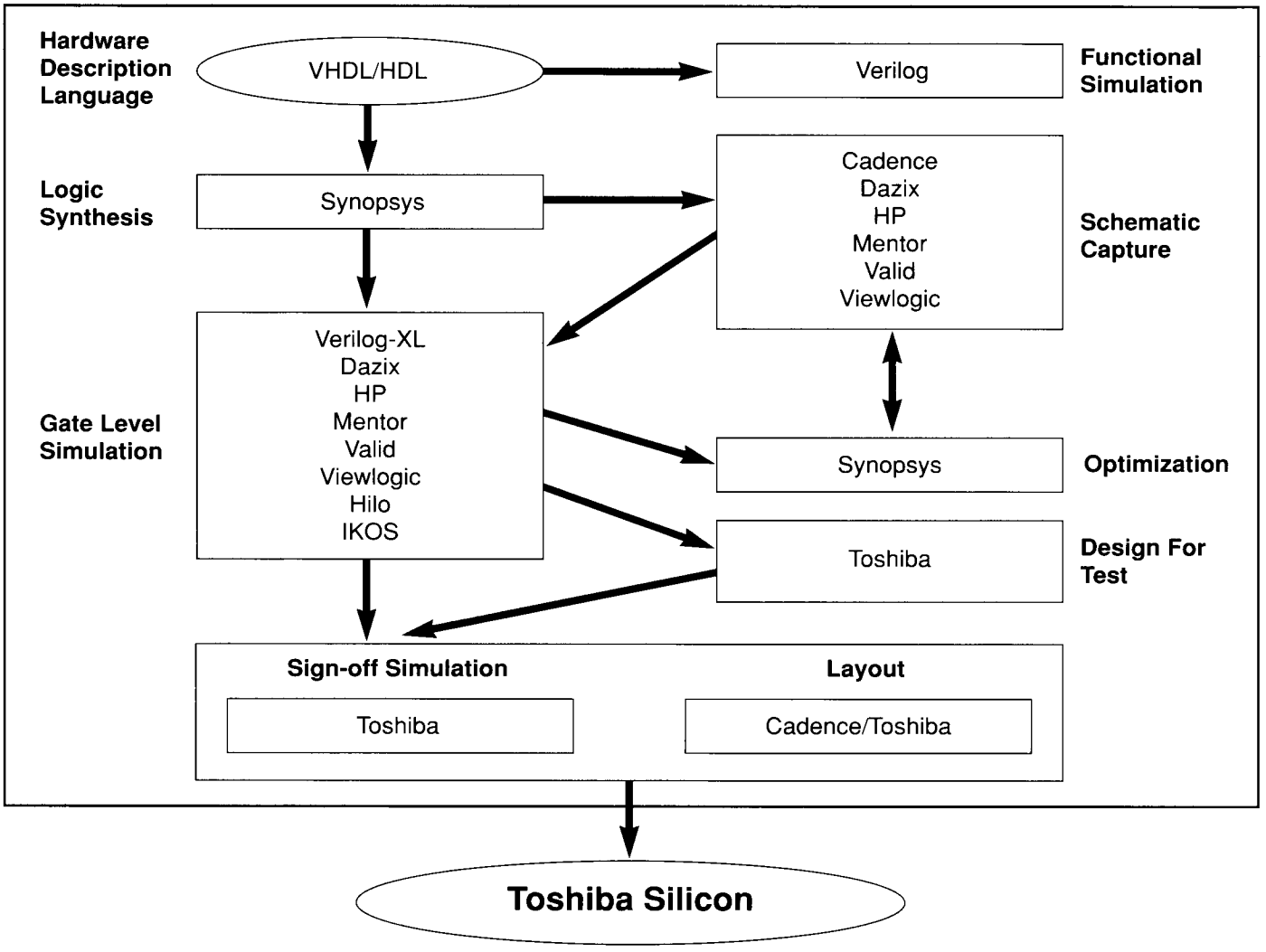
XFIxxyy
- First-in, first-out memory
- 16K gates (max.)

TC160G Package Availability (Preliminary)

Array Size			33	41	54	70	A8	D2	H6	N5	U2
Package	**Pin Count**	**Lead Pitch**	(144)	(160)	(184)	(208)	(256)	(280)	(320)	(368)	(416)
Plastic DIP	28	2.54	A*	A*							
	40	2.54	A*	A*							
	42	2.54	A*	A*							
	48	2.54	A*	A*							
	S42	1.778	A*	A*	A*						
	S64	1.778	A*								
Ceramic PGA	64	2.54	A*	A*	A*	A*	A*	A*			
	68	2.54	A*	A*	A*	A*	A*				
	84	2.54	A*	A*	A*	A*	A*				
	100	2.54	A*	A*	A*	A*	A*				
	120	2.54	A*	A*	A*	A*	A*				
	144	2.54	A*	A*	A*	A*	A*	A*			
	180	2.54			A*	A*	A*	A*			
	224	2.54					A*	A*			
	m120	2.54	A*	A*	A*	A*	A*				
	m144	2.54	A*	A*	A*	A*	A*	A*			
Ceramic cavity down PGA	95	2.54					P	P	P		
	155	2.54					A*	A*	A*	A*	A*
	223	2.54					A*	A*	A*	A*	A*
	299	2.54						A*	A*	A*	A*
PLCC	44	1.27	A*								
	68	1.27	A*	A*	A*	A*					
	84	1.27	A*	A*	A*	A*					
Plastic rectangular flat pack	64	1.0	A*	A*	A*						
	80	0.8	A*	A*	A*						
	100	0.65	A*	A*	A*						
	256	0.5							P	P	P
Plastic square flat pack	μ44	0.8	A*								
	m60	0.8	A*	A*	A*						
	m100	0.5	D	D	D						
	100	0.8	A*	A*	A*	A*	A*				
	120	0.8	A*	A*	A*	A*	A*	D	D	P	P
	144(1)	0.5	D	D	D	D	D	D	D		
	144(2)	0.65	A*	A*	A*	A*	A*	D	D	P	P
	144(3)	0.65	A*	A*	A*	A*	A*	D	D	P	P
	160	0.65		A*	A*	A*	A*	D	D	P	P
	176	0.5			A*	A*	A*	D	D		
	184	0.65			A*	A*	A*	A*	A*	P	P
	208	0.5				A*	A*	A*	A*	P	P
	232	0.65					D	D	D	P	P
	240	0.5							D	P	P
	272	0.5								P	P
	304	0.5									P
Ceramic flat pack cavity up	100	0.8		A*	A*	A*	A*				
	120	0.8			D	D	D	D	D	D	D
	144(1)	0.65				A*	A*	A*	A*	A*	A*
	144(2)	0.65				D	D	D	D	D	D
	160	0.65				D	D	D	D	D	D
	176	0.5				D	D	D			
	184	0.65					A*	A*	A*	A*	A*
	208	0.5						D	D	D	D
	232	0.65						P	D	D	D
	240	0.5							P	D	D
	272	0.5								D	D
	304	0.5									D
Rectangular	256	0.5							P	D	D
Ceramic flat pack cavity down	120	0.8			D	D	D	D	D	D	D
	144(2)	0.65				D	D	D	D	D	D
	144(3)	0.65				D	D	D	D	D	D
	160	0.65				D	D	D	D	D	D
	184	0.65					D	D	D	D	D
	208	0.5						P	D	D	D
	232	0.65							D	D	D
	240	0.5							P	D	D
	272	0.5								D	D
	304	0.5									D
Rectangular	256	0.5							P	D	D

Remarks: A*— Available, confirm with your Toshiba design center before design start
D — Under development P — Planning
(1) Body size 26mm SQ. (2) Body size 28mm SQ. (3) Body size 22mm SQ.

Toshiba Design Environment



Development Flow & Customer Interface

Available on most popular workstations.

		System & Logic Design	Schematic Entry	Verify Design	Functional & Timing Simulation	Verify Node Coverage	Auto Place & Route	Re-Simulate	PG & Mask Tooling
Interface level	Level 1	→	→	→	→	→	→	→	→
	Level 2	→	→	→	→	→	→	→	→
	Level 3	→	→	→	→	→	→	→	→
	Level 4	→	→	→	→	→	→	→	→

Level 2 design procedure is performed by the customer at a Toshiba Design Center.
Level 3 design procedure is performed at the customer site and is verified for both functionality and timing using Toshiba supplied libraries.
Level 4 design procedure—the customer takes total responsibility for the design using Toshiba supplied libraries.

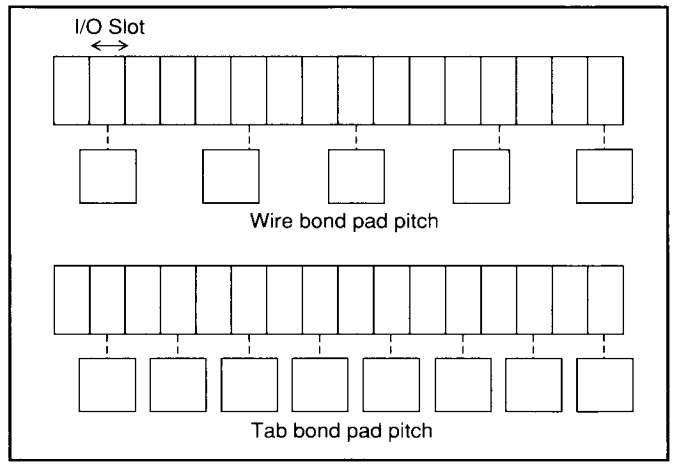
Customer → Toshiba →

More efficient I/O utilization so you can optimize the use of bonding pads

How it works. In the TC160G technology, the I/O slot pitch and pad pitch have been reduced to allow for up to seven I/O slots for every two pads. This is a change from the TC140G which has three I/O slots for every pad. This means that for wire bond pad pitch the mix of I/O drives allows for adjacent bonding pads to use certain combinations of drivers with three and four I/O slots per driver.

Even with a high current driver you only take one bonding position. With careful planning, unused I/O slots can still be "borrowed" from adjacent bonding pads. For example, an 24mA bidirectional cell which requires four I/O slots (three for output and one for the input) could be placed next to an output that requires a 16mA drive capability which uses only two of its three allotted I/O slots.

Well suited for tab. This architecture is well suited for tab technology. The bonding pads for tab can be placed with two I/O slots allocated to each pad. By doing so, drive currents are restricted to 16mA for outputs and 8mA for bidirectionals, but the number of bonding locations is increased considerably.



Pad layout of I/O cell showing I/O structure for wire bonding and tab bonding.

TOSHIBA

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

Regional Sales Offices

NORTHWEST REGION*
490-B Lakeside Drive
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TEL: (408) 737-9844
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600 S. North Lake Blvd.,
Suite 250
Altamonte Springs, FL 32701
TEL: (407) 332-0966
FAX: (407) 339-3777

*Denotes design center locations.

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