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16-Bit, Stereo A/D Converter for Digital Audio

Features

- Monolithic CMOS A/D Converter
 - Inherent Sampling Architecture
 - Stereo or Monaural Capability
 - Serial Output
- Monaural Sampling Rates up to 100 kHz
 - 50 kHz/Channel Stereo Sampling
- Signal-to-(Noise+Distortion): 92 dB
- Dynamic Range: 92 dB
 - 95 dB in 2X Oversampling Schemes
- Interchannel Isolation: 90 dB
- 2's Complement or Binary Coding
- Low Power Dissipation: 260 mW
 - Power Down Mode for Portable Applications
- Evaluation Board Available

Description

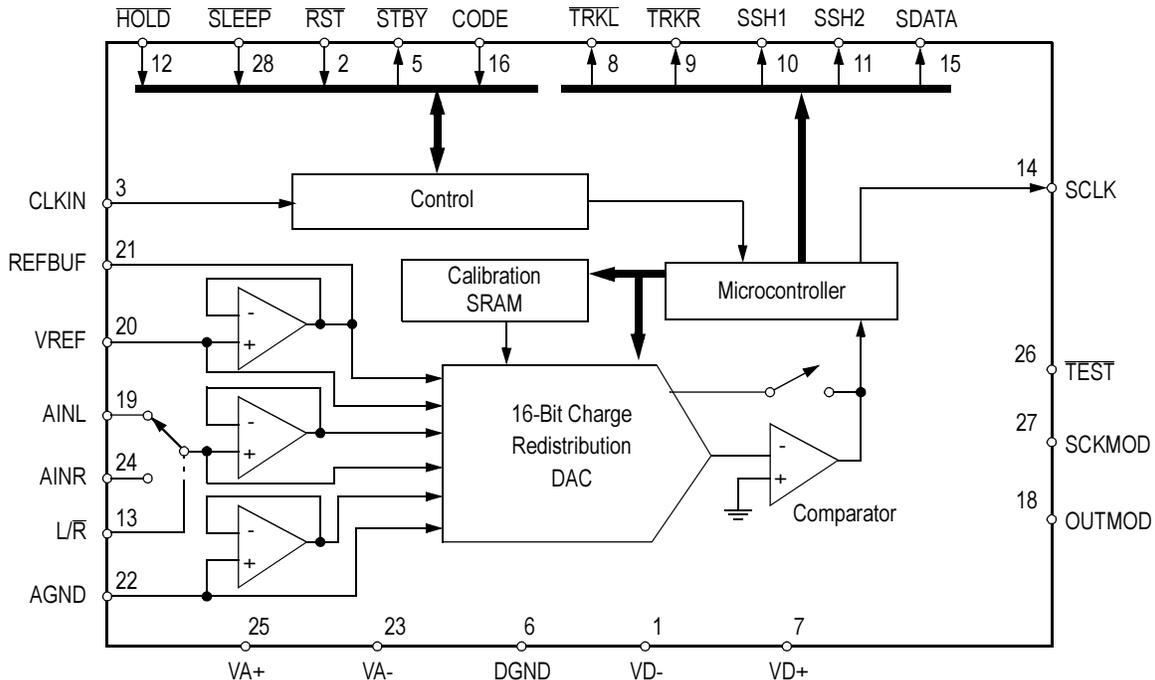
The CS5126 CMOS analog-to-digital converter is an ideal front-end for stereo or monaural digital audio systems. The CS5126 can be configured to handle two channels at up to 50 kHz sampling per channel, or it can be configured to sample one channel at rates up to 100 kHz.

The CS5126 executes a successive approximation algorithm using a charge redistribution architecture. On-chip self-calibration circuitry has 18-bit resolution thus avoiding any degradation in performance with low-level signals. The charge redistribution technique also provides an inherent sampling function which avoids the need for external sample/hold amplifiers.

Signal-to-(noise+distortion) in stereo operation is 92 dB, and is dominated by internal broadband noise (1/2 LSB rms). When the CS5126 is configured for 2X oversampling, digital post-filtering bandlimits this white noise to 20 kHz, increasing dynamic range to 95 dB.

ORDERING INFORMATION

CS5126-KP	0° to 70° C	28-pin Plastic DIP
CS5126-KL	0° to 70° C	28-pin PLCC



ANALOG CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $V_{A+}, V_{D+} = 5\text{V}$; $V_{A-}, V_{D-} = -5\text{V}$;
Full-Scale Input Sinewave, 1kHz; $f_{\text{clk}} = 24.576\text{MHz}$; $V_{\text{REF}} = 4.5\text{V}$; Analog Source Impedance = 200Ω ;
Stereo operation, L/R toggling at 48 kHz unless otherwise specified.)

Parameter*	Symbol	Min	Typ	Max	Units	
Resolution		-	-	16	Bits	
Dynamic Performance						
Signal-to-(Noise plus Distortion)	S/(N+D)					
VIN = $\pm\text{FS}$ (10 Hz to 20 kHz)		90	92	-	dB	
VIN = -20dB (f = 20 kHz)		70	72	-	dB	
Total Harmonic Distortion	THD	-	0.001	-	%	
Dynamic Range	DR	90	92	-	dB	
	Stereo Mode	-	95	-	dB	
	Monaural (20 kHz BW)					
Idle Channel Noise	$V_{n(\text{ic})}$	-	1/2	-	LSB _{rms}	
Interchannel Isolation	I_{ic}	88	90	-	dB	
	(Note 1)					
Interchannel Mismatch	M_{ic}	-	0.01	-	dB	
dc Accuracy						
Full-Scale Error	FSE	-	± 4	-	LSB	
Bipolar Offset Error	BPO	-	± 4	-	LSB	
Analog Input						
Aperture Time	t_{apt}	-	30	-	ns	
Aperture Jitter	t_{ajt}	-	100	-	ps	
Input Capacitance	C_{in}	-	200	-	pF	
	(Note 2)					
Power Supplies						
Power Supply Current	Positive Analog (Note 3)	I_{A+}	-	18	23	mA
	Negative Analog	I_{A-}	-	-18	-23	mA
	Positive Digital	I_{D+}	-	8	12	mA
	Negative Digital	I_{D-}	-	-8	-12	mA
Power Dissipation	(SLEEP High) (Notes 3, 4)	P_{do}	-	260	350	mW
	(SLEEP Low)	P_{ds}	-	1	-	mW
Power Supply Rejection	Positive Supplies (Note 5)	PSR	-	84	-	dB
	Negative Supplies		-	84	-	dB

- Notes: 1. One input grounded; dc to 20kHz, Full Scale input on the other channel. Guaranteed by characterization.
2. Applies only in the track mode. When converting or calibrating, input capacitance will typically be 10 pF.
3. All outputs unloaded. All inputs CMOS levels.
4. Power dissipation in sleep mode applies with no master clock applied (CLKIN high or low).
5. With 300mV p-p, 1kHz ripple applied to each supply separately. A plot of typical power supply rejection appears in the *Analog Circuit Connections* section.

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX} ; $V_{A+}, V_{D+} = 5V \pm 10\%$; $V_{A-}, V_{D-} = -5V \pm 10\%$)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 6)	V_{OH}	$(V_{D+})-1.0V$	-	-	V
Low-Level Output Voltage $I_{out} = 1.6$ mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	μA

Notes: 6. $I_{OUT} = -100 \mu A$. This specification guarantees that each digital output will drive one TTL load ($V_{OH} = 2.4V$ @ $I_{OUT} = -40 \mu A$).

RECOMMENDED OPERATING CONDITIONS ($AGND, DGND = 0V$, see note 7.)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Positive Digital	V_{D+}	4.5	5.0	V_{A+}	V
Negative Digital	V_{D-}	-4.5	-5.0	-5.5	V
Positive Analog	V_{A+}	4.5	5.0	5.5	V
Negative Analog	V_{A-}	-4.5	-5.0	-5.5	V
Analog Reference Voltage	V_{REF}	2.5	4.5	$(V_{A+})-0.5$	V
Analog Input Voltage (Note 8)	V_{AIN}	$-V_{REF}$	-	V_{REF}	V

Notes: 7. All voltages with respect to ground.

8. The CS5126 can accept input voltages up to the analog supplies (V_{A+}, V_{A-}). It will produce an output of all 1's for inputs above V_{REF} and all 0's for inputs below $-V_{REF}$.

ABSOLUTE MAXIMUM RATINGS ($AGND, DGND = 0V$, all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supplies:				
Positive Digital	V_{D+}	-0.3	$(V_{A+})+0.3$	V
Negative Digital	V_{D-}	0.3	-6.0	V
Positive Analog	V_{A+}	-0.3	6.0	V
Negative Analog	V_{A-}	0.3	-6.0	V
Input Current, Any Pin Except Supplies (Note 9)	I_{in}	-	± 10	mA
Analog Input Voltage (AIN and VREF pins)	V_{INA}	$(V_{A-})-0.3$	$(V_{A+})+0.3$	V
Digital Input Voltage	V_{IND}	-0.3	$(V_{D+})+0.3$	V
Ambient Temperature (power applied)	T_A	-55	125	$^{\circ}C$
Storage Temperature	T_{stg}	-65	150	$^{\circ}C$

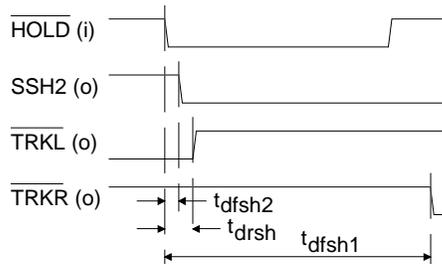
Notes: 9. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

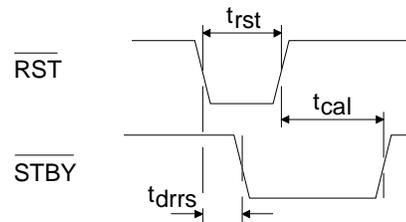
SWITCHING CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$; $V_{A+}, V_{D+} = 5V \pm 10\%$; $V_{A-}, V_{D-} = -5V \pm 10\%$; Inputs: Logic 0 = 0V, Logic 1 = V_{D+} ; $C_L = 50\text{ pF}$)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Period	t_{clk}	40	-	-	ns
HOLD to SSH2 Falling (Note 10)	t_{dfsh2}	-	80	-	ns
HOLD to TRKL, TRKR SSH1 Falling	t_{dfsh1}	$198t_{clk}$	-	$214t_{clk}+50$	ns
HOLD to TRKL, TRKR SSH1, SSH2 Rising	t_{drsh}	-	80	-	ns
RST Pulse Width	t_{rst}	150	-	-	ns
RST to STBY Falling	t_{drrs}	-	100	-	ns
RST Rising to STBY Rising	t_{cal}	-	34,584,480	-	t_{clk}
HOLD Pulse Width	t_{hold}	$2t_{clk}+50$	-	$192t_{clk}$	ns
HOLD to L/R Edge (Note 10)	t_{dhlri}	-30	-	$192t_{clk}$	ns
SCLK period	t_{sclk}	200	-	-	ns
SCLK Pulse Width Low	t_{sckl}	50	-	-	ns
SCLK Pulse Width High	t_{sckh}	50	-	-	ns
SCLK Falling to SDATA Valid	t_{dss}	-	100	140	ns
HOLD Falling to SDATA Valid	t_{dhs}	-	140	200	ns

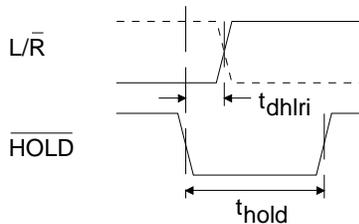
Notes: 10. SSH2 only works correctly if $\overline{\text{HOLD}}$ falling edge is within $\pm 30\text{ns}$ of L/R edge OR if $\overline{\text{HOLD}}$ falling edge occurs between 30ns before $\overline{\text{HOLD}}$ rises to $192 t_{clk}$ after $\overline{\text{HOLD}}$ falls.



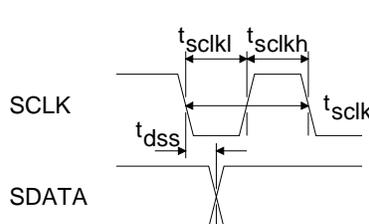
Control Output Timing



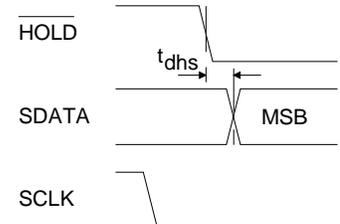
Reset and Calibration Timing



Channel Selection Timing



Serial Data Timing



Data Transmit Start Timing

GENERAL DESCRIPTION

The CS5126 is a 2-channel, 100kHz A/D converter designed specifically for stereo digital audio. The device includes an inherent sample/hold and an on-chip analog switch for stereo operation. Both left and right channels can thus be sampled and converted at rates up to 50kHz per channel. Alternatively, the CS5126 can be implemented in 2X oversampling schemes for improved dynamic range and distortion.

Output data is available in serial form with either binary or 2's complement coding. Control outputs are also supplied for use with an external sample/hold amplifier to implement simultaneous sampling.

THEORY OF OPERATION

The CS5126 implements a standard successive approximation algorithm using a charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. When not converting, the CS5126 tracks the analog input signal. The input voltage is applied across each leg of the DAC capacitor array, thus performing a voltage-to-charge conversion.

When the conversion command is issued, the charge is trapped on the capacitor array and the analog input is thereafter ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the binary-weighted legs of the capacitor array to the voltage reference and analog ground. All legs share one common node at the input to the converter's comparator. This forms a binary-weighted capacitive divider. Since the charge at the comparator's input remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The suc-

cessive-approximation algorithm is used to find the proportion of capacitance which will drive the voltage to the comparator's trip point. That binary fraction of capacitance represents the converter's digital output.

Calibration

The ability of the CS5126 to convert accurately clearly depends on the accuracy of its DAC. The CS5126 uses an on-chip self-calibration scheme to insure low distortion and excellent dynamic range *independent of input signal conditions*.

Each binary-weighted bit capacitor actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller manipulates the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, $16C = 8C + 4C + 2C + C + C$). The result is typical differential nonlinearity of $\pm 1/4$ LSB. That is, codes typically range from $3/4$ to $5/4$ LSB's wide.

The CS5126 should be reset upon power-up, thus initiating a calibration cycle which takes 1.4 seconds to complete. The CS5126 then stores its calibration coefficients in on-chip SRAM, and can be recalibrated at any later time.

SYSTEM DESIGN WITH THE CS5126

All timing and control inputs to the CS5126 can be easily generated from a master system clock. The CS5126 outputs serial data and a variety of digital outputs which can be used to control an external sample/hold amplifier for simultaneous sampling. The actual circuit connections depend on the system architecture (stereo or monaural 2X oversampling), and on the sampling characteristics (simultaneous or sequential sampling between channels).

System Initialization

Upon power up, the CS5126 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5126's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before $\overline{\text{RST}}$ rises to guarantee an accurate calibration. Later, the CS5126 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5126 will clear and initiate a new calibration cycle mid-conversion or midcalibration.

When $\overline{\text{RST}}$ is brought low all internal logic clears. When it returns high a calibration cycle begins which takes 34,584,480 master clock cycles to complete (approximately 1.4 seconds with a standard 24MHz master clock). The CS5126's $\overline{\text{STBY}}$ output remains low throughout the calibration sequence, and a rising transition indicates the device is ready for normal operation.

A simple power-on reset circuit can be built using a resistor and capacitor as shown in Figure 1. The RC time constant must be long enough to guarantee the rest of the system is fully powered up and stable by the end of reset.

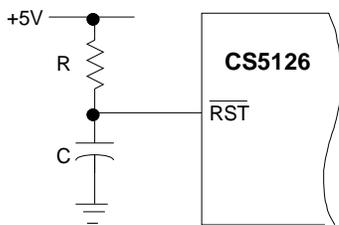


Figure 1. Power-On Reset Circuit

Master Clock

The CS5126 operates from an externally-supplied master clock. In stereo operation, the master clock frequency is set at 512 times the per-channel sampling rate (256 in 2X oversampling schemes). The CS5126 can accept master clocks up to 24.576 MHz for 48kHz stereo sampling or 96kHz monaural oversampling.

All timing and control inputs for channel selection, sampling, and serial data transmission may be divided down from the master clock. This yields a completely synchronous system, avoiding sampling and conversion errors due to asynchronous digital noise.

CIRCUIT CONNECTIONS

Stereo Operation

Figure 2 shows the standard circuit connections for operating the CS5126 in its stereo mode. The $\overline{\text{HOLD}}$, $\text{L}/\overline{\text{R}}$, and SCLK inputs are derived from the master clock using a binary divider string. A 24.576 MHz master clock is required for a sampling rate of 48kHz per channel.

For 48kHz stereo sampling, the CS5126 must sample and convert at a 96kHz rate to handle both channels. The master clock is divided by 256 and applied to the $\overline{\text{HOLD}}$ input. A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{\text{HOLD}}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns.

In stereo operation the CS5126 alternately samples and converts the left and right input channels. This alternating channel selection is achieved by dividing the $\overline{\text{HOLD}}$ input by two (that is, dividing the master clock by 512) and applying it to the $\text{L}/\overline{\text{R}}$ input. Upon completion of each conversion cycle, the CS5126 automatically returns to the track mode. The status of $\text{L}/\overline{\text{R}}$ as

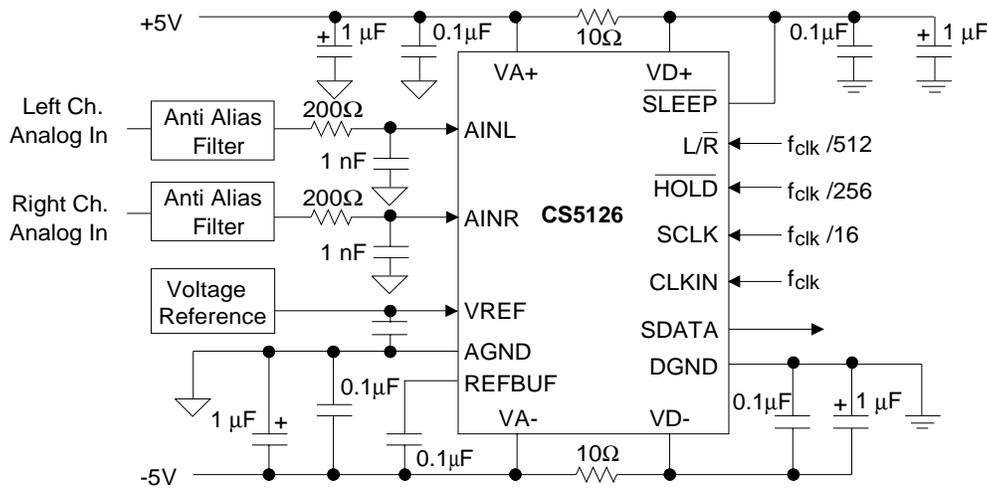


Figure 2. Stereo Mode Connection Diagram

each conversion finishes determines which channel is acquired and tracked. The L/\bar{R} input must remain valid at least until 30ns before the next falling transition on \overline{HOLD} .

As shown in the timing diagram in Figure 3, the CS5126 uses pipelined data transmission. That is, data from a particular conversion transmits during the *next* conversion cycle. The serial clock input, SCLK, is derived by dividing the master clock by 16. The MSB (most-significant-bit) will be stable on the first rising edge of SCLK after a falling transition on \overline{HOLD} . With a serial clock of $f_{CLK}/16$, transmission of all 16 output bits will span an entire conversion and acquisition cycle.

STEREO MODE PERFORMANCE

As illustrated in Figure 4, the CS5126 typically provides 92dB S/(N+D) and 0.001% THD. Unlike conventional successive-approximation ADC's, the CS5126's signal-to-noise and dynamic range are not limited by differential non-linearities (DNL) caused by calibration errors. Rather, the dominant noise source is broadband thermal noise which aliases into the baseband. This *white* broadband noise also appears as an idle channel noise of 1/2 LSB (rms).

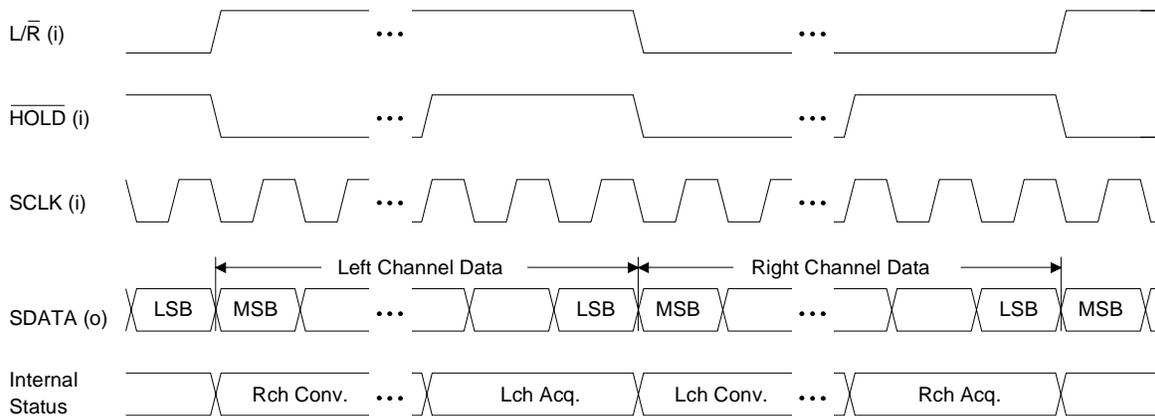


Figure 3. Stereo Mode Timing

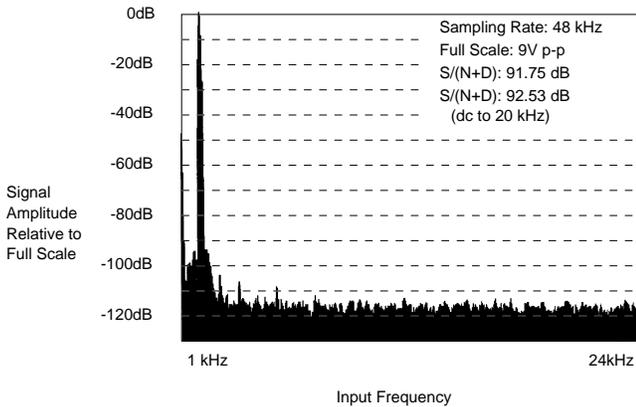


Figure 4. FFT Plot of CS5126 in Stereo Mode (Left Channel with 1 kHz, Full-Scale Input)

Differential Nonlinearity

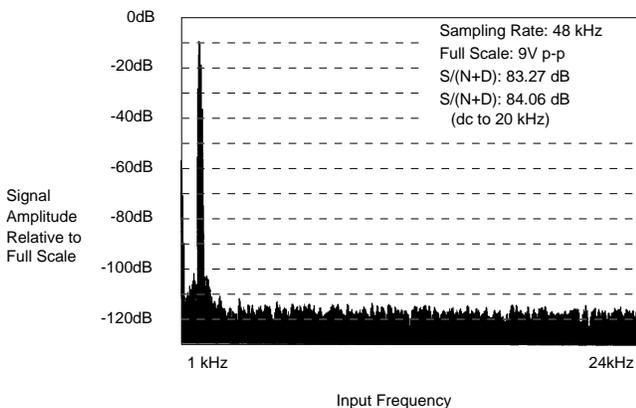
The self-calibration scheme utilized in the CS5126 features a calibration resolution of 1/4 LSB, or 18-bits. This ideally yields DNL of $\pm 1/4$ LSB, with code widths ranging from 3/4 to 5/4 LSB's. This insures consistent sound quality independent of signal level.

Traditional laser trimmed ADC's have significant differential nonlinearities which are disastrous to sound quality with low-level signals. Appearing as wide and narrow codes, DNL often causes entire sections of the transfer func-

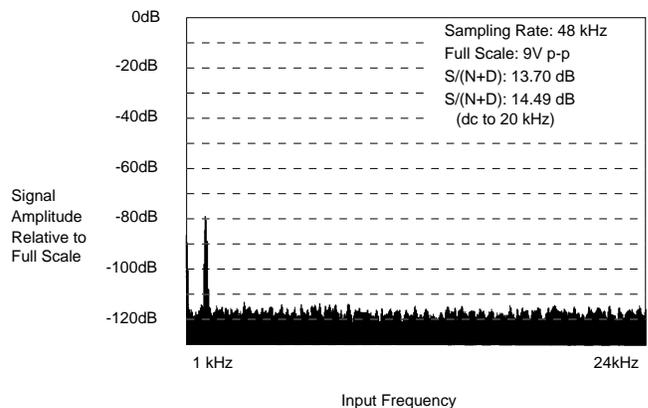
tion to be missing. Although their affect is minor on S/(N+D) with high amplitude signals, DNL errors dominate performance with low-level signals. For instance, a signal 80dB below full-scale will slew past only 6 or 7 codes. Half of those codes could be missing with a conventional hybrid ADC capable of only 14-bit DNL.

The most common source of DNL errors in conventional ADC's is bit weight errors. These can arise due to accuracy limitations in factory trim stations, thermal or physical stresses after calibration, and/or drifts due to aging or temperature variations in the field. Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions.

Differential nonlinearities in successive-approximation ADC's also arise due to dynamic errors in the comparator. Such errors can dominate if the converter's throughput/sampling rate is driven too high. The comparator will not be allowed sufficient time to settle during each bit decision in the successive-approximation algo-



a. Left Channel with 1 kHz, -10 dB Input



b. Left Channel with 1 kHz, -80 dB Input

Figure 5. FFT Plots of CS5126 in Stereo Mode

rithm. The worst-case codes for dynamic errors are the major transitions (1/2 FS; 1/4, 3/4 FS; etc.). Since DNL effects are most critical with low-level signals, the codes around in mid-scale, (that is, 1/2 FS), are most important. Yet those codes are worst-case for dynamic DNL errors!

With all linearity calibration performed on-chip to 18-bits, the CS5126 maintains accurate bit weights. DNL errors are dominated by residual calibration errors of $\pm 1/4$ LSB rather than dynamic errors in the comparator. Furthermore, *all* DNL effects on $S/(N+D)$ are buried by white broadband noise. This yields excellent sound quality *independent of signal level*. (See Figure 5)

Sampling Distortion

Like most discrete sample/hold amplifier designs, the CS5126’s inherent sample/hold exhibits a frequency-dependent distortion due to nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is given. The charge on the array ideally assumes a linear relationship to the analog input voltage. Any deviation from this linear relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array’s voltage coefficient dictates the converter’s linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between the charge on the array and the analog input voltage and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 4).

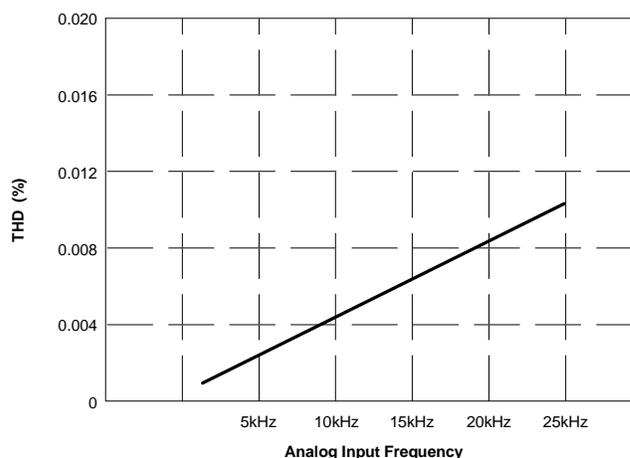


Figure 6. THD vs Input Frequency (9V p-p Full-Scale Input)

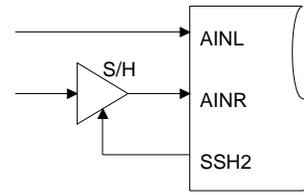
The ideal relationship between the charge on the array and the input voltage can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency and slew rate as shown in Figure 6 since the magnitude of the steady state current increases. First noticeable at 1kHz, this distortion assumes a linear relationship with input frequency. *With signals 20dB or more below full-scale, it no longer dominates the converter’s overall $S/(N+D)$ performance.*

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array’s charge current to decay, thereby eliminating any voltage drop across the switches. Since the CS5126 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter’s $\overline{\text{HOLD}}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

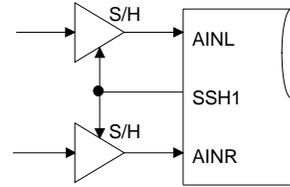
Simultaneous Sampling

The CS5126 offers four digital output signals, SSH1, SSH2, $\overline{\text{TRKL}}$, and $\overline{\text{TRKR}}$ which can be used to control external sample/hold amplifiers to achieve simultaneous sampling and/or reduce sampling distortion.

Figure 7 shows the timing relationships for SSH1, SSH2, $\overline{\text{TRKL}}$, and $\overline{\text{TRKR}}$. In the stereo configuration shown in Figure 1 the CS5126 samples the left and right channels 180° out of phase. Simultaneous sampling between the left and right channels can be achieved as shown in Figure 8a using the CS5126's SSH2 output. The external sample/hold will freeze the right channel analog signal as the CS5126 freezes the left channel input at AINL. It will hold that signal valid at AINR until the CS5126 begins a right channel conversion. Once that conversion begins, the sample/hold returns to the sample mode. The acquisition time for the external sample/hold amplifier must not exceed the CS5126's minimum conversion time of 192 master clock cycles (7.8µs for 48kHz stereo sampling).



a. Standard Connections



b. High-Slew Conditions

Figure 8. Simultaneous Sampling Connections

The CS5126's sampling distortion with high-frequency, high-amplitude input signals may be improved if a low distortion sample/hold amplifier is used as shown in Figure 8a. The right channel input at AINR will appear as dc to the CS5126 resulting in *no ac current* flowing through the internal MOS switches. Sampling distortion can likewise be improved for *both channels* using the SSH1 output as shown in Figure 8b. Simi-

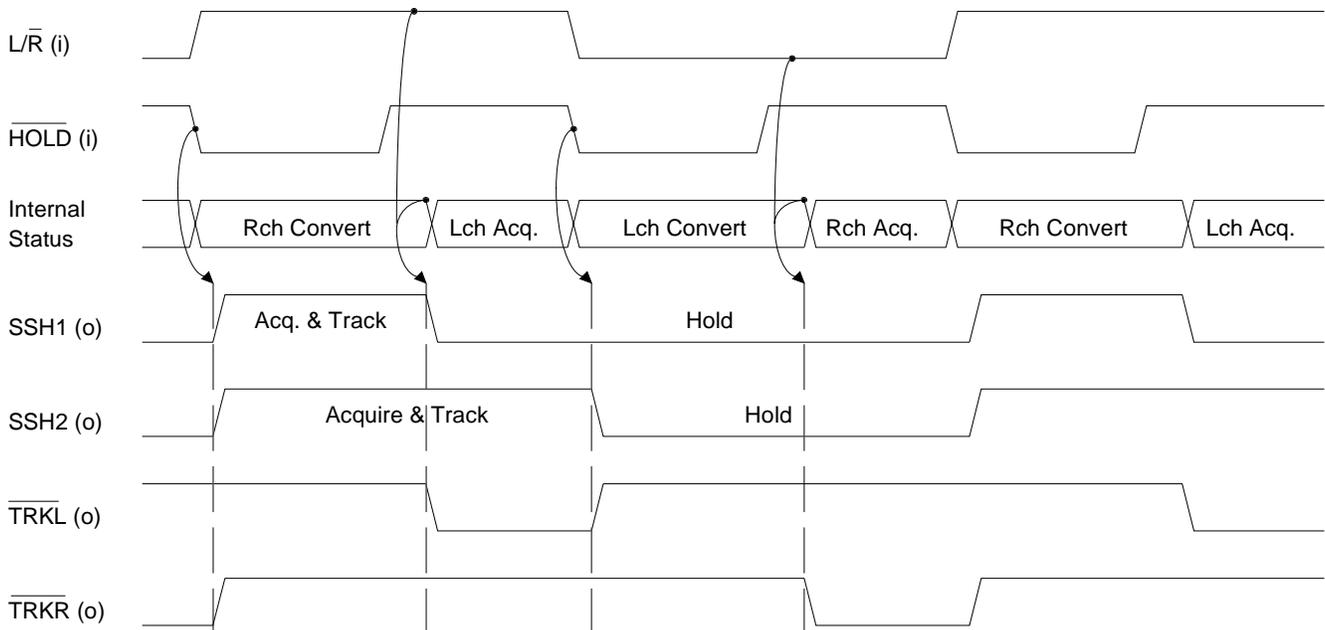


Figure 7. External Sampling Control Output Timing

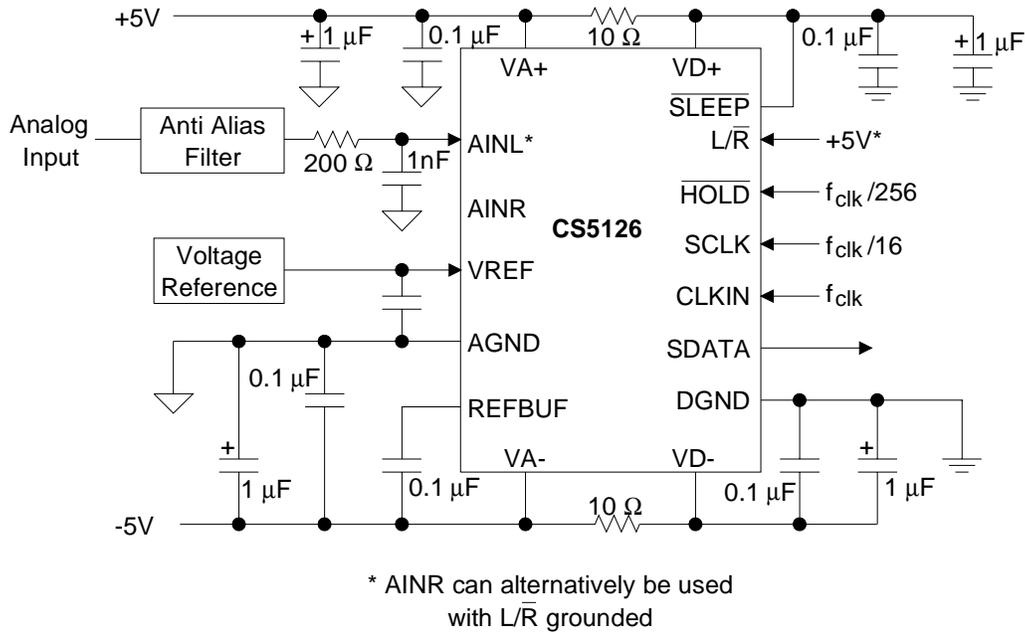


Figure 9. Monaural 2X Oversampling Connections

larly, the acquisition time for the external sample/hold amplifiers must not exceed the minimum conversion time of 192 master clock cycles (7.8μs for 48kHz stereo sampling).

Oversampling

The CS5126 can alternatively be used to oversample *one channel* (monaural) by 2X simply by tying the L/R input high or low. This moves much of the anti-alias burden from analog filters to digital post-filtering. The analog filters’ corner can be pushed out in frequency with lower roll-off, allowing lower passband ripple and more linear phase in the audioband. Digital FIR filtering, meanwhile, can be used to implement high roll-off filters with ultra-low passband ripple and perfectly linear phase.

Oversampling not only improves system-level filtering performance, but it also enhances the ADC’s dynamic range and distortion characteristics. All noise energy in a sampled, digital signal aliases into the baseband between dc and one-half the sampling rate. For an *ideal* succes-

sive-approximation ADC the noise spectral content is white. Therefore, in a 2X oversampling scheme such as 96kHz sampling the ADC’s noise will be spread *uniformly* from dc to 48kHz. Digital post-filtering then rejects noise outside of the 20kHz or 22kHz bandwidth, resulting in improved signal-to-noise and dynamic range. For a white noise spectrum, a 2X reduction in bandwidth yields a 3dB improvement in dynamic range.

Due to its on-chip self-calibration scheme, the CS5126’s dynamic range is limited only by *white* broadband noise rather than signal-dependent DNL errors. Therefore, the CS5126 picks up a full 3dB improvement in dynamic range to 95dB when implemented in 2X oversampling schemes.

Oversampling and digital filtering also enhance the ADC’s distortion performance. Consider for example a full-scale 15kHz input signal to the CS5126 sampling at 96kHz. Sampling distortion produces THD of approximately 0.005% (86dB) at the converter’s output. Most of the distortion energy resides in the second and third harmonics

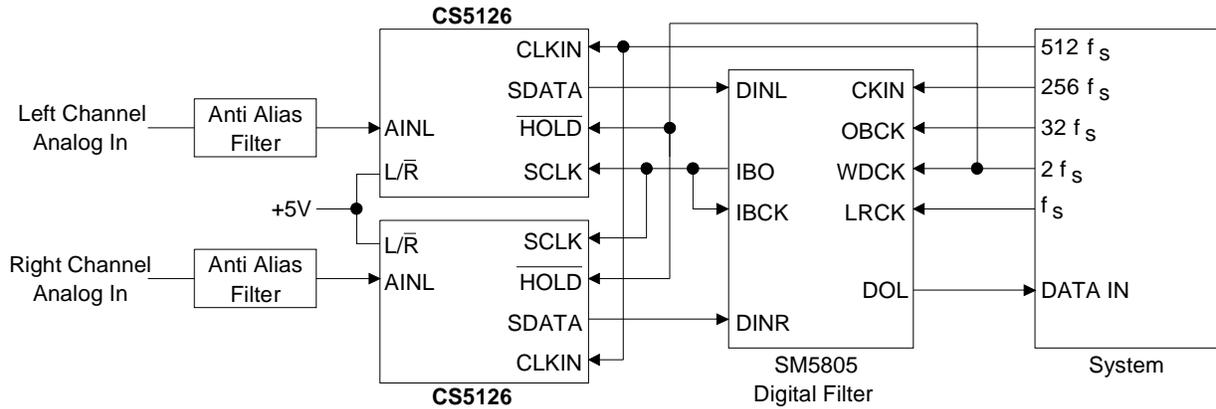


Figure 10. Example Oversampling System Diagram

at 30kHz and 45kHz. Meanwhile, digital filters such as the SM5805 shown in Figure 10 will roll-off rapidly from 22kHz to 28kHz and reject distortion energy in the second, third, and fourth harmonics. Clearly, oversampling results in superior system-level distortion.

Still, if the CS5126’s distortion performance with high-frequency, high-amplitude signals must be enhanced in 2X oversampling schemes, the $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ outputs can be used. Either $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ will fall at the end of each conversion cycle depending on which channel is being acquired. The AINL and $\overline{\text{TRKL}}$ connections (or AINR and $\overline{\text{TRKR}}$) can be used as shown in Figure 11 to control an external low-distortion sample/hold to create an effective dc input for the CS5126 and remove sampling distortion.

Digital Circuit Connections

When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The CS5126 has a power down mode, initiated by bringing $\overline{\text{SLEEP}}$ low. During power down, the A/D Converter’s calibration information is retained. The CS5126 may be used for conversion immediately after $\overline{\text{SLEEP}}$ is brought high.

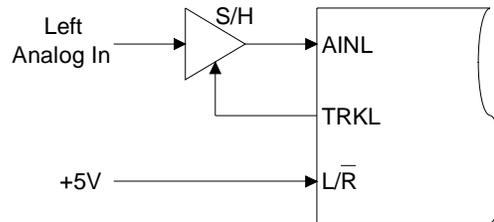


Figure 11. High-Slew Monaural Connections

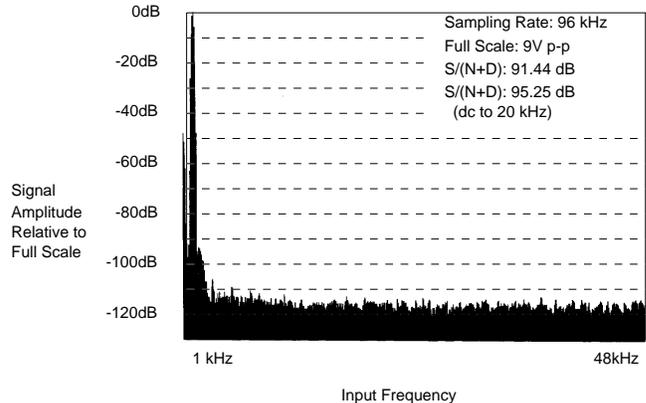


Figure 12. FFT Plot of CS5126 in Monaural 2X Oversampling Mode

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5126 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

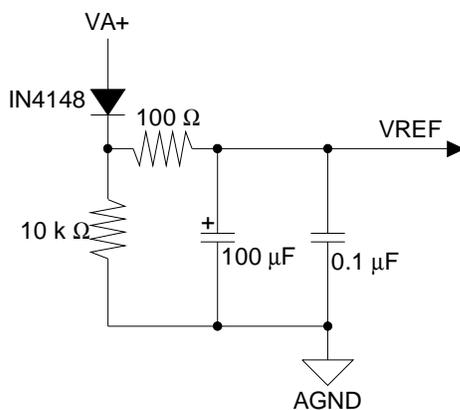
Reference Considerations

An application note titled "Voltage references for the CS501X/CSZ511X Series of A/D Converters" is available which describes the dynamic load conditions presented by the VREF input on Crystal's self-calibrating SAR A/D converters (including the CS5126). As the CS5126 sequences through bit decisions it switches portions of the capacitor array to the VREF pin in accordance with the successive-approximation algorithm. For proper operation, the source impedance at the VREF pin must remain low at frequencies up to 1MHz.

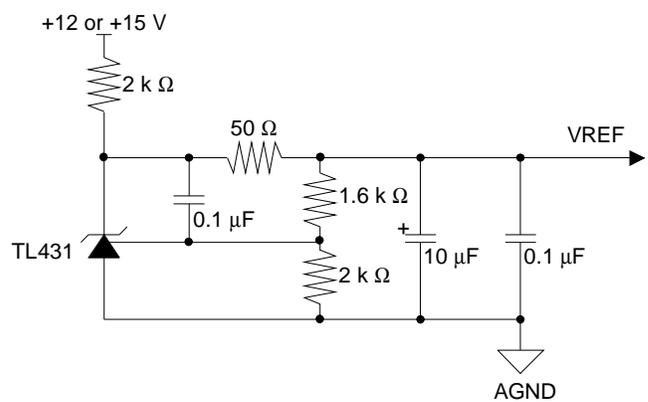
A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the frequencies of interest, so the reference voltage can simply be derived as shown in Figure 13a. Although very low cost, this reference has almost no power supply rejection from the VA+ line.

Alternatively, a more stable and precise reference can be generated using a TL431 shunt reference from T.I. or Motorola, as shown in Figure 13b.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At the full-rated 24 MHz clock the reference must supply a maximum load current of 20µA peak-to-peak (2µA typical). An output impedance of 2Ω will therefore yield a maximum error of 40mV. With a 4.5V reference and LSB size of 138mV this would insure approximately 1/4 LSB accuracy. A 10µF capacitor exhibits an impedance of less than 2Ω at frequencies greater than 16kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.



a. Simple Reference



b. Low-cost Shunt Reference

Figure 13. Suggested Voltage Reference Circuits

The CS5126 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5126 can actually accept reference voltages up to the positive analog supply. However, as the reference voltage approaches V_{A+} the external drive requirements may increase at V_{REF} .

An internal reference buffer is used to protect the external reference from current transients during conversion. This internal buffer enlists the aid of an external 0.1 μ F ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, V_{A-} .

Analog Input Connection

Each time the CS5126 finishes a conversion cycle it switches the internal capacitor array to the appropriate analog input pin, AINL or AINR. This creates a minor dynamic load at the sampling frequency. All throughput specifications apply for maximum analog source impedances of 200 Ω at AINL and AINR. In addition, the comparator requires source impedances of less than 400 Ω around 2MHz for stability, which is met by practically all bipolar op amps. For more information, see our Application Note: "Input Buffers for the CS501X/CSZ511X Series of A/D Converters"

Analog Input Range/Coding Format

The CS5126 features a bipolar input range with the reference voltage applied to V_{REF} defining both positive and negative full-scale. The coding format is set by the state of the CODE input. If high, coding is 2's complement; if low, the CS5126's output is in offset-binary format.

Grounding and Power Supply Decoupling

The CS5126 uses the analog ground connection, AGND, only as a reference voltage. *No dc power or signal currents flow through the AGND connection*, thus minimizing the potential for interchannel crosstalk. Also, AGND is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both analog inputs and the reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground. The digital and analog supplies are isolated within the CS5126 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 μ F ceramic capacitors. If significant low frequency noise is present on the supplies, 1 μ F tantalum capacitors are recommended in parallel with the 0.1 μ F capacitors.

The positive digital power supply of the CS5126 must never exceed the positive analog supply by more than a diode drop or the CS5126 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagrams in figures 2 and 9 show a decoupling scheme which allows the CS5126 to be powered from a single set of $\pm 5V$ rails. The positive digital supply is derived from the analog supply through a 10 Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10 Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital

supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5126 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5126. The CDB5126 evaluation board is available for the CS5126, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5126, and

can be quickly reconfigured to simulate any combination of sampling and master clock conditions.

Power Supply Rejection

The CS5126 features a fully differential comparator design, resulting in superior power supply rejection. Rejection is further enhanced by the on-chip self-calibration and "auto-zero" process. Figure 14 shows worst-case rejection for all combinations of conversion rates and input con-

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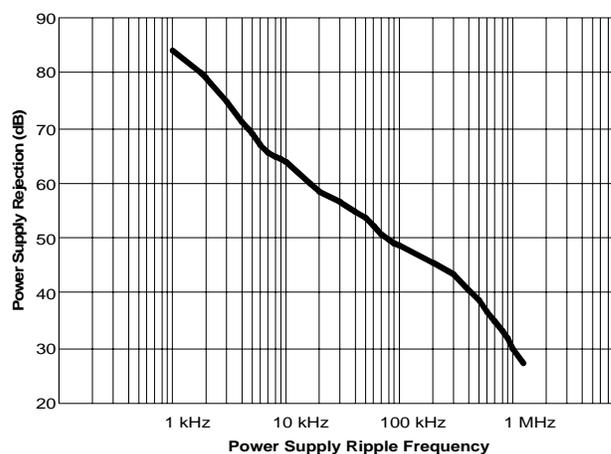
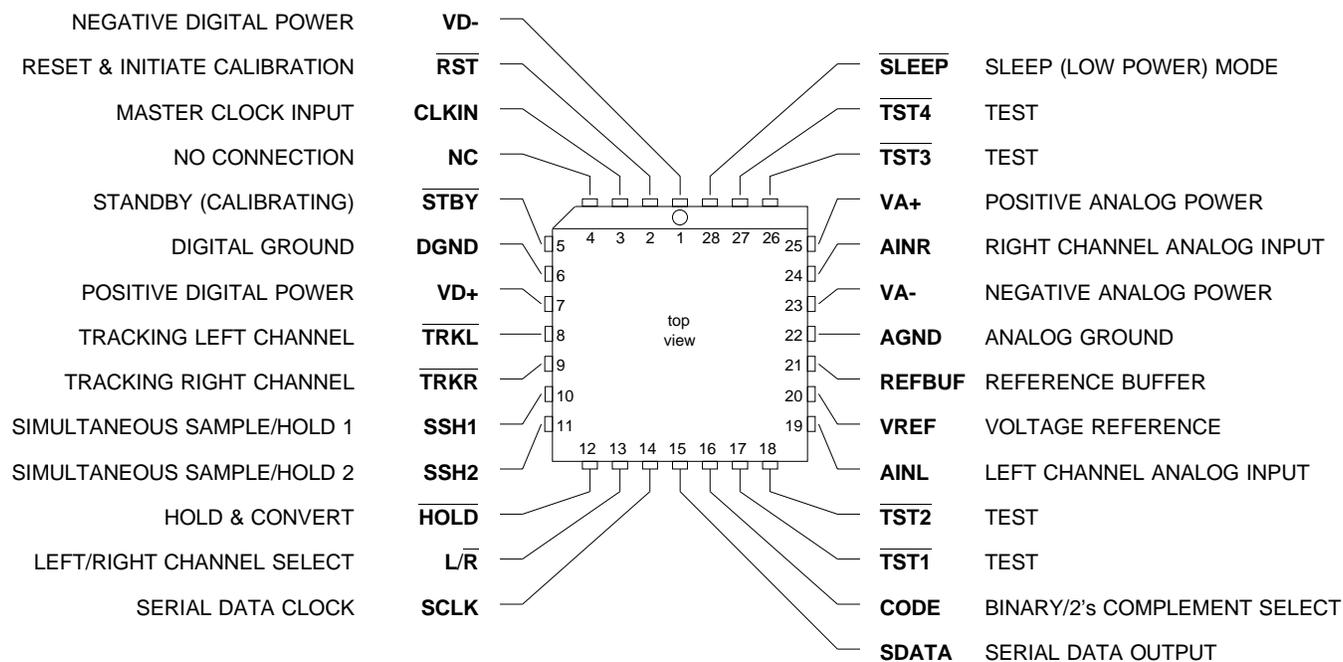


Figure 14. Power Supply Rejection

ditions.

PIN DESCRIPTIONS

NEGATIVE DIGITAL POWER	VD-	1	28	SLEEP	SLEEP (LOW POWER) MODE
RESET & INITIATE CALIBRATION	RST	2	27	TST4	TEST
MASTER CLOCK INPUT	CLKIN	3	26	TST3	TEST
NO CONNECTION	NC	4	25	VA+	POSITIVE ANALOG POWER
STANDBY (CALIBRATING)	STBY	5	24	AINR	RIGHT CHANNEL ANALOG INPUT
DIGITAL GROUND	DGND	6	23	VA-	NEGATIVE ANALOG POWER
POSITIVE DIGITAL POWER	VD+	7	22	AGND	ANALOG GROUND
TRACKING LEFT CHANNEL	TRKL	8	21	REFBUF	REFERENCE BUFFER
TRACKING RIGHT CHANNEL	TRKR	9	20	VREF	VOLTAGE REFERENCE
SIMULTANEOUS SAMPLE/HOLD 1	SSH1	10	19	AINL	LEFT CHANNEL ANALOG INPUT
SIMULTANEOUS SAMPLE/HOLD 2	SSH2	11	18	TST2	TEST
HOLD & CONVERT	HOLD	12	17	TST1	TEST
LEFT/RIGHT CHANNEL SELECT	L/R	13	16	CODE	BINARY/2's COMPLEMENT SELECT
SERIAL DATA CLOCK	SCLK	14	15	SDATA	SERIAL DATA OUTPUT



Power Supply Connections**VD+ - Positive Digital Power, PIN 7.**

Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 1.

Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 6.

Digital ground reference.

VA+ - Positive Analog Power, PIN 25.

Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 23.

Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 22.

Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 3.

All conversions and calibrations are timed from a master clock which must be externally supplied.

Digital Inputs **$\overline{\text{HOLD}}$ - Hold, PIN 12.**

A falling transition on this pin sets the CS5126 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

 $\overline{\text{L/R}}$ - Left/Right Input Channel Select, PIN 13.

Status at the end of a conversion cycle determines which analog input channel will be acquired for the next conversion cycle.

 $\overline{\text{SLEEP}}$ - Sleep, PIN 28.

When brought low causes the CS5126 to enter a low-power quiescent state. All calibration coefficients are retained in memory, so no recalibration is needed after returning to the normal operating mode.

CODE - 2's Complement/Binary Coding Select, PIN 16.

Determines whether data appears in 2's complement or offset-binary format. If high, 2's complement; if low, offset-binary.

SCLK - Serial Clock, PIN 14.

Serial data changes status on a falling edge of this input, and is valid on a rising edge.

$\overline{\text{RST}}$ - Reset, PIN 32.

When taken low, all internal digital logic is reset. Upon returning high, a full calibration sequence is initiated which takes 34,584,480 master clock cycles to complete.

Analog Inputs**AINL, AINR - Left and Right Channel Analog Inputs, PINS 19 and 24.**

Analog input connections for the left and right input channels.

VREF - Voltage Reference, PIN 20.

The analog reference voltage which sets the analog input range. Its magnitude sets both positive and negative full-scale.

Digital Outputs **$\overline{\text{STBY}}$ - Standby (Calibrating), PIN 5.**

Indicates calibration status after reset. Remains low throughout the calibration sequence and returns high upon completion.

SDATA - Serial Output, PIN 15.

Presents each output data bit on a falling edge of the SCLK input. Data is valid to be latched on the rising edge of SCLK.

SSH1, SSH2 - Simultaneous Sample/Hold 1 and 2, PINS 10 and 11.

Used to control external sample/hold amplifier(s) to achieve simultaneous stereo sampling.

 $\overline{\text{TRKL}}$, $\overline{\text{TRKR}}$ - Tracking Left, Tracking Right, PINS 8 and 9.

Indicate the end of a conversion cycle. Either $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ falls at the end of a conversion cycle depending on the status of L/R and which channel is to be tracked.

Analog Outputs**REFBUF - Reference Buffer Output, PIN 21.**

Reference buffer output. A 0.1 μ F ceramic capacitor must be tied between this pin and VA-.

Miscellaneous**NC - No Connection, PIN 4.**

Must be left floating for proper operation.

 $\overline{\text{TST1}}$, $\overline{\text{TST2}}$, $\overline{\text{TST3}}$, $\overline{\text{TST4}}$ - Test, PINS 17, 18, 26, 27.

Allow access to the CS5126's test functions which are reserved for factory use. Must be tied to VD+.

PARAMETER DEFINITIONS

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Signal-to-Noise plus Distortion Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Dynamic Range - Full-scale Signal-to-Noise plus Distortion with the input signal 60dB below full-scale. Units in decibels.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Full Scale Error - The deviation of the last code transition from the ideal ($V_{REF} - 3/2$ LSB's) after all offsets have been externally compensated. Units in decibels relative to full scale.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal ($1/2$ LSB below AGND). Units in microvolts.

Interchannel Mismatch - The difference in output codes between the left and right channels with the same analog input applied. Units expressed in decibels relative to full scale. Tested at full scale input.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

• **Notes** •

Evaluation Board for CS5126

Features

- Serial to Parallel Conversion
- All Timing Signals Provided
- Adjustable Voltage Reference
- ±5 V Regulators
- Digital and Analog Patch Areas

Description

The CDB5126 Evaluation Board allows fast evaluation of the CS5126 2-Channel, 16-bit Analog-to-Digital Converter.

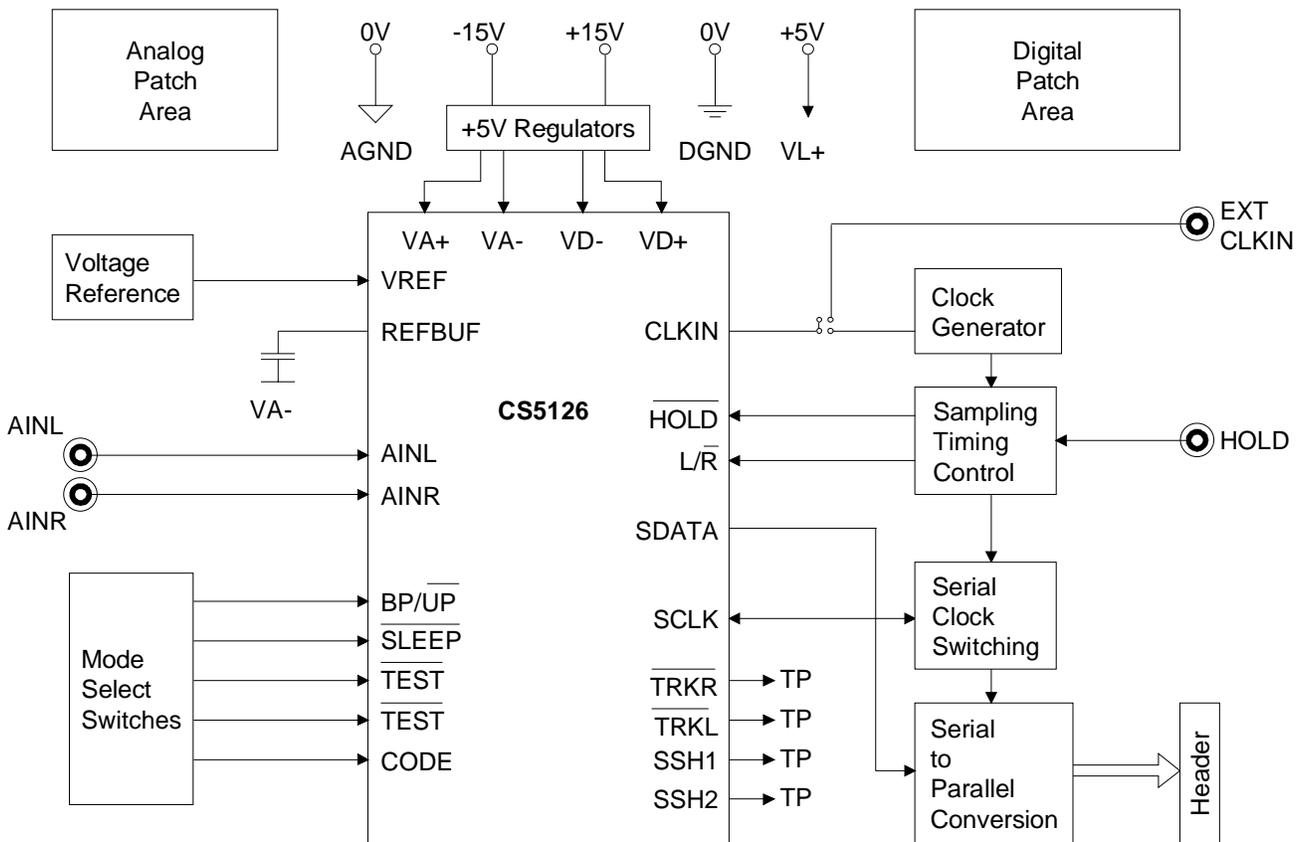
Analog inputs are via BNC connectors. Digital outputs are available both directly from the ADC in serial form, and in 16 bit parallel form.

An adjustable monolithic voltage reference is included.

ORDERING INFORMATION

CDB5126

Evaluation Board



Power Supplies

Figure 1 shows the power supply arrangements. The analog section of the board is powered by ± 15 volts, which is regulated down to ± 5 V for the ADC. A separate +5 V digital supply is required to power the discrete logic. Be sure to switch on the ± 15 V at the same time as, or before, the +5 V logic supply. This will make sure that the CLK and other logic signal are not driving the part before it is powered.

Analog Input

The analog input range is either $\pm V_{ref}$ in the bipolar mode or 0 V to $+V_{ref}$ in the unipolar mode. The voltage reference is factory set to the recommended value of +4.5 volts, so the typical input signal ranges become ± 4.5 volts or 0 V to +4.5 V.

The source driving the analog inputs should have a low ($< 200 \Omega$ at high frequency) output impedance. Be careful not to overdrive the inputs outside the power supplies of the ADC (± 5 V). Figure 2 shows the buffer circuit used at the Crystal factory to drive the ADC when performing FFT testing. See the CS5126 data sheet for example FFT test results.

Voltage Reference

As shown in Figure 3, an LT1019-5 voltage reference provides a stable 4.5 V reference for the ADC. An optional OP27 buffer filters out excess reference noise and provides a very low output impedance. To try the unbuffered LT1019-5 directly, solder in J2 and cut the VREF trace. Alternatively the shunt reference based reference schematic given in the CS5126 data sheet can be evaluated by adding it to the analog patch area.

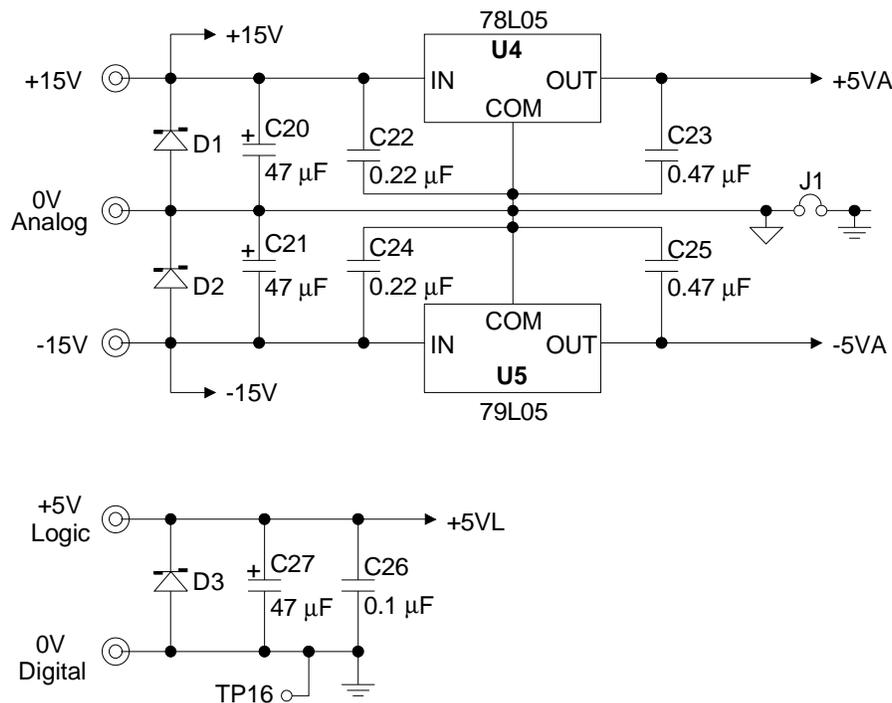


Figure 1. Power Supplies

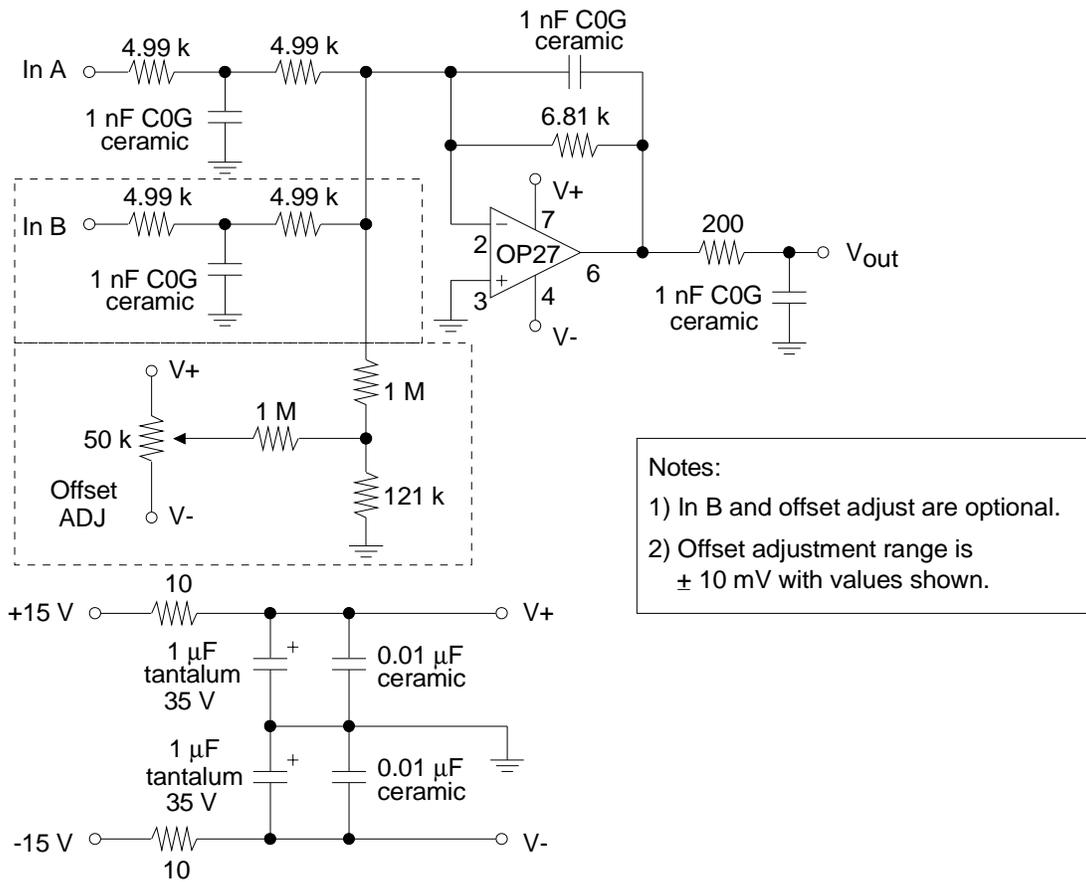


Figure 2. Example Input Buffer Circuit (not provided on the CDB5126 evaluation board)

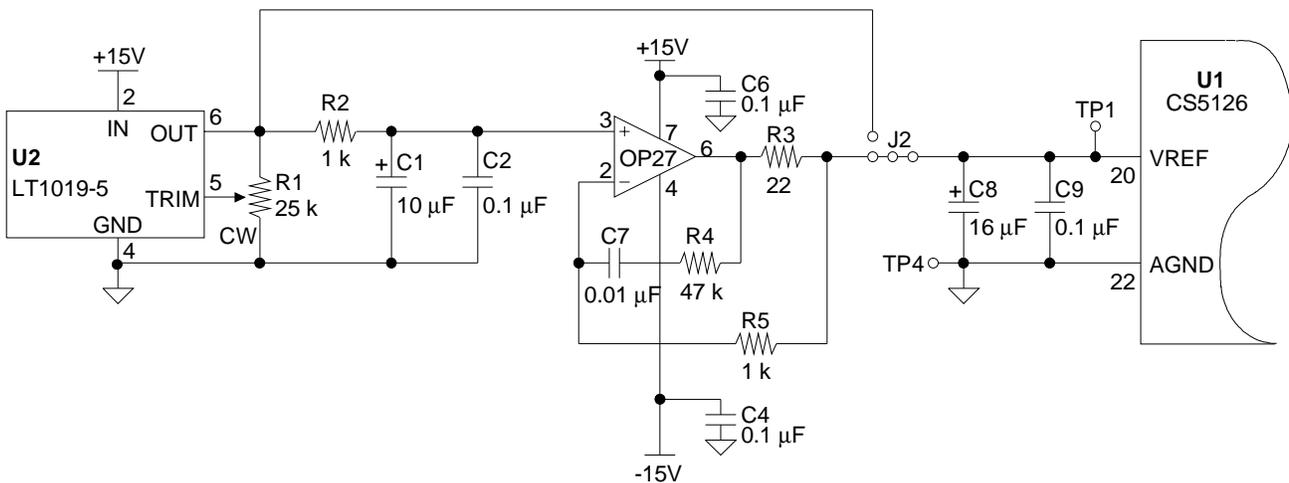


Figure 3. Voltage Reference

A 5 volt reference can be used provided the supplies to the ADC are elevated to ± 5.3 volts. This can be done by inserting $22\ \Omega$ resistors in series with the regulator (U4 and U5) common leads.

Master Clock

The CS5126 requires an external 24.576 MHz clock for a 96 kHz sample rate. A 24.576 MHz clock oscillator module (U6) is provided. An external clock can also be selected by P1, via a

BNC connector. R15 is an optional $75\ \Omega$ terminating resistor for the external clock BNC.

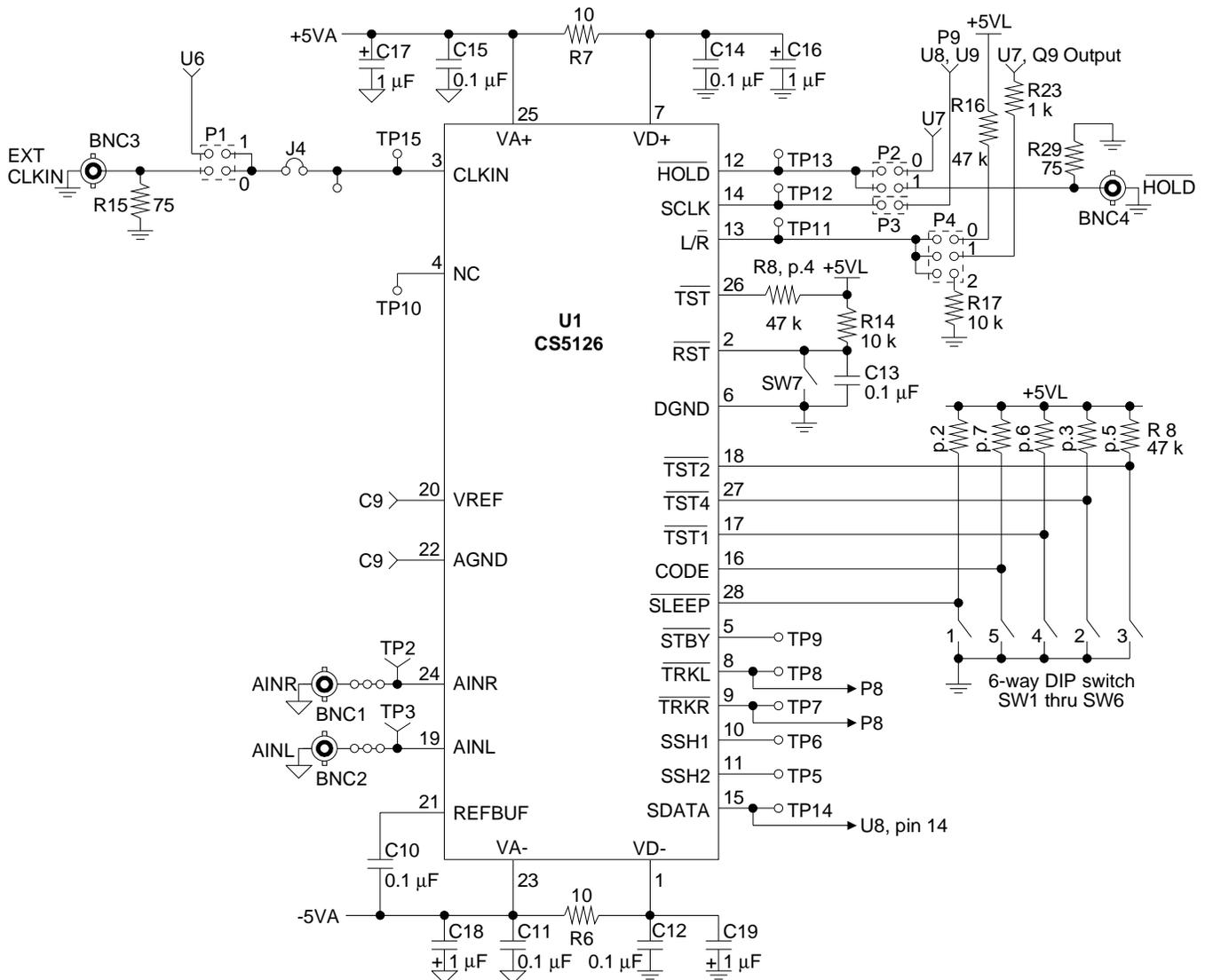


Figure 4. ADC Connections

Sampling Clock Generation Logic

The CS5126 requires an external serial clock to clock out the data. The CDB5126 board has the logic necessary to generate the master clock, $\overline{\text{HOLD}}$, L/R, and SCLK to allow fast evaluation of the ADC. In most systems, these timing signals will be available from the main timing section, typically generated by a logic array of some variety. $\overline{\text{HOLD}}$ may be brought in externally via a BNC, optionally terminated by R29. SCLK and $\overline{\text{L/R}}$ select may be brought in externally via test points and removing jumpers.

Figure 5 shows the on-board clock generation circuitry. U7 (74HC4040) produces binary divided ratios of the 24.576 MHz master clock. Q4 generates a 1.5 MHz clock, which is used for SCLK. Q8 generates a 96 kHz clock, used for $\overline{\text{HOLD}}$, and Q9 generates a 48 kHz clock, option-

ally used to toggle $\overline{\text{L/R}}$ select. This set of clocks causes the CS5126 to continuously convert, generating a continuous stream of serial data bits. To correctly identify the last bit of each word, U12 produces a pulse only when Q4, Q5, Q6, Q7, Q8, and optionally Q9 are all high. This state is latched by U10A to prevent any glitches, and the resulting signal (attached to TP18) is used to latch the U8-U9 shift registers.

Serial to Parallel Conversion

Figure 6 shows the serial to parallel conversion circuit. Two 74HC595 shift register/latches connected in series with SDATA assemble 16-bit, parallel words, clocked by SCLK. As discussed above, the outputs are latched inside the 74HC595 at the end of each 16-bit word. The outputs are brought out to a 40-way header (P5). Only low capacitance, twisted pair, ribbon cable should be used.

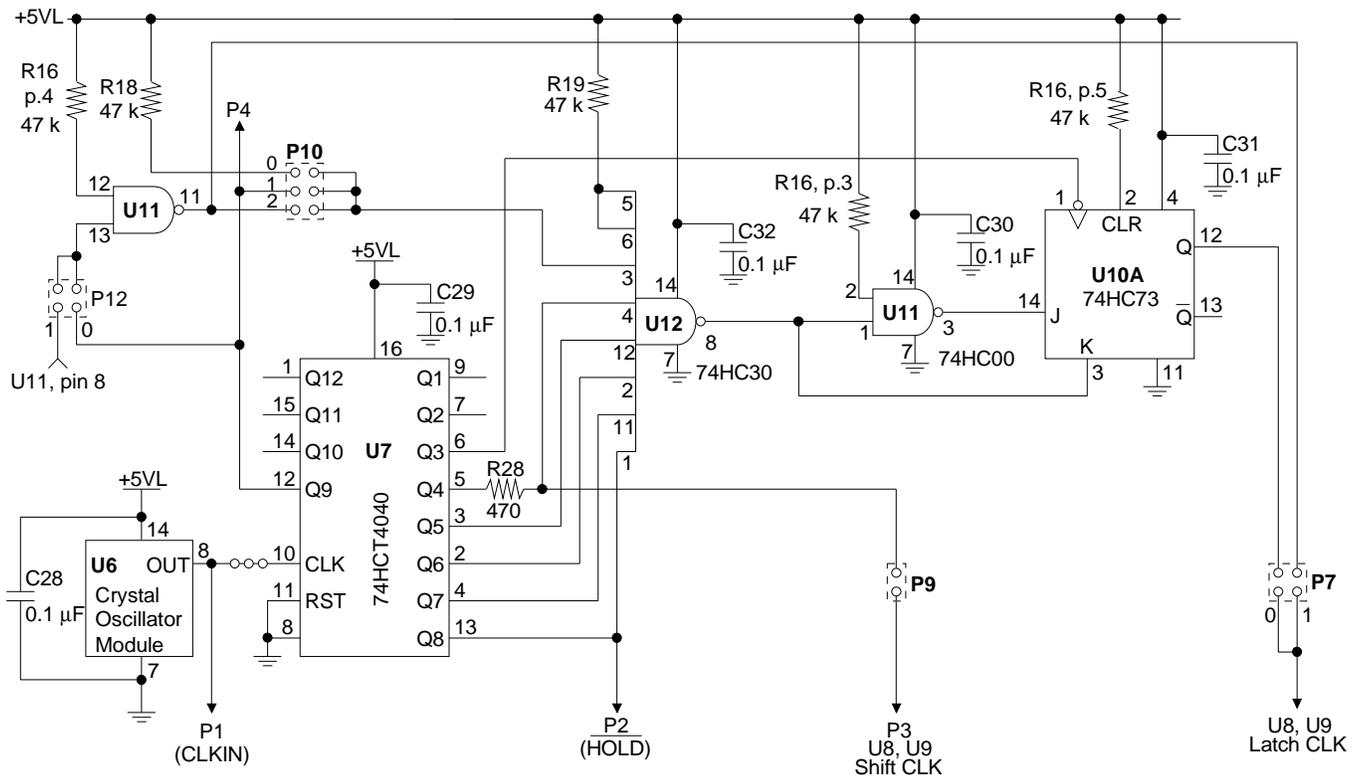


Figure 5. Timing Generator

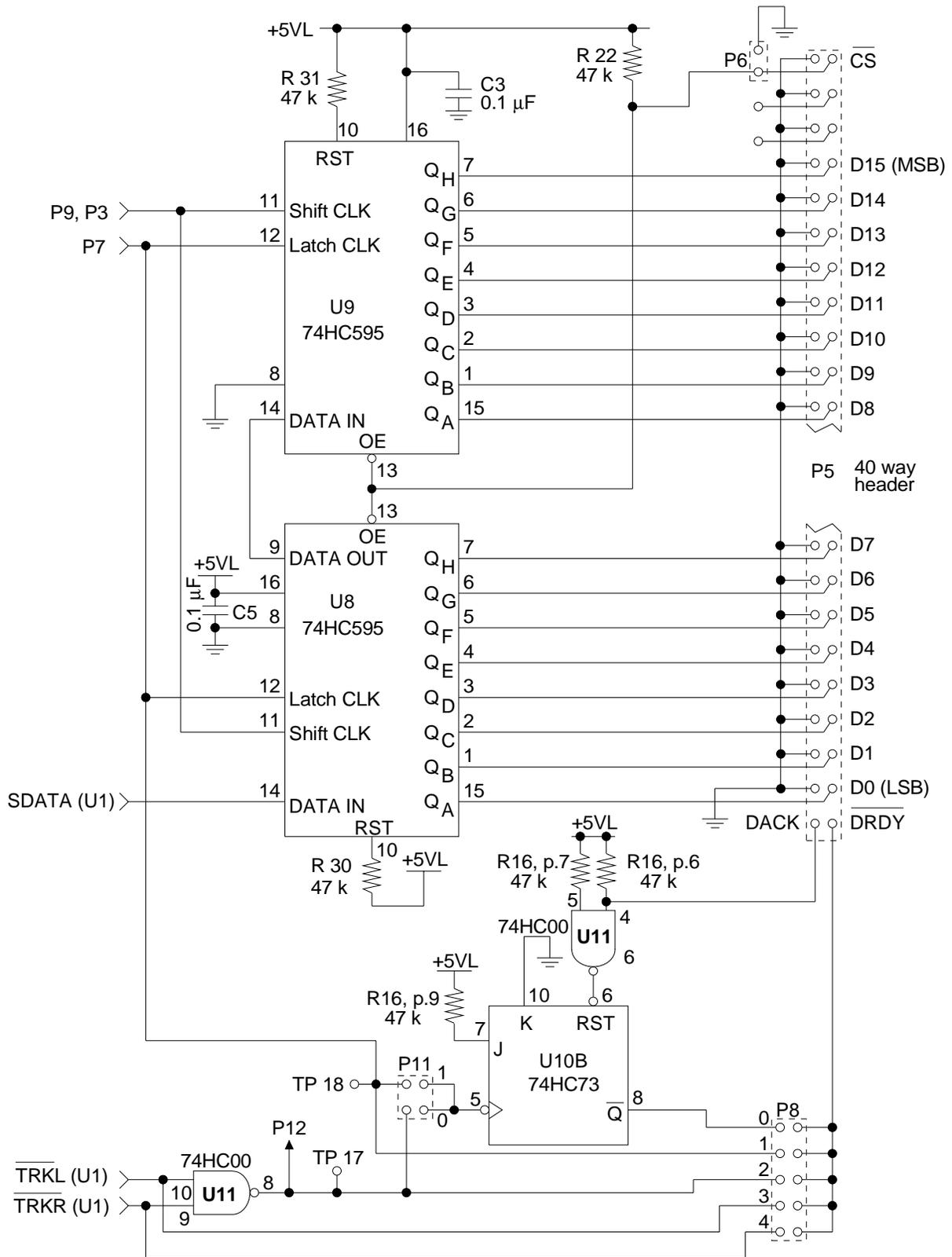


Figure 6. Serial to Parallel Converter

- J1 - Joins analog ground to digital ground on the board.
- J2 - Joins LT1019-5 reference directly to the VREF pin on the ADC. Before doing this, break the connection between R3 and the ADC VREF pin by using a twist drill to remove the central feedthrough. This option allows evaluation of different reference configurations.
- J4 - Connects an external clock to CLKIN on the ADC.

Table 1. Solder Link Options

- P1 0 - Select external clock via BNC connector
- * 1 - Select on-board clock generated by U6.
- P2 * 0 - Select on-board generated $\overline{\text{HOLD}}$.
- 1 - Select external $\overline{\text{HOLD}}$ via BNC connector.
- P3 * Connect SCLK to on-board shift registers.
- P4 * 0 - Pull $\overline{\text{L/R}}$ select pin high, selecting the left channel only.
- 1 - Drive $\overline{\text{L/R}}$ select at 48 kHz from the on-board timing generator.
- 2 - Pull $\overline{\text{L/R}}$ select pin low, selecting the right channel only.
- P6 * Connect the $\overline{\text{OE}}$ pins of the shift registers to ground. Permanently enables the 3-state output buffers.
- P7 * 0 - Connects the on-board Data Ready signal to the shift registers.
- 1 - Connects the NAND gate outputs (U11, pin 11) to the shift registers.
- P8 * 1 - Connects the un-latched on-board Data Ready signal to P5.
- 2 - Connects $\overline{\text{TRKL}}$ and $\overline{\text{TRKR ANDED}}$ together to P5. This signal can be used as an "End of Convert" indicator.
- 3 - Connects $\overline{\text{TRKL}}$ to P5.
- 4 - Connects $\overline{\text{TRKR}}$ to P5.
- P9 * Connects the on-board generated SCLK to the rest of the on-board circuitry.
- P10 * 0 - Causes the on-board Data Ready generating circuit to flag data ready every conversion.
- 1 - Causes the on-board Data Ready generating circuit to flag data ready every left conversion. P4 must be in position 1 for this to work.
- 2 - Causes the on-board Data Ready generating circuit to flag data ready every right conversion. P4 must be in position 1 for this to work.
- P11 0 - Connects $\overline{\text{TRKL}}$ & $\overline{\text{TRKR}}$ to U10B, the handshake flip-flop.
- * 1 - Connects the on-board data ready signal to U10B.
- P12 * 0 - Allows selection of the $\overline{\text{DRDY}}$ signals for alternate channels.
- 1 - Connects the $\overline{\text{TRKL}}$ & $\overline{\text{TRKR}}$ to U11, pin 13.

* Factory default state for CS5126

Table 2. Shorting Plug Selectable Options

U10B (74HC73) is used as a handshake flip-flop with the computer system attached to the evaluation board. The board brings DRDY low. The computer reads the data and then sets DACK momentarily high. This resets U10B for the next word. This handshake can be disabled by setting P8 jumper to position 1.

DIP Switches

Figure 7 and Table 3 shows the DIP switch selectable options.

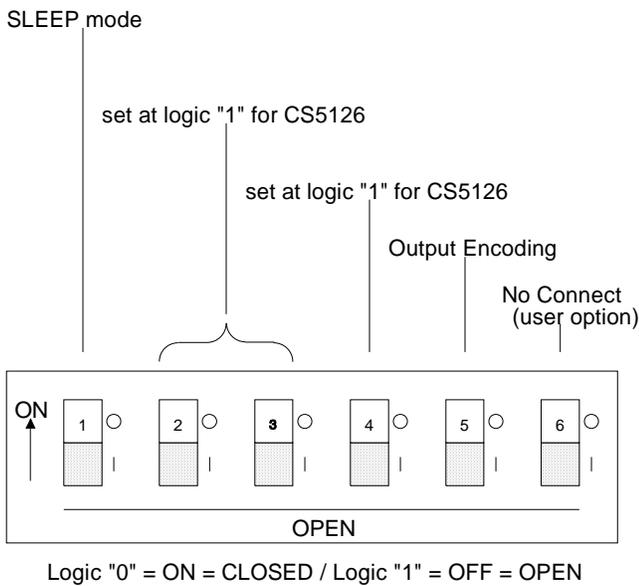


Figure 7. DIP switch configuration

Switch	Logic	Mode
1	0	SLEEP mode
	1	Normal mode
2, 3, 4		set to "1" for CS5126
5	0	Offset binary output code
	1	2's complement output code
6		Unconnected. Available for user's applications

Table 3. DIP Switch Selection Options

Test Points

Table 4 is a list of the test points provided on the Evaluation Board.

	CS5126
TP1	VREF
TP2	AINR
TP3	AINL
TP4	AGND
TP5	SSH2
TP6	SSH1
TP7	TRKR
TP8	TRKL
TP9	STBY
TP10	NC
TP11	L/R
TP12	SCLK
TP13	HOLD
TP14	SDATA
TP15	CLKIN
TP16	DGND
TP17	TRKL + TRKR
TP18	Latch Clock for the 74HC595 shift registers

Table 4. CDB5126 Test Points

Miscellaneous Hints on Using the Evaluation Board

Always hit the reset button after powering-up the board. The CS5126 is self calibrating and require the reset signal to initiate the calibration procedure.

P4 controls the ADC input mux. This is used to set the mux to be continuously connected to one channel, or to be toggling between two channels. This is very useful for evaluating oversampled vs. regular sampling digital audio.

P10 controls the Data Ready pulses from the on-board logic. To cause every data sample to be read, select option 0. If you wish to read only every alternate sample, then select option 1 or 2, depending on whether you wish to read every left channel value, or every right channel value. This is useful for evaluating the part with a test system which does not separate alternate values.

CDBCAPTURE Interface

Figure 8 illustrates the CDBCAPTURE interface that can be constructed in the digital patch area. A 2-row, 10 pin stake header is wired as shown.

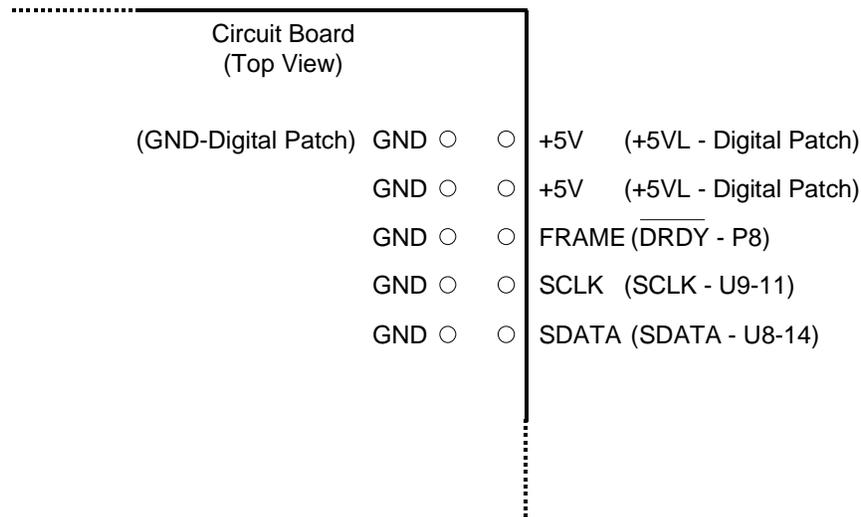


Figure 8. CDBCAPTURE Header Signal Pattern

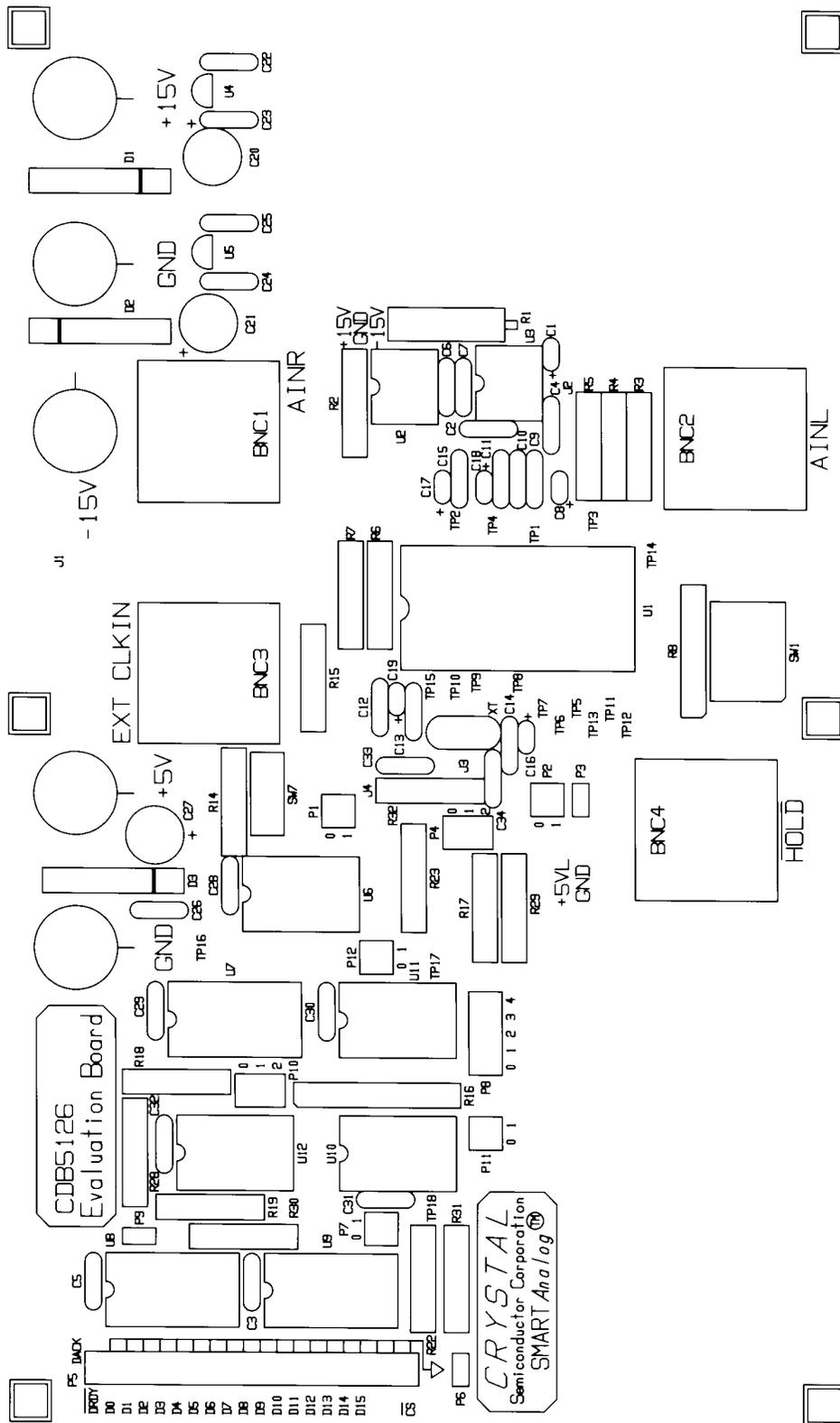


Figure 9. CDB5126 Component Layout

• **Notes** •

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