PCS42

CHARACTERISTICS

Microprocessor	i486 SX @ 25 MHz i486 SX @ 33 MHz i486 DX @ 33 MHz i486 DX2 @ 50 MHz internal (25 MHz system) i486 DX2 @ 66 MHz internal (33 MHz system)
Clock	25 MHz or 33 MHz
Architecture	ISA / VESA
Memory	From 4 MB to 112 MB on the motherboard. The motherboard has three banks in which can SIMMs can be installed . **Bank A** Consisting of four 30-pin sockets **Bank B** Consisting of one 72-pin socket **Bank C** Consisting of one 72-pin socket The motherboard comes with four 1 MB x 9 (4 MB) SIMMs installed in bank A. - Memory in **bank A** can be expanded using the following expansion kit: **EXM-821/D** 16 MB - Four 4MBx9 SIMMs (existing SIMMs have to be replaced) - Memory in banks B and C can be expanded using the following expansion kits: **EXM 28-004** 4 MB - One 1MBx36 SIMM **EXM 28-008** 8 MB - One 2MBx36 SIMM **EXM 28-016** 16 MB - One 4MBx36 SIMM These systems can also accomodate SIMMs commercially available (with a 70 ns access time and FAST PAGE MODE). **Note:** In the 112 MB memory configuration (64 + 16 + 32), the 32 MB SIMM must installed in **bank C** and not in **bank B**.
Memory access time	70 ns
Video controller	Video control functions can be provided by any one of the following boards: - **GO 2030 (1580)** - AT board with 1 MB of video RAM. - **VD-5428** - VESA board with 1 MB of video RAM expandable to 2 MB. - **VGA-542VT** - VESA board with 1 MB of video RAM expandable to 2 MB.
Streaming Tape	**Irwin 31250A** 80/120 MB Floppy interface
HDU and FDU controllers	**I/O controller board for TIN BOX cases** - SUPER I/O board - PRIME IIC **I/O controller board for SLIM TIN BOX cases** - Super I/O board

Continues

CASE

BOX TIN

BOX TIN SLIM

See the appropriate section in this Chapter.

MOTHERBOARD

MICROSTAR

BIOS

Last level:

POWER SUPPLY

TIN BOX Case
ASTEC SA 201 3450
115 V / 230 V 200W

SLIM TIN BOX Case
ASTEC SA100 3430
115 V / 230 V 100W

DSP 0584 100AG
115 V / 230 V 100W

Secondary level cache memory	The motherboard is equipped with sockets into which secondary level cache memory chips can be installed. Bank 1 consists of sockets U1-U4. Bank 0 consists of sockets U6-U9. Socket U10 hosts the TAG RAM chip. The following cache capacities cn be obtained: 64KB 8 8Kbx8 SRAM chips (bank 0 and 1) 1 28-pin TAG RAM chip 128 KB 4 32Kbx8 SRAM chips (bank 0) 1 28-pin TAG RAM chip 256 KB 8 32Kbx8 SRAM chips (bank 0 & 1) 1 28-pin TAG RAM chip The access time is 20 ns. **Note:** The **128 KB** cache memory configuration is used. The 64 KB and 256 KB configurations are not used.
Floppy Disk	Panasonic JU 257 A 1.44 MB Sony MP-F17 W / MPF420-1 1.44 MB Mitzumi D359T3 1.44 MB Y-E DATA YD-702B / Y-E DATA YD-702D 1.44 MB TEAC FD235HF 1.44 MB Mitsubishi MF 355 1.44 MB EPSON SMD 1040-418 1.44 MB Panasonic JU 475-3 / JU 475-4 JU 475-5 1.2 MB Canon MD 5501-64 1.2 MB
Hard Disk	170 MB QUANTUM LPS 170 AT 210 MB W.D. AC1210 210 MB CONNER CFS210A (local BUS) 210 MB SEAGATE ST3250A 210 MB QUANTUM LPS210 AT (local BUS) 270 MB QUANTUM LPS270 AT (local BUS) 270 MB CONNER CFA270 A (local BUS) 340 MB QUANTUM LPS 340 AT 340 MB W.D. AC2340 340 MB SEAGATE ST3391A 420 MB SEAGATE ST3491A 420 MB W.D. AC2420 420 MB CONNER CFS420A (local BUS) 540 MB QUANTUM LPS540 AT (local BUS) 540 MB CONNER CFA540 A (local BUS)
Slots	**TIN BOX** Slots on the motherboard: - Four AT full-size - Three shared AT/VESA **SLIM TIN BOX** Slots on the bus board - Two AT full-size, one shared AT/VESA
Mouse	400 dpi 3-button serial mouse which connects to the serial port of the I/O board.
Keyboard	101/102-key ANK 27-101/N, ANK 27-102/N 101/102-key ANK 28-101, ANK 28-102 Super compact keyboard. An adapter cable is required to connect the keyboard to the basic module.

BUS EXPANSION BOARD

Only used in models with a SLIM TIN BOX case.

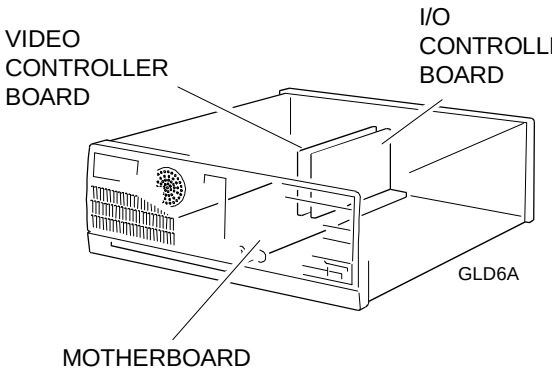
CONFIGURATION UTILITIES

The configuration utilities for this system are stored in the BIOS.

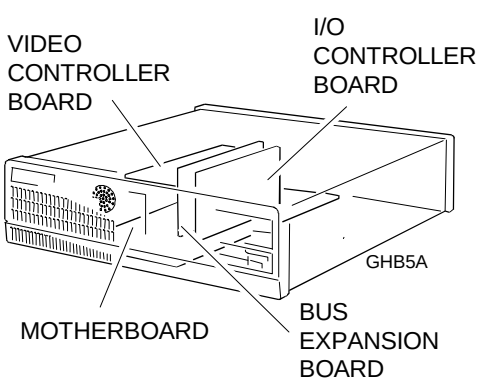
SYSTEM CASES

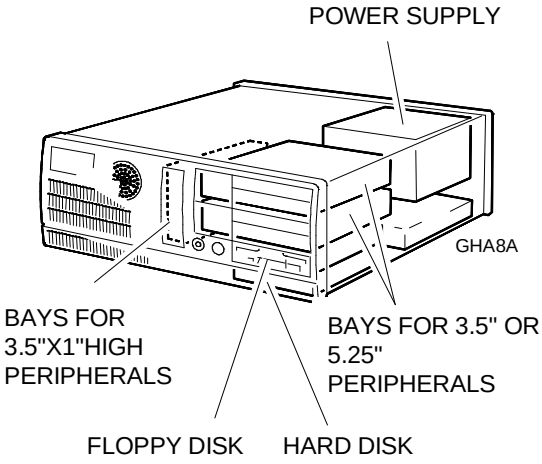
The following figure shows this personal computer's two system cases, in addition to the boards and peripherals installed in each type of case.

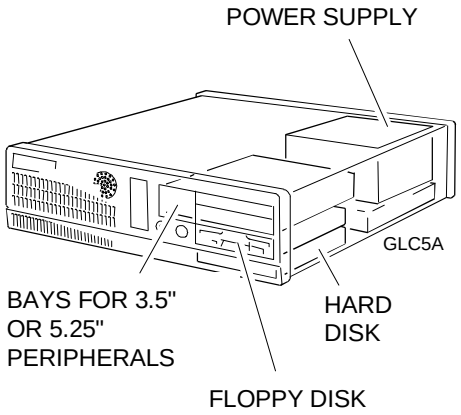
TIN BOX



SLIM TIN BOX







MOTHERBOARD

	LEVEL	D.R.S. CODE	ROM BIOS	NOTES
MICROSTAR	Nasc.			System motherboard.

MOTHERBOARD INTEGRATED CONTROLLERS

MOTHER-BOARD	INTEGRATED CONTROLLERS
	CPU 25 MHz or 33 MHz i486SX processor in QFP package (soldered) **Processor Socket** The following PGA processors can be installed in this socket: - i486 SX @ 25 or 33 MHz - i486 DX @ 25 or 33 MHz - i486 DX2 @ 50 or 66 MHz **M1429** Chip set component which offers the following functions: - DRAM control - Cache control - ISA bus control - Keyboard control - Real Time Clock - CMOS RAM **M1431** Chip set component which offers address and data bus buffering. **27512** 512 KB EEPROM containing the system BIOS. **8042** Keyboard controller **U1/ U10** Sockets for secondary level cache memory chips.

VIDEO CONTROLLER BOARDS

BOARD	LEVEL	NOTES
GO2030 (1580)	Nasc.	AT board with 512 KB of video RAM expandable to 1 MB
VD - 5428	Nasc.	VESA board with 1 MB of video RAM expandable to 2 MB
VGA - 542 VT	Nasc.	VESA board with 1 MB of video RAM expandable to 2 MB

I/O CONTROLLER BOARDS

BOARD	LEVEL	NOTES
Super I/O board	Nasc.	I/O controller board for TIN BOX cases
PRIME IIC	Nasc. Lev. 01	I/O controller board for TIN BOX cases The BALE signal output by the hard disk is cut to correct the problem of noise disturbance on the 1570 SX video controller (**GO2021**). This noise is caused by the CONNER 210 A hard disk
Super I/O board	Nasc.	I/O controller board for SLIM TIN BOX cases

ENHANCED VIDEO DRIVER

DRIVER	NOTES
EVD for the GO2030 (1580) - Ver. 1.02 video controller	

SYSTEM TEST

LEVEL	NOTES
Rev. 1.00	The video test does not work with the 1580 SX video controller board. New version which includes new keyboard, video and floppy disk tests.

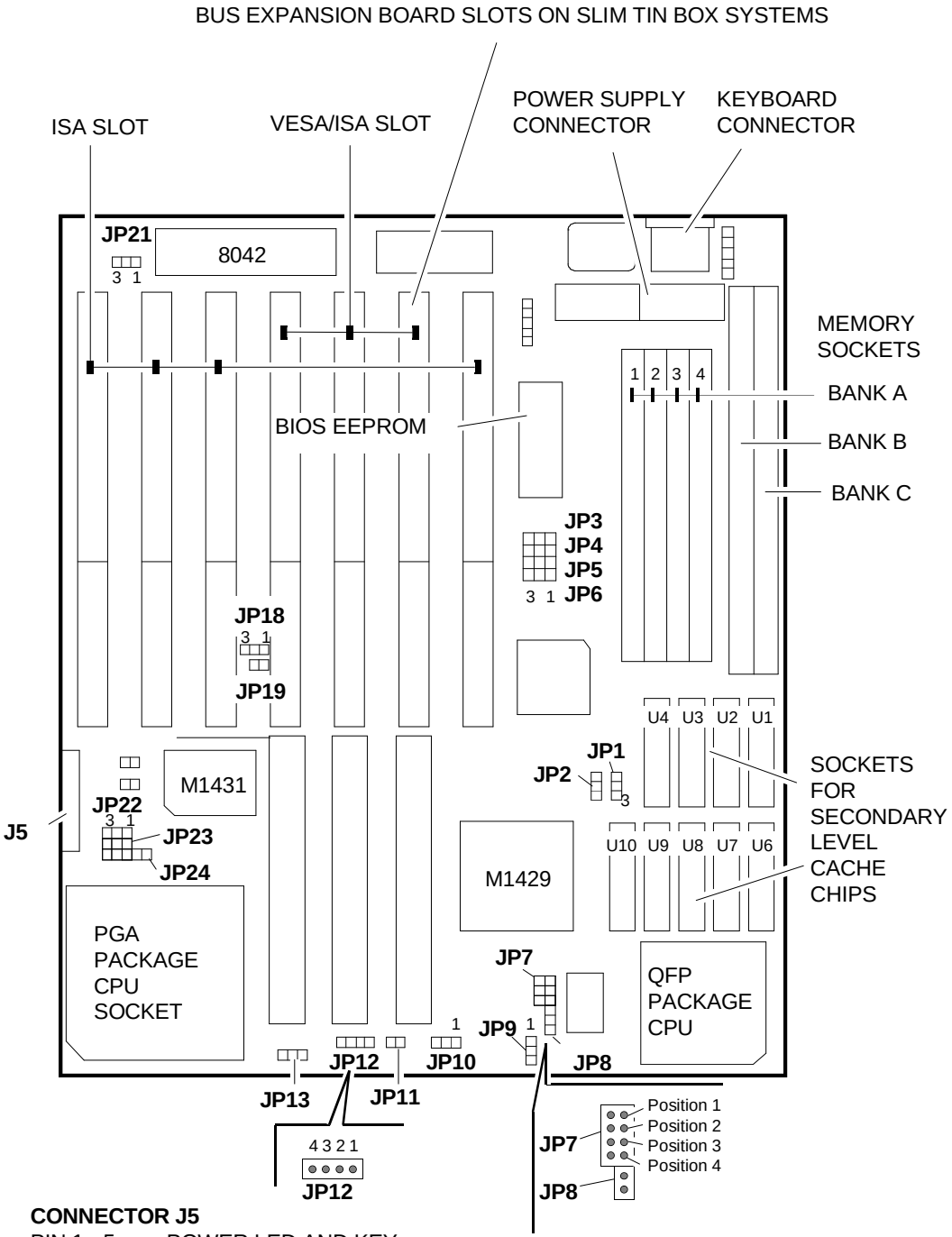
BIOS

LEVEL	NOTES

POWER SUPPLY

POWER SUPPLY	LEVEL	DESCRIPTION
SA201 3450	Nasc.	200 W power supply for **TIN BOX cases.**
	Lev. 01	To reduce EMI noise, the BEAD PN 35052B ferrite is installed on the center pin of mosfet Q1, and diode D2 is removed.
	Lev. 02	To : - comply with ENERGY STAR (EPA) requirements, and - ensure that power supply powers off correctly the modifications were made: - Components D8 - Q4 - R46 - C9 were added to the already preset printed circuit. - A 33 K 1/6 W resistor was added to the primary of the primary of the power supply. A new supplier for the 2.200 uF-16V C23 capacitor is used. Besides NCC, also RUBICON will now supply this component.
	Lev. 03	- The layout of the Power Good board is optimized so that capacitors C125 and C126, previously volatile, can now be installed on the printed circuit. - Renewed motherboard printed circuit so that the R62 and Z5 components can be added. - New alternative suppliers for the following components: C1 - C2 (ISKRA and RIFA) - C12 (EVOX and ARCOTRONICS) - T1 (EDT39).
	Lev. 04	Some power supply components were removed to cut production costs.
ASTEC SA100 3430	Nasc	100 W power supply **for SLIM TIN BOX cases.**
	Lev. 01	Modification made to the fan regulation circuit. From a High Speed model, the fan now becomes a Medium Speed model. This modification was implemented to correct the problems given by the systems supplied to MERCEDES.
	Lev. 02	To correct: - Excessive ripple on the +12 V - Low power supply yield - Power Good problems the following modifications were made: - The SGS THOMSON alternative for the IC3 regulator was eliminated - Zener Z102 was changed from HZ11C2 to HZ11C3 - Capacitor C64 was changed from 470 pF to 2,200 pF This level does not include the modifications made in level 01 (specific for MERCEDES).
	Lev. 03	Modified fan circuitry to include the level 01 modifications on all the power supplies.
DSP 0584 100AG	Nasc	100 W power supply **SLIM TIN BOX cases**.

COMPONENTS AND JUMPERS ON THE MOTHERBOARD



CONNECTOR J5

PIN 1 - 5	POWER LED AND KEY
PIN 7 - 10	SPEAKER
PIN 12 - 13	TURBO LED
PIN 15 - 17	TURBO BUTTON
PIN 19-20	HARDWARE RESET

EWU2A

JUMPERS

JUMPER	FUNCTION	SETTING
JP24	CPU selection	OUT = Soldered CPU (PQFP) IN = On-socket CPU (PGA)

CPU SELECTION JUMPERS	i486 SX	i487 SX	i486 DX / i486 DX2
JP18	On 1-2	On 2-3	On 2-3
JP22	OUT	On 1-2	On 3-2

CPU CLOCK SELECTION JUMPERS	25 MHz	33 MHz	40 MHz	50 MHz
JP6	On 1 - 2	On 1 - 2	On 2 - 3	On 2 - 3
JP7	Jumpers installed in position 3 and 4	Jumpers installed in position 1 and 4	Jumpers installed in position 1 and 2	Jumper installed in position 2
JP8	IN	IN	IN	OUT
JP9	On 1 - 2	On 1 - 2	On 2 - 3	On 2 - 3
JP10	On 1 - 2	On 1 - 2	On 2 - 3	On 2 - 3

CACHE SELECTION JUMPERS	128 KB	256 KB
JP1	On 2 - 3	On 1 - 2
JP2	On 2 - 3	On 1 - 2

VESA BUS CONFIGURATION JUMPERS	FUNCTION	SETTING
JP12	High-speed write setting (VESA bus)	OUT = Zero Wait State On 3 - 4 = 1 Wait State (default)
	CPU speed setting (VESa bus)	OUT = Less than or equal to 33 MHz (default) On 1 - 2 = Greater than 33 MHz
JP21	Monitor type setting	On 2 - 3 = Color monitor On 1 - 2 = Monochrome monitor

CPU TYPE SELECTION JUMPERS

JP23 - JP19
JP13 - JP11
JP3 - JP4
JP5

Configuration of the type of CPU installed in the system - These jumpers are factory set.

I/O ADDRESS MAP

ADDRESS	FUNCTION
0 - 0F h	DMA controller #1
20 - 21 h	Interrupt controller #1
40 - 43 h	Timer counter
60 h , 64 h	Keyboard controller
61 h	Port B
70 h	Real Time Clock index register/NMI enable
71 h	Real Time Clock data register
80 - 8F h	DMA page registers
90 h	Custom I/O port #1
91 h	Custom I/O port #2
92 h	PS/2-compatible FAST GATE A20 and FAST RESET
94 h	Video controller system Setup register
102 h	Video controller system Setup register
A0 - A1 h	Interrupt controller #2
EC - ED h	Chipset configuration ports
EE h	FAST A20 (alternative)
EF h	FAST CPU reset port (alternative)
F0 h	Coprocessor busy register
F1 h	Coprocessor reset register
F4 h	CPU slow register
F5 h	CPU fast register
F9 h	Chipset configuration register disable
FB h	Chipset configuration register enable
0C0 - 0DF h	DMA controller #2
1F0-1F7 h	IDE hard disk registers
201 h	Game port
278 - 27F h	Alternative LPT2 parallel port
2B0 - 2BF h	EGA video
2C0 - 2CF h	EGA video
2D0 - 2DF h	EGA video
2E8 - 2EF h	Alternative COM4 location for serial port B
2F8 - 2FF h	Primary COM2 location for serial port B
378 - 37F h	Primary LPT1 parallel port
3B0 - 3BB h	MDA video
3B4 / 3D4 h	VGA video
3B5 / 3D5 h	VGA video
3BA / 3DA h	VGA video
3C0 - 3CF h	EGA/VGA video
3D0 - 3DF h	CGA video
3F0 - 3F7 h	Floppy disk drive location
3E8 - 3EF h	Alternative COM3 location for serial port A
3F8 - 3FF h	Primary COM1 location for serial port A

DMA CHANNELS

CHANNEL	NUMBER OF BITS	FUNCTION
0	8 or 16	Free
1	8 or 16	Free
2	8 or 16	Floppy disk transfers
3	8 or 16	Free
4	16	Used for the cascade connection of DMA1
5	16	Free
6	16	Free
7	16	Free

INTERRUPT LEVELS

INTERRUPT	FUNCTION
IRQ1	Counter timer
IRQ2	Cascade input of the second interrupt controller
IRQ3	COM2 interrupt
IRQ4	COM1 interrupt
IRQ5	LPT1
IRQ6	Floppy drive
IRQ7	LPT2
IRQ8	Real Time Clock
IRQ9	Not used
IRQ10	Not used
IRQ11	Not used
IRQ12	Mouse
IRQ13	Math coprocessor
IRQ14	IDE drive controller
IRQ15	Not used

SYSTEM MEMORY MAP

ADDRESS RANGE	FUNCTION
00000h - 7FFFFh	512 KB system memory
80000h - 9FFFFh	128 KB system memory / optional ISA mapping
A0000h -BFFFFh	Text and graphics memory (on the motherboard)
C0000h - CFFFFh	Video BIOS
D0000h - DFFFFh	Extended ROM BIOS / expansion for the I/O channels
E0000h - EFFFFh	Video BIOS
F0000h - FFFFFh	System BIOS
100000h - 3FFFFFh	4 MB of system DRAM
400000h - 13FFFFFh	Expansion SIMMs
FFFF0000h - FFFFFFFFh	System BIOS shadow

The entire DRAM area can be cached or not.

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