Cat. No. 25-1504

Tandy 1000

Technical Reference Manual

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Tandy 1000 Computer
25-1504

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10 9 8 7 6 5 4 3 2 1

Table of Contents

INTRODUCTION TO THE TANDY 1000 COMPUTER

The Tandy 1000 Computer is modular in design to allow maximum flexibility in system configuration. The computer consists of a Main Unit, a detachable keyboard with coiled cable, and a monitor. The Main Unit is supplied with one internal floppy disk drive. (A second floppy disk drive is optional.) The standard types of monitors used with the Tandy 1000 are the monochrome composite and the color RGB monitor. Since these units are modular, they may be placed on top of the Main Unit or at any convenient location.

Internal storage is expanded by adding a second 5¼" floppy disk drive. Each disk drive has a capacity of 360K bytes formatted.

The Tandy 1000 has a standard 128K of system RAM. An optional DMA/RAM board allows the Tandy 1000 to be expanded in increments of 128K of RAM. This board will fit into one of the expansion slots. With two fully populated RAM boards installed, the Tandy 1000 will have 640K bytes of maximum RAM allowed by the system memory map.

Other features include a parallel printer port, two built-in joystick interfaces, a speaker for audio feedback, and a light pen interface.

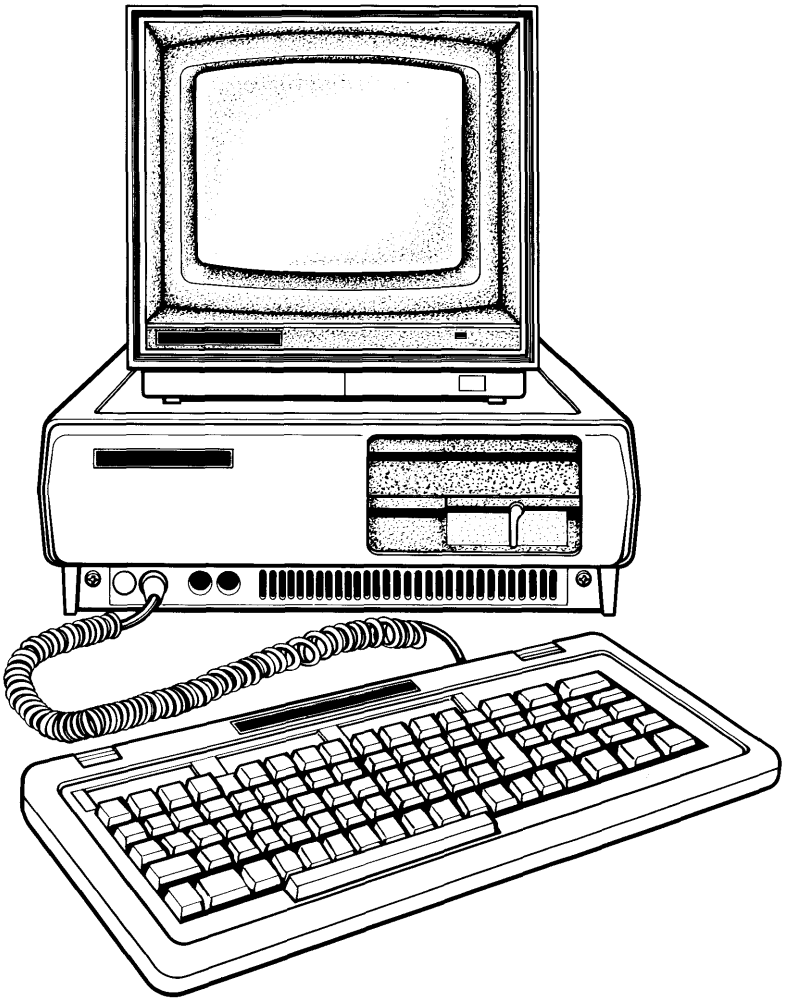
The Main Unit is the heart of the Tandy 1000. It houses the Main Logic Assembly, system power supply, and floppy disk drives.

The Main Logic Assembly is a large board mounted to the bottom of the Main Unit and interconnected to the keyboard, power supply, and disk drives by a series of cables. The illustration in Figure 1 shows the major components of a Tandy 1000 system.

The Power Supply is a 54W switching regulator type, designed to provide adequate power capacity for a fully configured system using all the option slots.

The Floppy Disk Drive uses 5¼" double-sided, double-density diskettes to read, write, or store data. These are soft sector diskettes. The Disk Drive assembly is installed in the standard unit. The floppy disk stores approximately 360K bytes (formatted) of data. All system programs, with the exception of the system startup sequence, are stored on disk.

Either a monochrome or a color display may be used with the Tandy 1000. The monochrome monitor is a high-resolution green phosphor display which provides excellent visual quality. It features a 12" screen with an anti-glare surface. Each display is capable of 25 lines of 80 characters. The character matrix is 8 wide x 9 high.



Tandy 1000 System
Figure 1

SPECIFICATIONS

Processor: Intel 8088

Dimensions:

6 x 17 x 13 3/8 inches (HWD)

Weight:

17 lbs. 4 oz. with 1 Disk Drive

Power Requirements:

120 VAC, 60 Hz, 1 Amp maximum

With 2 Floppy Disk Drives, 2 Memory Cards, and RS-232:

AC Current: 0.7 – 0.8 Amps with Floppy doing R/W tests.
Leakage Current: 0.5 mA
Disk Drive:

Idle +5 VDC	0.23 Amps	+12 VDC	0.106 Amps
R/W	0.286 Amps		0.295 Amps
R/W	0.2 Minimum		0.550 Max.

Main Logic Board: +5 VDC 4.07 Amps +12 VDC 0.056 Amps
Main Logic Board Option Cards: –12 VDC 0.032 Amps

Environment:

Air Temperature
System ON: 60 to 90 degrees F (15.6 to 32.2 degrees C)
System OFF: 50 to 110 degrees F (10 to 43 degrees C)

Humidity
System ON-OFF: 8% to 80%

Disk Drive Specifications

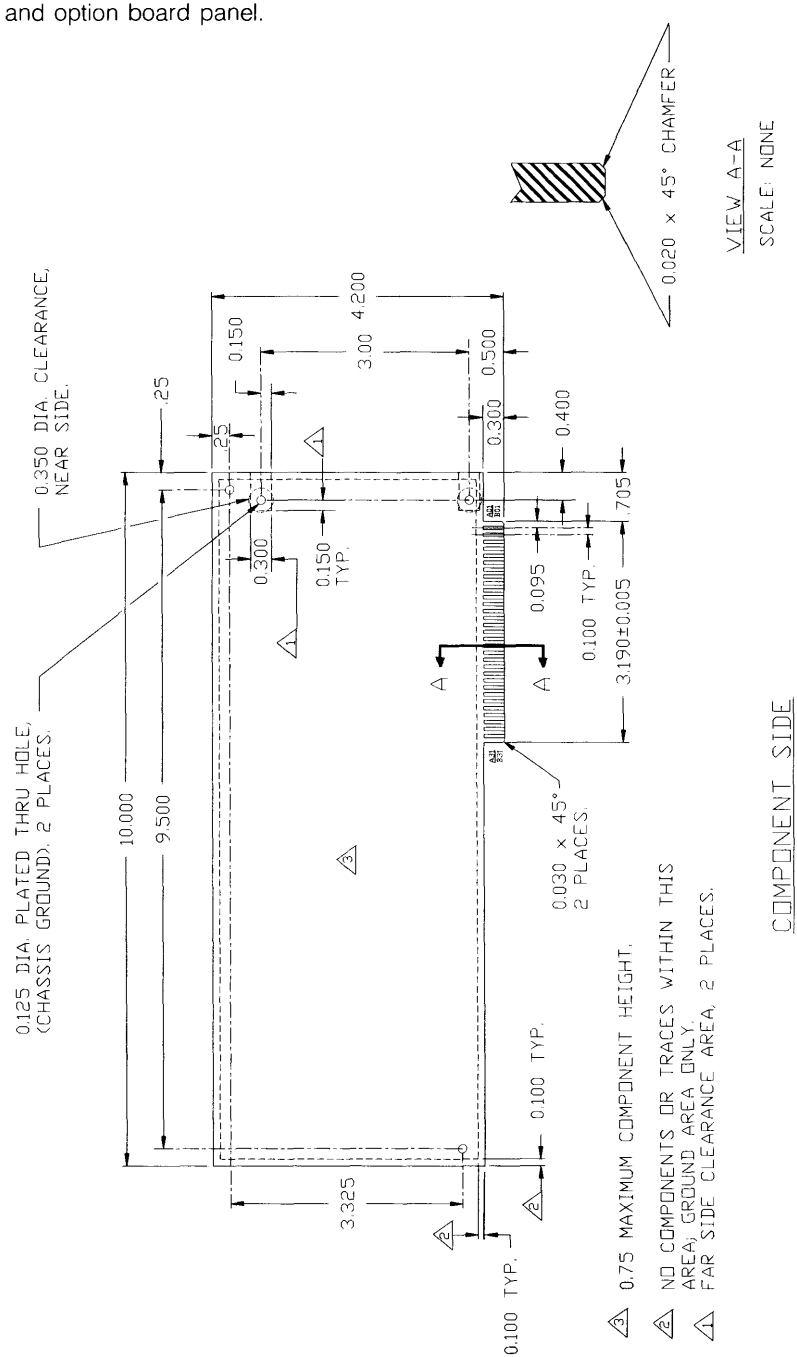
Power:

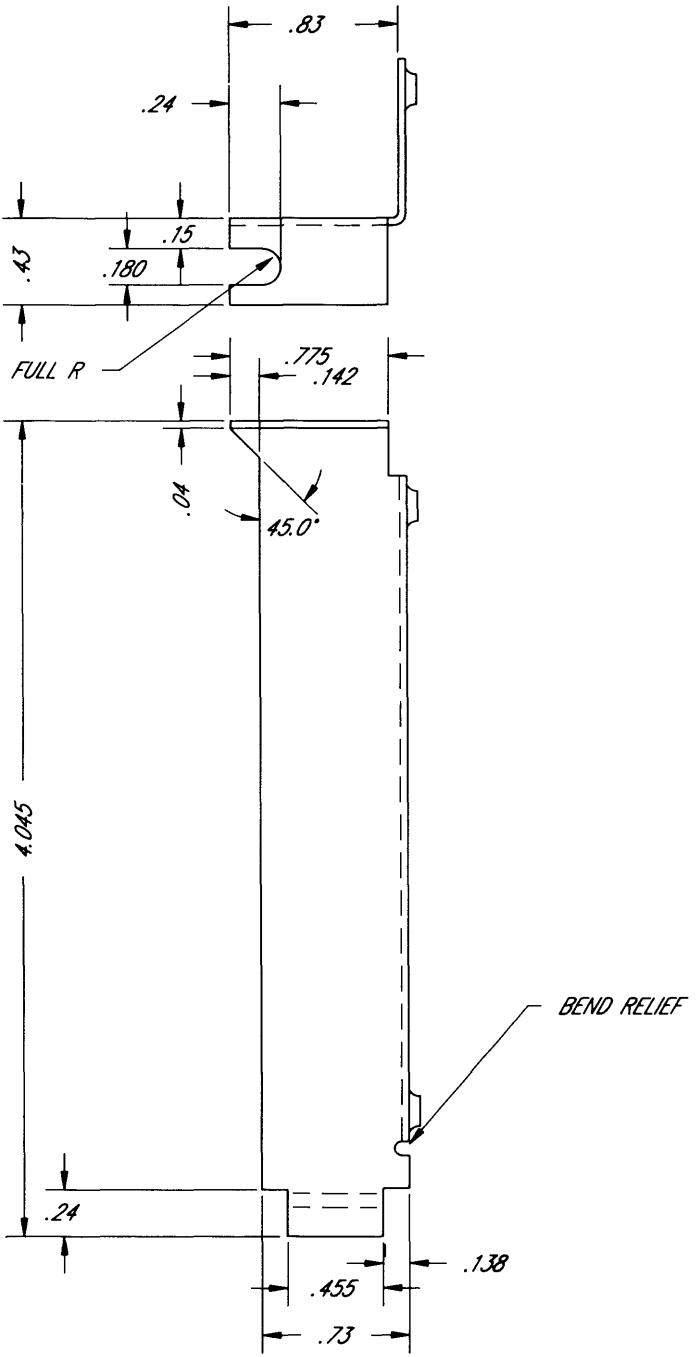
Supply Voltage	+5 VDC Input	+12 VDC Input
Ripple 0 to 50 kHz	100 mV	100 mV
Tolerance Including Ripple	+/–5%	+/–5%
Standby Current		
Nominal	600 mA	400 mA
Worst Case	700 mA	500 mA
Operating Current		
Nominal	600 mA	900 mA
Worst Case	700 mA	2400 mA

Environment:

Temperature	
Operating	50 to 122 degrees F (10 to 44 C)
Nonoperating	–40 to 140 degrees F (–40 to 60 C)
Relative Humidity	
Operating	20% to 80% (noncondensing)
Nonoperating	5% to 95% (noncondensing)

The following pages reflect the mechanics for the Tandy 1000 option PCB's and option board panel.

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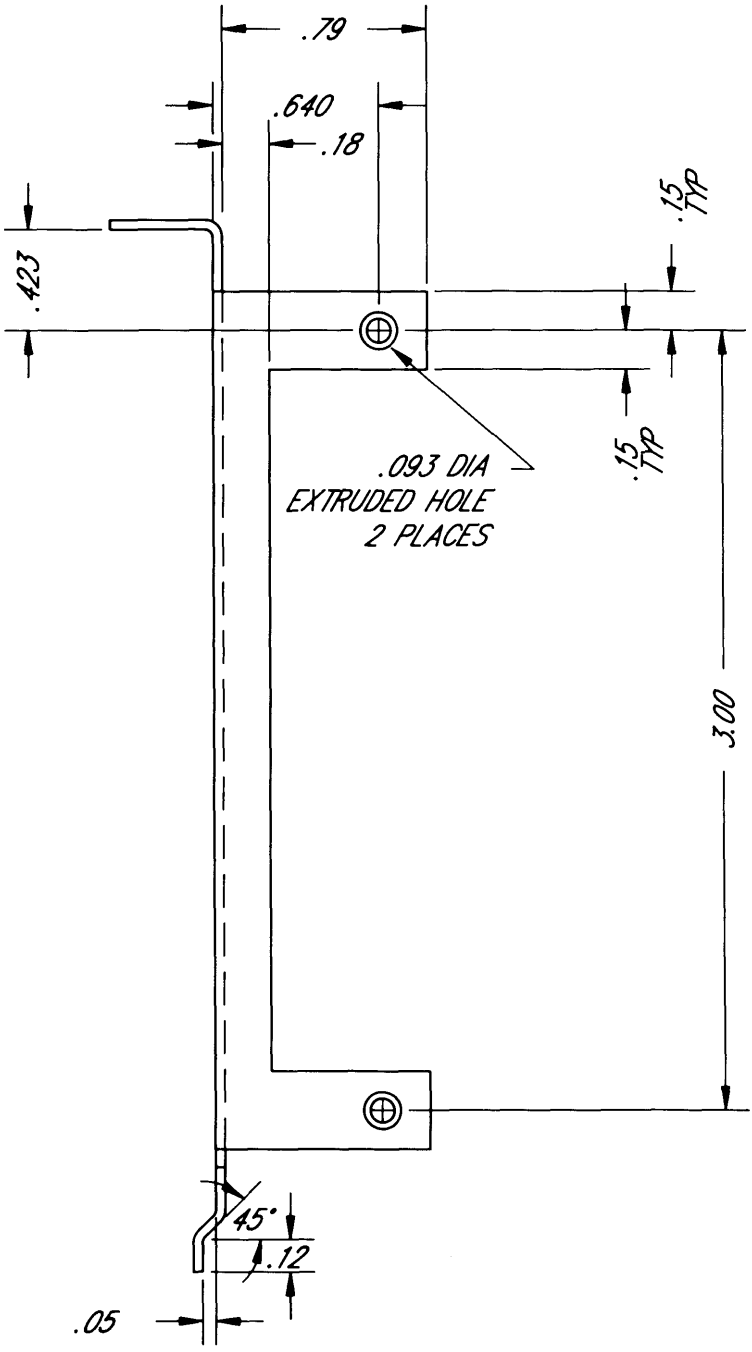
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Connector Pin Assignments

J2 — Speaker Interface
(2-Pin Vertical Header)

1	— Sound	2	— Ground

J3 — Right Joystick
(6-Pin Rt. Angle Circular Din)

1	— Y Axis	2	— X Axis
3	— Ground	4	— Switch 1
5	— +5 VDC	6	— Switch 2

J4 — Left Joystick
(6-Pin Rt. Angle Circular Din)

1	— Y Axis	2	— X Axis
3	— Ground	4	— Switch 1
5	— +5 VDC	6	— Switch 2

J5 — Keyboard Interface
(8-Pin Rt. Angle Circular Din)

1	— KBDDATA	2	— KBDBUSY*
3	— Ground	4	— KBDCLK
5	— +5 VDC	6	— KBDRST
7	— MULTIDATA	8	— MULTICLK

J6 — Floppy Disk Interface
(Dual 17-Pin Vertical Header)

1	— Ground	2	— NC
3	— Ground	4	— NC
5	— Ground	6	— NC
7	— Ground	8	— INDEX*
9	— Ground	10	— DS0*
11	— Ground	12	— DS1
13	— Ground	14	— NC
15	— Ground	16	— MTRON*
17	— Ground	18	— DIR*
19	— Ground	20	— STEP*
21	— Ground	22	— WRDATA*
23	— Ground	24	— WEN*
25	— Ground	26	— TRK0*
27	— Ground	28	— WRPRT*
29	— Ground	30	— RDDATA*
31	— Ground	32	— SIDESELECT*
33	— Ground	34	— DRVRDY*

J7 — DC POWER
(9-PIN VERTICAL HEADER)

1	—	+5 VDC	2	—	+5 VDC
3	—	+5 VDC	4	—	Ground
5	—	Ground	6	—	Ground
7	—	Ground	8	—	-12 VDC
9	—	+12 VDC			

J8,J9,J10 — Expansion Interface Connectors
(Dual 31-Pin Card Edge)

A01	— NMI	B01	— Ground
A02	— D7	B02	— RESET
A03	— D6	B03	— +5 VDC
A04	— D5	B04	— IR2
A05	— D4	B05	— (-5 VDC)
A06	— D3	B06	— FDCDMARQ*
A07	— D2	B07	— -12 VDC
A08	— D1	B08	— AUDIOIN
A09	— D1	B09	— +12 VDC
A10	— READY	B10	— Ground
A11	— AEN	B11	— MEMW*
A12	— A19	B12	— MEMR*
A13	— A18	B13	— IOW*
A14	— A17	B14	— IOR*
A15	— A16	B15	— (DACK3*)
A16	— A15	B16	— (DRQ3*)
A17	— A14	B17	— (DACK1*)
A18	— A13	B18	— (DRQ1*)
A19	— A12	B19	— REFRESH*
A20	— A11	B20	— CLK
A21	— A10	B21	— RFSHRQ
A22	— A09	B22	— BREQ*
A23	— A08	B23	— IR5
A24	— A07	B24	— IR4
A25	— A06	B25	— IR3
A26	— A05	B26	— FDCDACK*
A27	— A04	B27	— DMATC
A28	— A03	B28	— ALE
A29	— A02	B29	— +5 VDC
A30	— A01	B30	— OSC
A31	— A00	B31	— Ground

Note: Signals in parentheses on J8, J9, and J10 are shown for PC Compatible Reference only and are not used on the main logic board of the Tandy 1000.

J11 — Parallel Interface
(34-Pin Card Edge)

1	—	PPSTROBE*	2	—	Ground
3	—	PPDATA0	4	—	Ground
5	—	PPDATA1	6	—	Ground
7	—	PPDATA2	8	—	Ground
9	—	PPDATA3	10	—	Ground
11	—	PPDATA4	12	—	Ground
13	—	PPDATA5	14	—	NC
15	—	PPDATA6	16	—	Ground
17	—	PPDATA7	18	—	Ground
19	—	PPACK*	20	—	Ground
21	—	PPBUSY	22	—	Ground
23	—	PPPAEM	24	—	Ground
25	—	PPBUSY*	26	—	NC
27	—	Ground	28	—	PPFAULT
29	—	NC	30	—	PPINIT*
31	—	Ground	32	—	PPAUTOFEED*
33	—	Ground	34	—	NC

J12 — Light Pen
(9-Pin Connector Male Rt. Angle D-Subminiature)

1	—	+5 VDC	2	—	Ground
3	—	LPIN	4	—	LPSW*
5	—	NC	6	—	NC
7	—	NC	8	—	NC
9	—	NC			

J13 — RGBI Video
(9-Pin Socket Rt. Angle D-Subminiature)

1	—	Ground	2	—	Ground
3	—	Red	4	—	Green
5	—	Blue	6	—	Intensity
7	—	+12 VDC	8	—	HSYNC
9	—	VSYNC			

J14 — Composite Output
(Dual Rt. Angle RCA-Type Phone Jack)

A — Video
B — Audio

1000 and IBM I/O Bus Cross Reference Chart

Pin No.	Signal Name	Description
B18	DRQ1*	IBM - This signal is always available on the IBM PC. TANDY 1000 - DMA request 1 is available only on the I/O bus when the Memory/DMA board is installed.
B17	DACK1*	IBM - This signal is always available on the IBM PC. TANDY 1000 - DMA grant 1 is only available on the I/O bus when the Memory/DMA board is installed.
B16	DRQ3*	IBM - This signal is always available on the IBM PC. TANDY 1000 - DMA request 3 i only available on the I/O bus when the Memory/DMA board is installed.
B15	DACK3*	IBM - This signal is always available on the IBM PC. TANDY 1000 - DMA grant 3 is only available on the I/O bus when the Memory/DMA board is installed.
B05	-5VDC	IBM - -5VDC is always available. TANDY 1000 - -5VDC is not installed on the I/O bus, but a modification is available through an authorized repair center.
B21	RFSHRQ*	IBM - This signal functions as a refresh request on the I/O bus, but is labeled Interrupt Request 7. TANDY 1000 - Same function as on the IBM PC, but different pin designation.
B22	BREQ*	IBM - This signal functions as a bus request on the I/O bus, but is labeled Interrupt Request 6. TANDY 1000 - Same function as on the IBM PC, but different pin designation.
B08	AUDIOIN	IBM - Reserved TANDY 1000 - Audio input is supplied from an optional board on the I/O bus to a multiplexer on the main logic board for an output to the external speaker.

1000 and IBM I/O Bus Cross Reference Chart (Continued)

Pin No.	Signal Name	Description
B06 B26 B27	FDCDMARQ* FDCDACK* DMATC	These signals are functionally the same as those on the IBM PC, however, the Tandy 1000 was designed with an FDC Controller on the main logic board and the DMA Controller on the optional memory board. The IBM PC has the DMA Controller on the main logic board and the optional FDC Controller on the I/O bus.

Note: All other pins are identical to the IBM PC. See Section 3 for the connector pin assignments.

BUS INTERFACE SPECIFICATIONS

This specification is for the primary bus on the Tandy 1000 main logic board, which also is available to the option board connectors. The specification describes the signals in the following manner. See Figures 5 and 5.1.

- The following signal nomenclature is used in the schematic and literature. Signals designated with the suffix "*" are logically "true low" (normal inactive state is high); if they are not so designated, the signal is logically "true high."
- Direction – input or output – is referenced to the CPU.
- Brief functional description of the signal.
- Description of the "drive" or "load" characteristics of the signal. This includes the specific source by IC type and reference designator, drive capability for "output" signals, and actual load for "input" signals. The drive/load is defined in "unit loads" and specified as "high/low." This specification is for the main logic board only. Some signals have an alternate source, an external bus master such as the DMA.
- 1 Unit Load (UL) is defined as: Ioh = .04mA @ 2.4V
  Iol = 1.6mA @ 0.5V

Signal Listing

A00 - A19	O	ADDRESS	SOURCE: U41, U42, U61 Drive - 65/15 UL Latch Strobe - ALE Output Enable - AEN Alternate external source
D0-D7	I/O	DATA	SOURCE: U62 Drive - 37/15 UL Direction Control - RD* (CPU read signal) Enable - DEN*
ALE	O	ADDRESS LATCH STROBE	SOURCE: U46
IOW*	O	I/O WRITE STROBE	Drive - 50/7.5 UL
IOR*	O	I/O READ STROBE	Output Enable - AEN
MEMW*	O	MEMORY WRITE STROBE	Pull-Up - 4.7K ohms
MEMR*	O	MEMORY READ STROBE	Alternate external source
CLK	O	CPU CLOCK	4.77MHz, 33% duty cycle SOURCE: U82 Drive - 75/7.5 UL
OSC	O	OSCILLATOR	14.32MHz, 50% duty cycle SOURCE: U82 Drive - 75/7.5 UL
NMI	I	NON-MASKABLE INTERRUPT	To System NMI Load: 1/1 UL, U117

READY	I	SYSTEM WAIT	SOURCE: OPEN-COLLECTOR OR 3-STATE BUFFERS Load: 1 UL and 1.0K ohm pull-up. 10/0.9 UL Set LOW by Peripherals (I/O or Memory) to extend READ or WRITE cycles.
RESET	O	SYSTEM RESET	Power On or Manual SOURCE: U82 Drive: 75/7.5 UL
BREQ*	I	BUS REQUEST	From external masters Load: 1 UL and 10K ohm pull-up. 10/0.9 UL
AEN	O	BUS GRANT	To external masters SOURCE: U82 Drive - 75/7.5 UL
IR2	I	INTERRUPT REQUEST#2	To system interrupt controller Load: 1 UL and 2.2K pull-down
IR3	I	INTERRUPT REQUEST#3	
IR4	I	INTERRUPT REQUEST#4	
AUDIO IN	I		From External Sound Source Load: 10k ohms.
AUDIO OUT	O		To External Source Drive: 1.25 Volts P-P into 10K

The following are not sourced by the CPU but are to be SOURCED (O) Output or LOADED (I) Input by an external DMA source:

RFSHRQ	I	REQUEST DMA CHANNEL#0	Dedicated input requests to DMA
DRQ1	I	REQUEST DMA CHANNEL#1	Load: 8237A-5/9517A
FDCDMARQ	I	REQUEST DMA CHANNEL#2	1 MOS load 40/160 UL
DRQ3	I	REQUEST DMA CHANNEL#3	
REFRESH*	O	ACKNOWLEDGE DRQ0*	Dedicated output acknowledges from DMA. Drive: 8237A-5/9517A 2/2 UL
DACK1*	O	ACKNOWLEDGE DRQ1*	
FDCDACK*	O	ACKNOWLEDGE DRQ2*	
DACK3*	O	ACKNOWLEDGE DRQ3*	
DMATC	O	TERMINAL COUNT	Used by DMA Controller to indicate Terminal Count reached. Drive: 2/2 UL

+5VDC	+5VDC ± 4% 3.0 Amps available on the bus.
+12VDC	+12VDC ± 5% 0.5 Amps available on the bus.
−12VDC	−12VDC + 8.3% − 25% 0.06 Amps available on the bus.
GROUND	Power Return for +5, +12, −12 VDC.

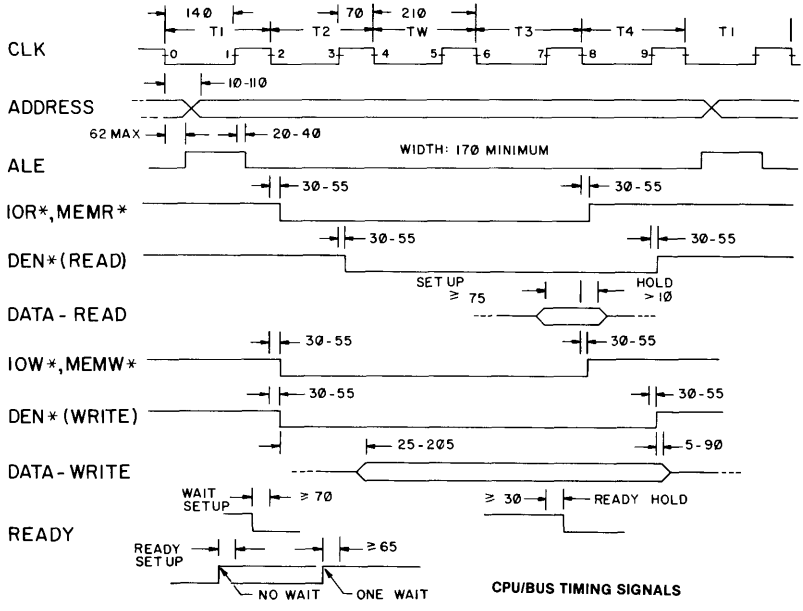


Figure 2
CPU/BUS Timing Signal

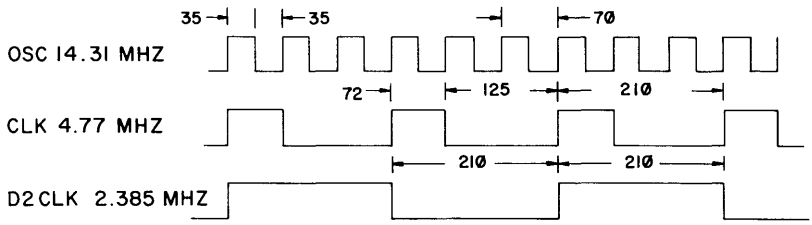


Figure 2.1
CPU/BUS Timing Signal

THEORY OF OPERATION

Main Logic Board

The Block Diagram of the main logic board (Figure 3) shows the basic functional divisions.

CPU Function

The CPU function consists of the CPU (Intel 8088), the address, data interface, the CPU control signal generator, the bus control signal generator and the interrupt controller (Intel 8259A). It is located in the upper right hand corner of the board above the external bus connectors.

Non-CPU Function, Main Logic Board

The non-CPU functions can be divided into two main parts: memory and I/O. Memory consists of RAM and ROM. RAM or Video/System Memory serves as storage for both the video data and program data. ROM memory contains the BIOS and diagnostics. I/O consists of all the peripheral functions; keyboard, floppy disk controller, printer, joystick, light pen and sound.

Processor Address/Data Interface

The 8088 has three groups of Address/Data lines; AD0 - AD7, A8 - A15 and A16 - A19. AD0 - AD7 are multiplexed address and data lines. To separate and save the address that comes out first, the signals are applied to U61 (74LS373) and latched by ALE. Additionally, the signals are applied to data transceiver U62 (74LS245). U62 is enabled only during the data portion of the CPU cycle. (The exception is during an Interrupt Acknowledge cycle.) Direction of transmission is controlled by the RD* (READ) signal from the CPU. Address lines A8 - A15 are present during the entire CPU cycle and need only to be buffered. Address lines A16 - A19 are multiplexed with status signals S4 - S7 and need to be latched. The results are: A8 - A11, A16 - A19 are latched into U41 (74LS373) by ALE and A12 - A15 are buffered by half of U43 (74LS244). The outputs from these latches/buffers/transceivers are the BUS Signals A00 - A19, D0 - D7.

CPU Control Signal Generation

The 8088 CPU uses a 4.77 MHz clock with a special duty cycle (33% high, 67% low.) This clock is produced by the 8284 clock generator/driver U45. The 8284 receives a 14 MHz input clock and divides it by 3 to produce CPUCLK (4.77 MHz) and by 6 to produce D2CLK (2.385 MHz). In addition to being used by the control signal logic the clocks are buffered by U82 (74LS244) for

the bus signals OSC (14 MHz), (4.77 MHz) and main logic signal D2CLK (2.385 MHz). (See the Bus Interface Specification)

The RESET signals (CPURESET, SYSRST*, RST*) originate at U45 (8284) which synchronizes the input RES*. RES* originates from C26 which is shorted to 0 volts by either the manual reset switch or by diode CR6 when the power is off.

The READY circuit synchronizes the system "ready" signals with the CPU clock and generates the CPU input CPUREADY. If a function needs one or more "wait" states added to its access, it must set the READY line low. From the main logic board, READY is set low by the sound IC for 32 extra "wait states" and the video/system memory sets READY low for typically one or two "wait" cycles. The READY circuit of the 8284 (U45) is operated in the non-asynchronous mode; i.e. two sequential edges of clock (a rising edge first) are required to set the CPUREADY signal true. Of the four inputs provided, two are used, RDY2 and AEN2. Inputs to RDY2 must be high and the input to AEN2 must be low to set CPUREADY high. Only one input is applied to AEN2: IOWAIT which is a positive pulse generating one "wait" state for every I/O cycle. The signal READY applied to the RDY2 input comes directly from the BUS and is the wired-or (logical OR) of any/all READY's from the subsystems which need "wait state(s)" inserted. READY is pulled-up by R34.

Oscillator Timing and Dynamic RAM Control

The main system timing starts with the 28.63636 MHz oscillator. This oscillator is a single package which produces a TTL output. From the oscillator, U39 divides the master frequency into 4 multiples. The timing diagram (Figure 4) shows this division. 14.31818 MHz is used to clock the video array chip, and also is used by the Intel 8284 to generate the CPU clock signal.

The first three outputs from the counter (U39) are used to derive 8 time states, (U38) and the last output is used to effectively double the number to 16. These 16 time states are shown at the bottom of Figure 6.1. These time states are then used as J-K inputs for F109 flip-flops, which generate the system timing signals RAS*, CAS* and MUX.

The timing diagram shows RAS* and CAS* as constantly occuring pulses which cycle every 279 ns. Only the RAS* and CAS* pulses for the video cycles are constant. During the CPU cycle, RAS* and CAS* pulse will occur only if the CPU is accessing memory. This function is controlled by U116 and ½ of U94. A CPU request for accesses is first latched by the first half of U116. As soon as the next CPU cycle time starts, the second half of U116 is clocked and the CPU access cycle starts. The CPU cycle lasts until the rising edge of RAS* in the video cycle.

The other signals generated by the system timing are STIS, DYMU, and CPULT. ST15 is a syncronization signal for the Video Array chip, and references time state 0 from U39. DYMUX occurs on the rising edge of MUX in the CPU cycle and latches the video data. The final signal, CPULT occurs only during a CPU access and is used to latch read data for the CPU.

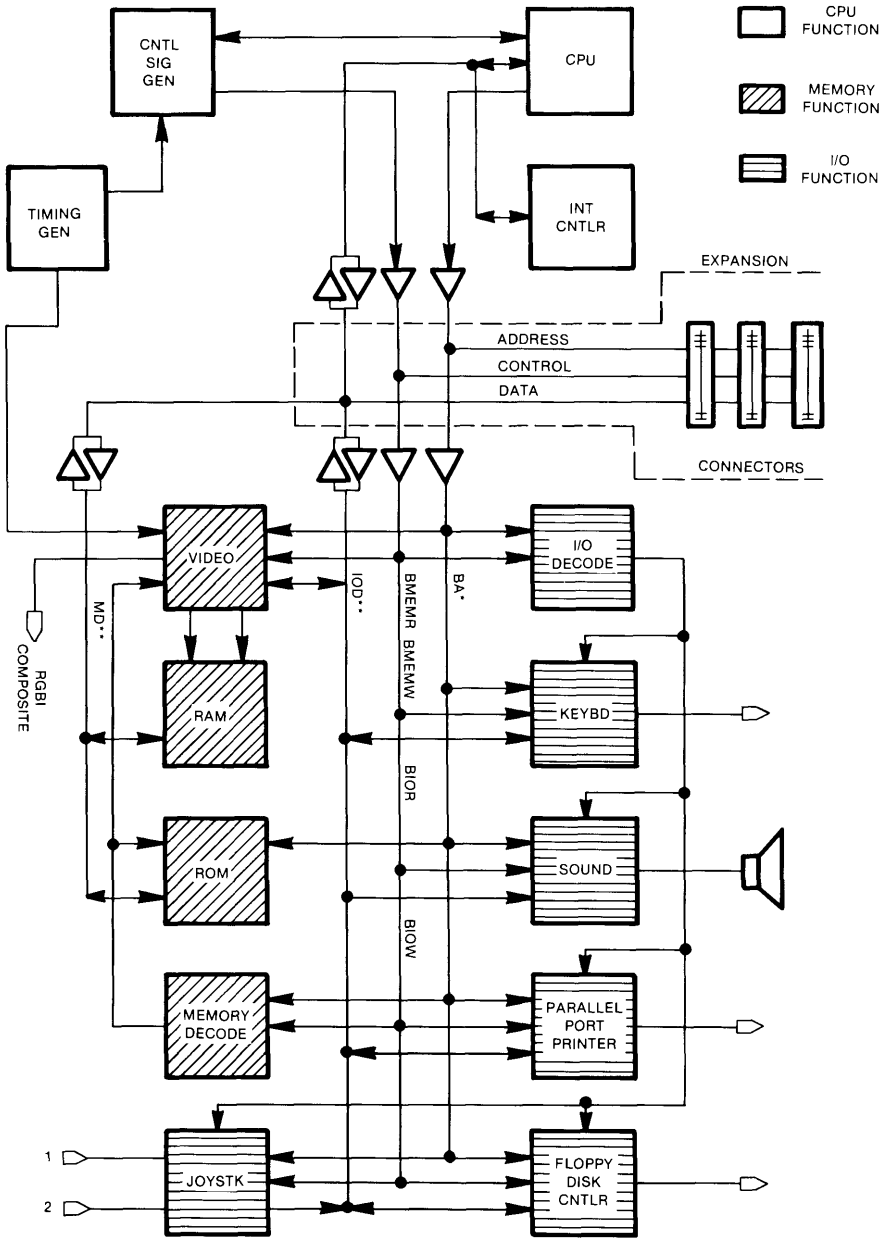


Figure 3
Main Logic Block Diagram

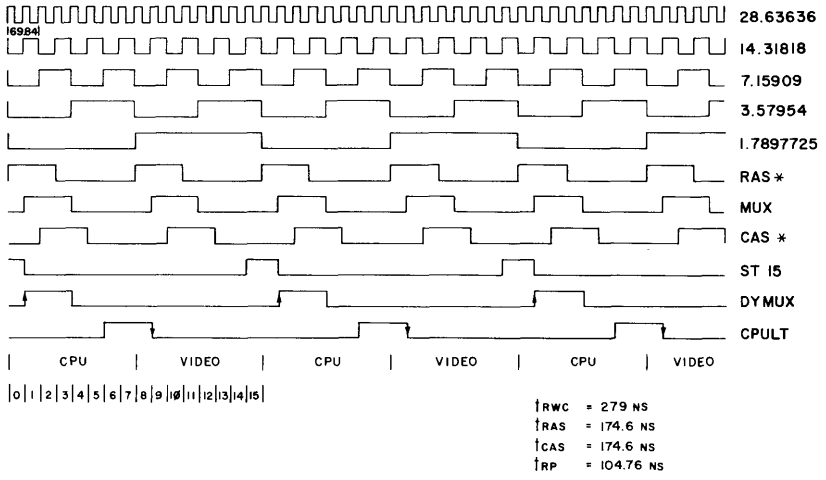


Figure 4
Master Oscillator Timing
(All Times in Nanoseconds)

IFL Equations

U53 Memory Address Decode

Code: 53G **Checksum: 50C9**

Equations:

$$
\begin{aligned}
VSACC^* &= RFSH^* \cdot \overline{MEMR}^* \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{MC3} \cdot \overline{MC2} \cdot \overline{MC1} \\
&+ \quad \overline{19} \cdot \overline{18} \cdot 17 \cdot \overline{MC3} \cdot \overline{MC2} \cdot MC1 \\
&+ \quad \overline{19} \cdot 18 \cdot \overline{17} \cdot \overline{MC3} \cdot MC2 \cdot \overline{MC1} \\
&+ \quad \overline{19} \cdot 18 \cdot 17 \cdot \overline{MC3} \cdot MC2 \cdot MC1 \\
&+ RFSH^* \cdot \overline{MEMR}^* \cdot 19 \cdot \overline{18} \cdot \overline{17} \cdot MC3 \cdot \overline{MC2} \cdot \overline{MC1} \\
&+ \overline{RFSH}^* \cdot \overline{MEMW}^* \cdot \overline{19} \cdot \overline{18} \cdot \overline{17} \cdot \overline{MC3} \cdot \overline{MC2} \cdot \overline{MC1} \\
&+ \quad \overline{19} \cdot \overline{18} \cdot 17 \cdot \overline{MC3} \cdot \overline{MC2} \cdot MC1 \\
&+ \quad \overline{19} \cdot 18 \cdot \overline{17} \cdot \overline{MC3} \cdot MC2 \cdot \overline{MC1} \\
&+ RFSH^* \cdot \overline{MEMW}^* \cdot 19 \cdot \overline{18} \cdot \overline{17} \cdot MC3 \cdot \overline{MC2} \cdot \overline{MC1} \\
&+ HGMEMAC \\
HGMEMAC^* &= RFSH^* \cdot \overline{MEMR}^* \cdot 19 \cdot \overline{18} \cdot 17 \cdot 16 \cdot 15 \\
&+ RFSH^* \cdot \overline{MEMW}^* \cdot 19 \cdot \overline{18} \cdot 17 \cdot 16 \cdot 15 \\
ROMSCO^* &= RFSH^* \cdot \overline{MEMR}^* \cdot 19 \cdot 18 \cdot 17 \cdot 16 \cdot 15 \cdot 14 \cdot 13 \\
ROMSC1^* &= RFSH^* \cdot \overline{MEMR}^* \cdot 19 \cdot 18 \cdot 17 \cdot 16 \cdot 15 \cdot 14 \cdot \overline{13} \\
MEMSEL^* &= VSACC^* \cdot + HGMEMAC^* + ROMCSO^* + ROMCS1^*
\end{aligned}
$$

U80 Main I/O Address Code

Code: 80B **Checksum: 58F9**

Inputs: **Addresses**

	15 · 14 · 13 · 12 · 11 · 10 · 9 · 8 · 7
IO0SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 0 · 0 · 0
IO1SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 0 · 0 · 1
IO4SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 1 · 0 · 0
IO6SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 1 · 1 · 0
IO7SEL*	= 0 · 0 · 0 · 0 · 0 · 0 · 1 · 1 · 1

Outputs:

INTCS* = IO0SEL* · $\overline{6}$ · 5 · $\overline{4}$ · $\overline{3}$

TMRCS* = IO0SEL* · 6 · $\overline{5}$ · $\overline{4}$ · $\overline{3}$

PIOCS* = IO0SEL* · 6 · 5 · $\overline{4}$ · $\overline{3}$

NMICS* = IO1SEL* · $\overline{6}$ · 5 · $\overline{4}$ · $\overline{3}$

SNDCS* = IO1SEL* · 6 · $\overline{5}$ · $\overline{4}$ · $\overline{3}$

JOYSTKCS* = IO4SEL* · $\overline{6}$ · $\overline{5}$ · $\overline{4}$ · $\overline{3}$

PRINTCS* = IO6SEL* · 6 · 5 · 4 · 3

FDCCS* = IO7SEL* · 6 · 5 · 4 · $\overline{3}$

IOSEL* = TMRCS* + PIOCS* + NMICS* + SNDCS
+ PRINTCS* + FDCCS* + IO7SEL* · 6 · 5 · 4

U46 System Timing Synthesizer

Code: 46DC **Checksum: 3E69**

Equations:

ALE = $\overline{HLDA}$ · CALE

DEN* = $\overline{HLDA}$ · IO/M · $\overline{DT/R}$ · C · INTCS* · SS0 (IOR) · (during IOR*)

+ $\overline{HLDA}$ · $\overline{IO/M}$ · $\overline{DT/R}$ · C · INTCS* · (MEMR) · (during IOR*)

+ $\overline{HLDA}$ · B · DT/R · · INTCS* · $\overline{SS0}$ (MEMW) · (during IOR*)

+ $\overline{HLDA}$ · · DT/R · C · INTCS* · $\overline{SS0}$ (MEMW) · (during IOR*)

IOR* = $\overline{HLDA}$ · IO/M · B · $\overline{DT/R}$ · SS0*

MEMR* = $\overline{HLDA}$ · $\overline{IO/M}$ · B · $\overline{DT/R}$ ·

IOW* = $\overline{HLDA}$ · IO/M · B · DT/R · $\overline{SS0}$

MEMW* = $\overline{HLDA}$ · $\overline{IO/M}$ · B · DT/R · $\overline{SS0}$

IOWAIT = $\overline{HLDA}$ · IO/M · A · $\overline{DT/R}$ · SS0

+ $\overline{HLDA}$ · IO/M · A · DTR

U103 Video Address Decode

Code: 103C **Checksum: 44B0**

GACS* = · $\overline{IOW}$ · $\overline{IO7SEL*}$ · 6 · $\overline{5}$ · 4 · 3 · $\overline{2}$ · $\overline{1}$ · $\overline{0}$ · MODE*

+ · $\overline{IOW}$ · $\overline{IO7SEL*}$ · 6 · $\overline{5}$ · 4 · 3 · $\overline{2}$ · $\overline{1}$ · 0

+ · $\overline{IOW}$ · $\overline{IO7SEL*}$ · 6 · $\overline{5}$ · 4 · 3 · $\overline{2}$ · 1 · $\overline{0}$ · STATUS*

+ · $\overline{IOW}$ · $\overline{IO7SEL*}$ · 6 · $\overline{5}$ · 4 · 3 · 2 · 1 · 0

STATUS* = IO7SEL* · 6 · $\overline{5}$ · 4 · 3 · $\overline{2}$ · $\overline{1}$ · 0

MODE* = · IOW · IO7SEL* · 6 · $\overline{5}$ · 4 · 3 · $\overline{2}$ · $\overline{1}$ · $\overline{0}$

LPCLR* = $\overline{IO7SEL*}$ · 6 · $\overline{5}$ · 4 · 3 · $\overline{2}$ · 1 · 0 · $\overline{IOW}$

LPSET* = $\overline{IO7SEL*}$ · 6 · $\overline{5}$ · 4 · 3 · 2 · $\overline{1}$ · $\overline{0}$ · $\overline{IOW}$

PGCLK* = $\overline{IO7SEL*}$ · 6 · $\overline{5}$ · 4 · 3 · 2 · 1 · 0 · $\overline{IOW}$

6845CS* = $\overline{IO7SEL*}$ · 6 · $\overline{5}$ · 4 · $\overline{3}$ ·

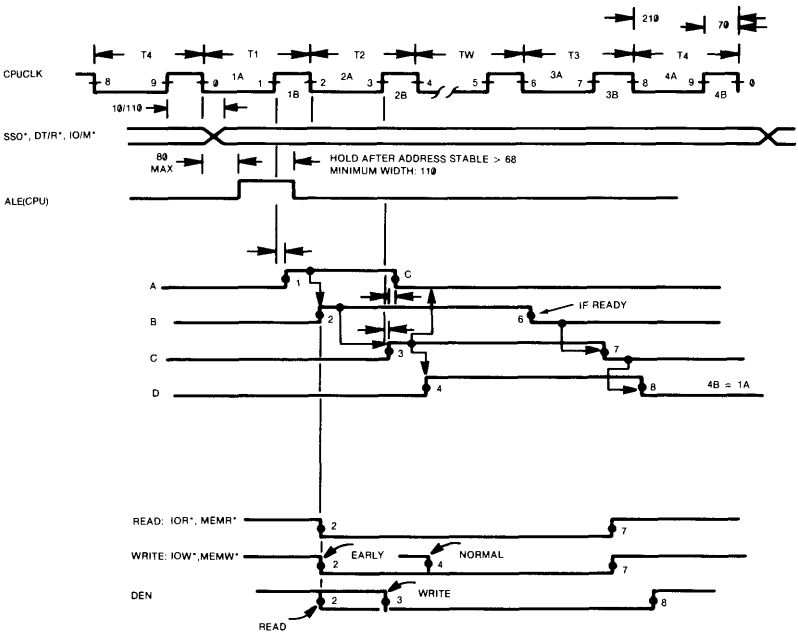
System Control Signal Generation

The System Control Signal Generator provides the timing strobes required by the system. These include IOW*, IOR*, MEMW*, MEMR*, ALE, DEN* and IO/M*. These signals are synthesized by U46 (IFL) from timing signals A,B,C,D, 8088 status signals SSO*, DT/R*, IO/M* plus HLDA and INTCS* (8259 chip select). Timing signals A, B, C, D come from flip-flops U23 and U47. The timing clock is CPUCLOCK. A CPU cycle is divided into five periods: T1, T2, T3, TWAIT, and T4. Each cycle has a clock rising edge and a clock falling edge. Thus T1+ denotes rising, and T1– denotes falling. Signal "A" is started by ALE true (T1+) and stopped by "C", (T2+). Signal "B" is started by "A" and (T1–) and stopped by CPUREADY, and "D". Signal "C" is started by "B", (T2+) and stopped by "BNOT", (T3+). Signal "D" is started by "C", (T2–) and stopped by "CNOT", (T3–). Characteristically, "A" is always one clock long while "B", "C" and "D" are variable in length depending on the number of inserted "wait" states. Thus any half-clock period between T1+ and T3– can be logically combined to create the output timing signals. See Figure 5.

All external devices, except the 8259A Interrupt Controller, are buffered by an LS244 that is controlled by the DEN* signal. Since the 8259A is not buffered, the DEN* signal must remain inactive during accesses to the 8259A.

Bus Specification

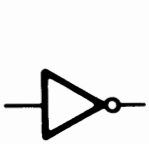
Specifications for the bus will include the expansion connector pin/signal assignments and the signal characteristics. Refer to the Expansion I/F Connector diagram. See Figure 6.



TIMING DIAGRAM

Figure 5
(All Times in Nanoseconds)

EXPANSION I/F CONNECTOR



B		A	
GND	1	1	NMI
RESET			D7
+5VDC			D6
IR2			D5
NC	5	5	D4
FDCDMAR0*			D3
-12VDC			D2
AUDIO IN			D1
+12VDC			D0
GND	10	10	READY
MEMW*			AEN
MEMR*			A19
IOW*			A18
IOR*			A17
DACK3*	15	15	A16
DRQ3*			A15
DACK1*			A14
DRQ1*			A13
REFRESH*			A12
CLK	20	20	A11
RFSHRQ*			A10
BREQ*			A09
NC			A08
IR4			A07
IR3	25	25	A06
FDCDMACK*			A05
TC			A04
ALE			A03
+5VDC			A02
OSC	30	30	A01
GND	31	31	A00

Figure 6

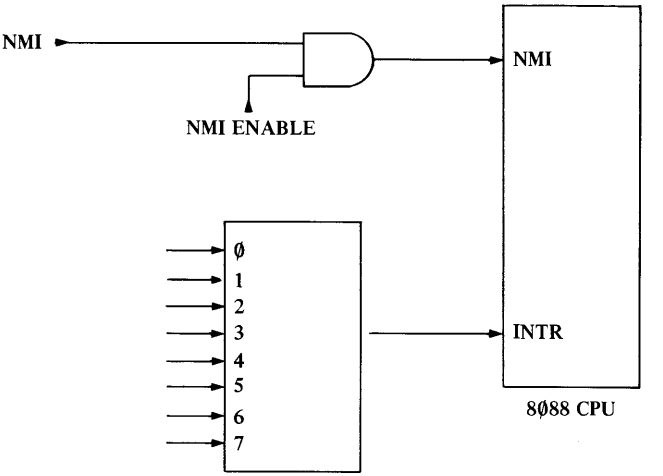
Interrupt Function

The 8088 supports two types of interrupts: maskable (by the CPU, INT) and non-maskable (NMI). See Figure 7. The 8259A Interrupt Controller is the source of the INT for the 8088. The 8259A has eight interrupt inputs controlled through software commands. It can mask (disable) and prioritize (arrange priority) to generate INT. These eight interrupts are:

#0	Timer Channel 0	Software Timer
#1	Keyboard	Keyboard Code Received
#2	Hard Disk Controller	Optional Function, Interrupt on Bus
#3	Modem	Optional Function, Interrupt on Bus
#4	RS-232	Optional Function, Interrupt on Bus
#5	Vertical Sync	Software Timer for Video
#6	Disk Controller, Floppy	Ready to Receive/Transmit Data
#7	Printer	Data Transmission Complete

The NMI interrupt is not maskable by the CPU but it can be enabled/disabled by hardware. The enable is at Port 00A0 Bit 7. The enable is cleared by RESET. There is no specific function assigned to NMI and it is available on the bus.

INTERRUPT STRUCTURE



8259A INTERRUPT CONTROLLER

INTERRUPT	FUNCTION
NMI	AVAILABLE ON BUS
Ø	8253 TIMER CH Ø
1	KEYBOARD
2	HARD DISK
3	SECONDARY COMM.
4	PRIMARY COMM.
5	VERTICAL SYNC.
6	FLOPPY DISK CONTROLLER
7	PARALLEL PORT

Figure 7

Bus Interface

The interface to the main bus is divided into three parts: address/control strobes, memory data and I/O data. The address/control strobe part (BA0 - BA19, BMEMR*, BMEMW*, BIOR*, BIOW*) is shared by both the I/O and the memory sections. Input buffers are U59, U60 and U42. One function of the address bus is the select logic for each of the functions. U80 decodes all the I/O chip selects except those for the Video/System Memory I/O ports which are decoded by U103. The memory selects are decoded by U53. The I/O data transceiver is U97 with its output enable decoded by U80. The memory transceiver is U14 and its output enable is decoded by U53. The direction control for both data transceivers are the "read" strobes; IOR* for U97 and MEMR- FOR U14.

Keyboard / Timer / Sound Circuits

The focal point for this circuit is the 8255 Programmable Peripheral Interface (PPI). It has three 8 bit parallel ports, A, B and C. Port A is configured as an input port and is used for keyboard data. Port B is configured as an output port and is used for control signals for the sound, keyboard and timer functions. Port C is split into 4 inputs, including the timer channel and #2 monitor and 4 outputs including the keyboard/multifunction interface signals. See Figure 8.

Keyboard Data

The computer receives data from the keyboard in an asynchronous serial format with one 8 bit word for each keystroke. This serial data is converted by the shift register, U91. This byte is then read by the CPU through the 8255 Port A. On receipt of a character an interrupt is set and the keyboard "BUSY" signal disables further transfers from the keyboard (½ of U104). To enable the keyboard again, the "keyboard clear" signal from 8255 Port B must be toggled. This signal when high clears the interrupt, the shift register and holds "BUSY" active (U78 pin 11.) Holding "BUSY" active prevents another character from being sent until the clear routine is complete. The serial data from the keyboard consists of a clock signal and a data signal. The clock consists of 8 consecutive positive pulses (signal normal state is logic low). The rising edge of each pulse is centered in the middle of each data period. The data signal consists of 8 data periods and a "end-of-character" bit. Normal state of the data signal is logic high which represents a logic 1. Thus the data signal will change only if the data bit is a 0. The ninth and last data bit is always a 0. In the absence of a ninth clock it will strobe a 1 into U104 and set the interrupt and busy signals. See the Keyboard Timing Chart in the Keyboard Chapter.

PROGRAMMABLE PERIPHERAL I/F 8255A-5 (PPI)

PORT ASSIGNMENTS

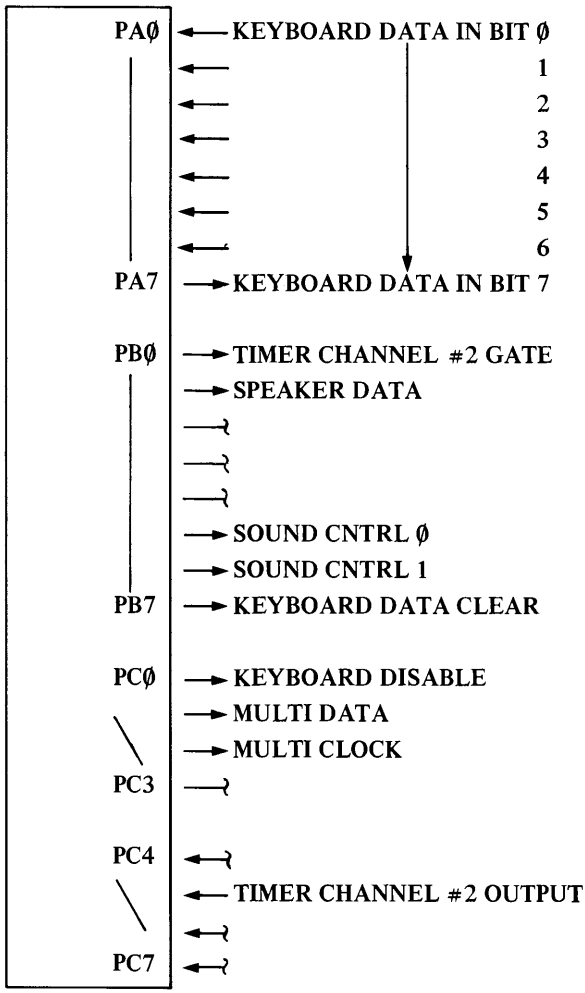


Figure 8

Timer Function

The Timer is an 8253 Timer/Counter consisting of three independent counters. The clock for all three counters is 1.1925 MHz. The gate for counter #0, #1 is permanently "on". The gate for counter #2 is controlled by a bit of the 8255 Port B. The output of counter #0 is dedicated to system interrupt #0 (8259 IR0) for software timing functions. The output of counter #1 is dedicated to the REFRESH function. When the optional DMA/Memory board is installed, DMA channel #0 is used for refreshing the RAM memory. Counter #1 sets RFSHRQ* (DRQ0) every 15 microseconds to initiate a single "dummy" memory read. The output of counter #2 is routed to the sound circuit and into the 8255 Port C for monitoring by the CPU. See Figure 9.

Sound Function

The sound function consists of an internal and an external sound circuit. The internal sound circuit is directly connected to the speaker via U118. The source of the sound frequencies is U96 Complex Sound Generator. Internally, U96 has four programmable sound generators. The frequency and output level of each is controlled by software. The four internal generators are summed with an external input into a single output. The external source is from the 8253 counter #2 (programmable frequency and fixed amplitude). In addition to being the only source for the unit speaker, it is one of three selectable sources for the external audio out signal. This signal is intended as an input into a external amplifier such as a stereo. The three sound frequency sources are:

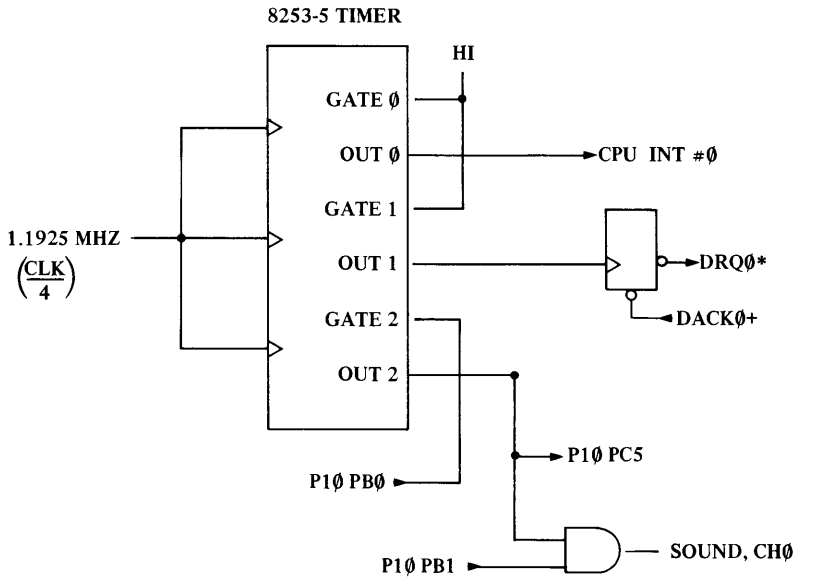
1. Complex sound generator U96.

2. The 8253 counter at channel 2.

3. Any external source applied to bus interface pin B08, Audio In.

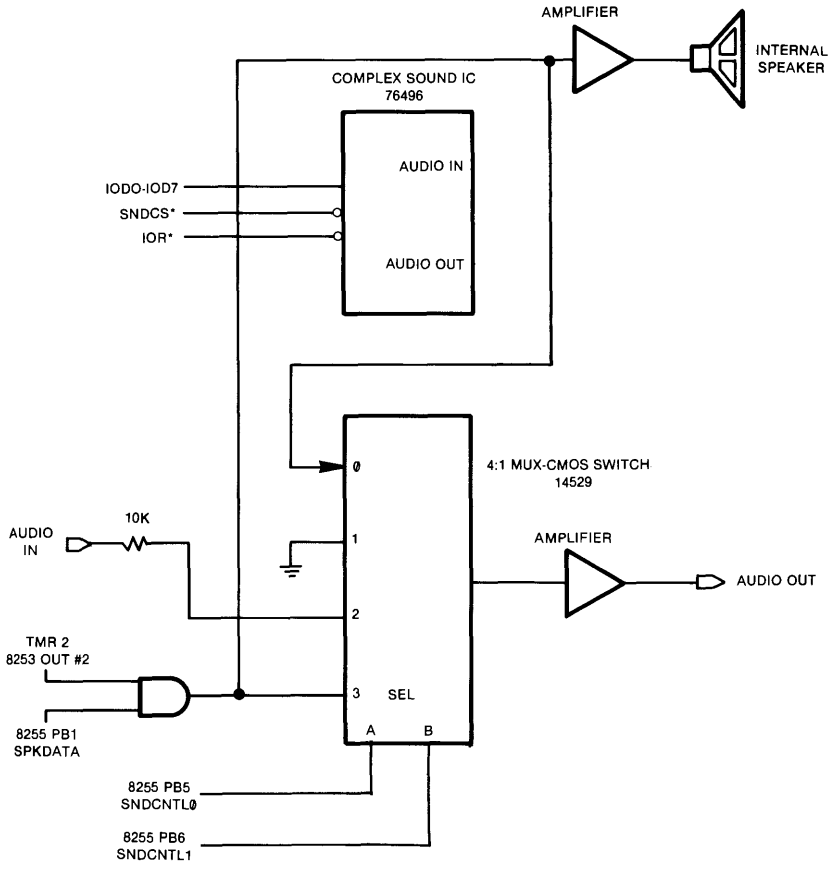
These are selected by an analog multiplexer U105. Selection signals are SNDCNTL0, SNDCNTL1 from the 8255. The output driver for Audio Out is U119 which is designed to drive a load impedance of 1000 ohms. See Figure 10.

SYSTEM TIMER 8253-5



CHANNEL Ø: MODE Ø, INTERRUPT ON T/C
1: MODE Ø, NEGATIVE PULSE ON T/C
2: MODE 3, SQUARE WAVE OUTPUT

Figure 9



SOUND FUNCTIONAL BLOCK DIAGRAM

Figure 10

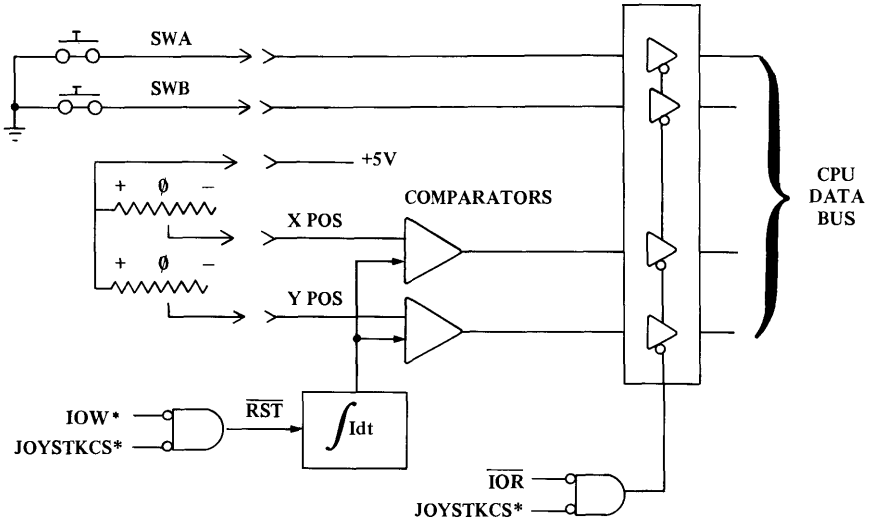
Joystick Interface

The joystick interface converts positional information from hand-held joysticks (1 or 2) into CPU data. Each joystick provides 1 or 2 push-buttons and X, Y position for a total of 4 bits each. You can use 2 joysticks. The joystick handle is connected to two potentiometers mounted perpendicular to each other; one for X position, one for Y position. Through the cable, the main logic board applies +5 VDC to one side and ground to the other of the pots. The pot wiper is the position signal: a voltage between 0 and +5 VDC. This signal is applied to one input of a comparator U119. The other comparator input is the reference signal (a ramp between 0.0 to +5.0 volts.) When the position signal is equal or less than the reference signal, the comparator output goes true. This comparator output is the X or Y position data bit. The ramp is reset to 0.0 VDC whenever a "write" is made at Port 200/201 Hex. The IOW* signal turns on Q2, which drains C6 to 0.0 volts. When Q2 is turned off, Q1, R3, R4, R9, and CR1 create a constant-current source that linearly charges C6 to +5.0 VDC in 1.12 milliseconds. The joystick information is "read" by the CPU at Port 200/201 Hex through U18. See Figure 11.

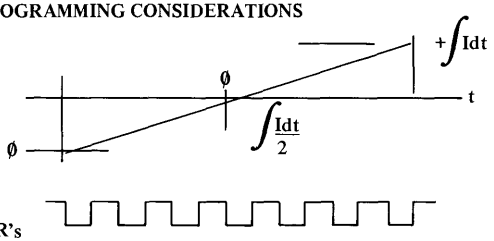
Printer Interface

The printer interface is totally contained in a custom Gate Array U108 and is shown in Figure 12. Functionally, the printer interface consists of an output data latch (write @ 378) and accompanying input data buffer. The latch and buffer reads back the output data (read @ 37A) with an accompanying input buffer for read-back (read @ 37A). The input buffer is for reading printer input signals (read @ 379), I/O address decoding, data transceiver, and interrupt logic. The interrupt is (logically) ACKNOWLEDGE* if interrupts are enabled (37A Bit 4).

JOYSTICK I/F

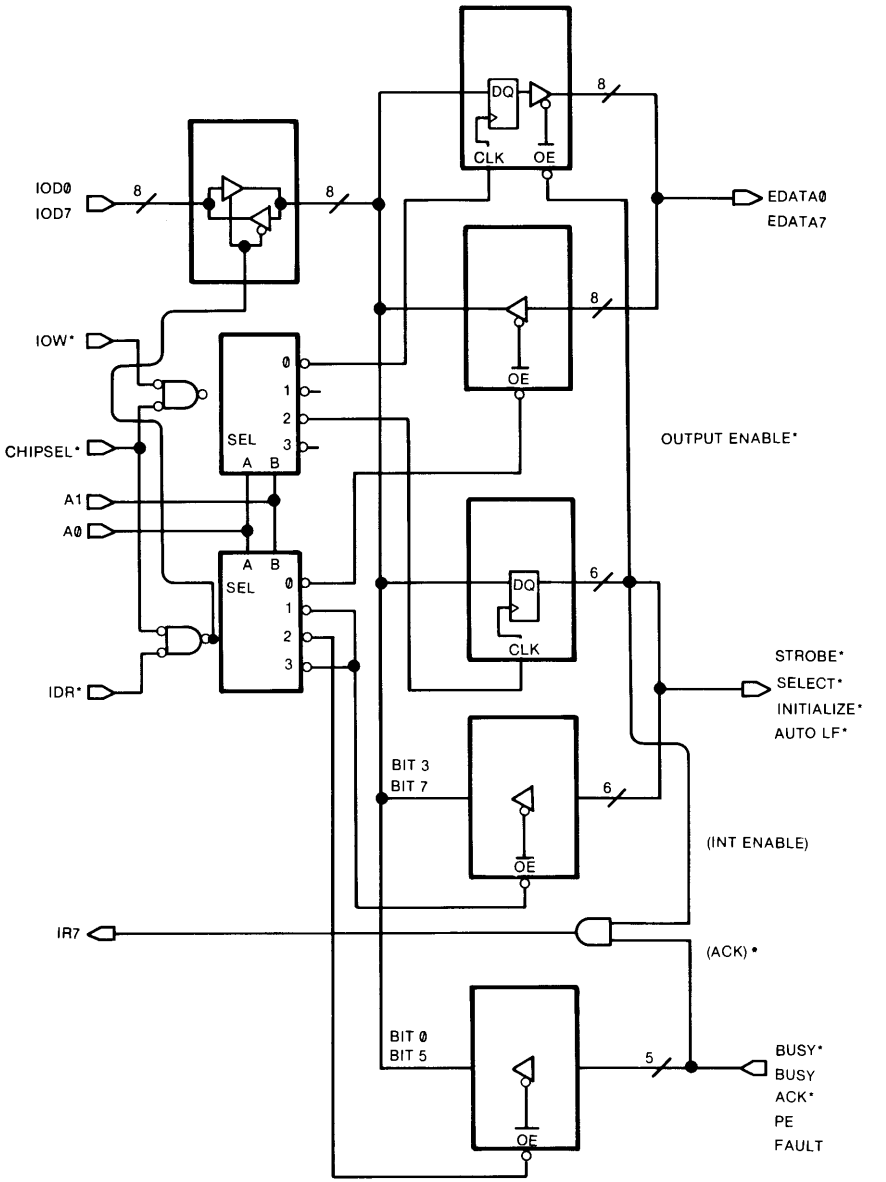


PROGRAMMING CONSIDERATIONS



ONCE TRIGGERED BY SOFTWARE THE INTERGRATOR CIRCUIT PRODUCES A PULSE THE DURATION OF WHICH IS DEPENDENT ON JOYSK POSITION.

Figure 11



PRINTER SCHEMATIC

Figure 12

Floppy Disk Controller Interface

The Floppy Disk Controller interface consists of the 765 controller and support circuitry. The oscillator formed by U29, Y1 generates an 8.00 MHz clock that is divided down to 4.00 MHz and 2.00 MHz by U30. The 4.00 MHz signal is applied to the FDC for its internal processor clock (CLK pin 19) and to counter circuit U31 to generate the FDC write clock (WCK pin 21). U31 produces a pulse at count 15 that loads the next count of 8. Therefore, WCK is a 250 nanosecond pulse every 2.0 microseconds. The CPU interface consists of the chip select decode U98, U51 address A0, A1, function decode FDCCS*, and IOR*, IOW*. The function decode FDCDS* is separated into the lower four address range for the "DOR" register and into the upper four address range for the FDC; both are inhibited by AEN. The "DOR" latch U71 is for configuration control, drive select, reset, interrupt/DMA request enable, drive motor control, and software transfer terminal count. Latch U106 is used to delay the FDC DMA request (DRQ) as specified by the 765 specification. Counter U50 is used to add pre-compensation to the MFM coded write data (250 nanosecond pulse every 2.0 microseconds maximum). The 765 FDC signals "early" and "late" determine the number of 8 MHz clock periods (125 nanoseconds) the write data is delayed thru U69 - normal = 6, early = 4, late = 7. Data separator U69 converts "raw data" from the drive into read data (RDD) and read clock (RDW).

Introduction to the Video System Logic

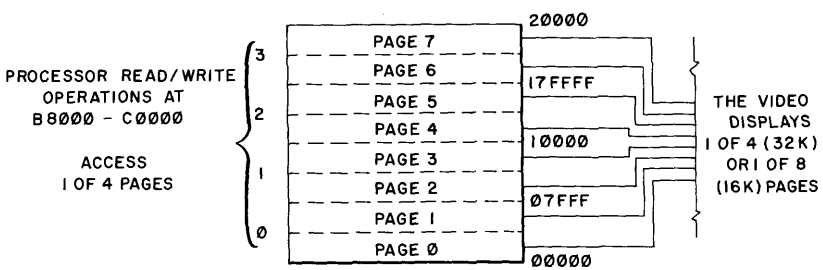
The Video System Logic is composed of three functional sections: Video Address Generation, Video Memory, and Video Data Processing.

The Video Address Generation logic is composed of the MC6845, one control register U99, and six multiplexers. The MC6845 generates the video addresses and video timing signals for all modes of operation. The control register is used for paging the 128K system memory. The MC6845 has a maximum address range of 32K. Since the Video/System RAM size is 128K, the RAM is divided into 4 pages of 32K each. Selection of the page is determined by the Page Register U99, by the Page Multiplexer U89, U90, and by associated gates. The CPU has the option of addressing the RAM at two different locations, one as 32K window starting at B8000 or as System RAM at an assigned 128K page between 00000 and A0000. The top two bits of the control register U99 are used to select different addressing modes for high resolution graphics. For programming ease, any of the graphics modes requiring only 16K of memory will be automatically selected by the addressing logic. Multiplexers U72 through U75 are used to select either the CPU or the video address and to switch between row and column addresses for the dynamic RAM chips.

The Video Memory is composed of two 8 bit rows of 64K dynamic RAMs (64K x 8 x 2) that is shared by the video and the CPU (8088). The video system sees the memory organized as 64K x 16 bits wide to allow a high video bit rate. See the RAM Timing Chart (page 41) for the RAM specifications. The CPU sees the memory as only 8 bits wide. During any read operation (either CPU or video), both banks of memory are accessed at the same time. The data is latched into U35 and U56 for the video or into U36 and U57 for the CPU. The video uses all 16 bits of memory; however, the CPU expects only 8 bits, and the extra bits are ignored. The CPU selects the 64K x 8 bank using address 00000; so the memory is organized as 128K x 8 to the CPU.

The RAM is located at an address determined by the memory configuration control port. In a 128K system that address is normally 00000 — 1FFFF. In addition this memory may be accessed at the 32K byte address from B8000 — BFFFF. A page register selects which of the 4 pages are available to the CPU. The CPU access is synchronized to the video so that no adverse effects are observed at any time.

The processor can address any location in memory while the video is using only a 16K or 32K page. This allows one video page to be displayed while another is being changed by the CPU. Therefore, the displayed page can be switched during vertical retrace. A video system memory map is shown on the next page.



VIDEO SYSTEM MEMORY MAP

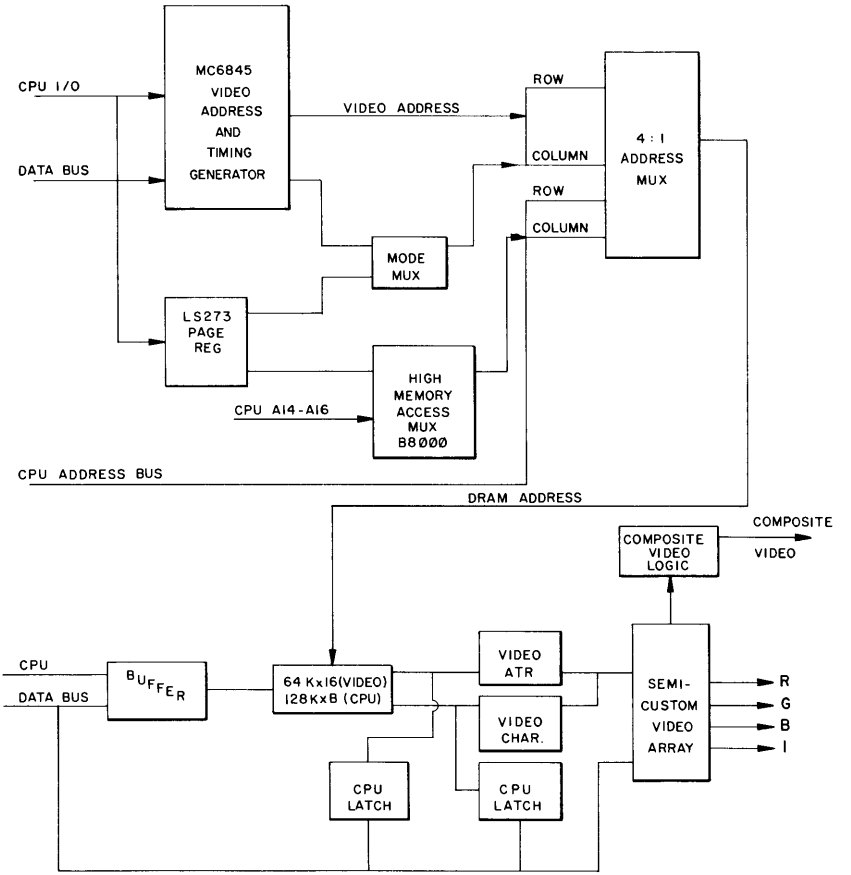
The third section of the video (Video Data Processing) is composed of only one 40-pin IC. However, a large amount of logic has been compressed into that single HCMOS custom IC. Figure 13 shows a block diagram of the logic. The multiplexed data input from the RAM is divided back into 16 bits of information. For the alphanumeric mode this is character byte and attribute byte data. In alphanumeric mode, the character data is used to address the character ROM. The character ROM output is loaded into a shift register controls the on/off selection of each video dot. The attribute byte defines foreground and background color. In graphics mode, the data bits are first rearranged depending on the mode, and then loaded into the shift register. The mode selection multiplexer selects alpha, 2 color, 4 color medium resolution, 4 color high resolution, or 16 color modes. The output of the mode selection multiplexer clocks the RGBI data before it goes to the palette RAM and then clocks it again after the palette. From this last register, the RGBI data passes through the border color mux and then through the output buffers as RGBI data. The RGB outputs are also used to generate the composite color signal.

The remaining logic of the Video Array consists of the timing logic, the control register logic and the timing delay logic. The timing logic provides the clocks and shift load signals for the latches and the shift registers. The control registers are loaded by the system software and provide the mode selection and color control bits. The timing delay logic synchronizes all the logic. See Figure 14 for the Video Array Block Diagram.

Main System Board Ram Timing Specification

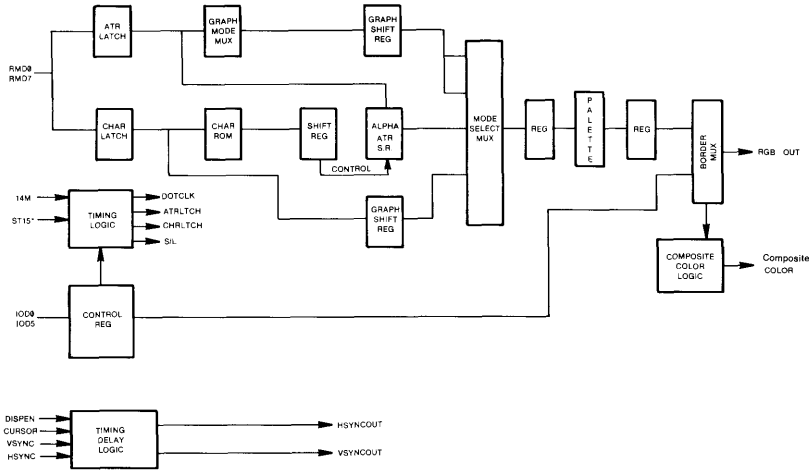
AC Operating Conditions and Characteristics

Parameter	Symbol	Min.	Max.	Units
Random Read or Write Cycle Time	tRC	279	—	ns
Read Write Cycle Time	tRWC	279	—	ns
Access Time from Row Address Strobe	tRAC	—	200	ns
Access Time from Column Address	tCAC	—	100	ns
Output Buffer and Turn-Off Delay	tOFF	0	30	ns
Row Address Strobe Precharge Time	tRP	100	—	ns
Row Address Strobe Pulse Width	tRAS1	170	—	ns
Column Address Strobe Pulse Width	tCAS	130	—	ns
Row Address Setup Time	tASR	0	—	ns
Row Address Hold Time	tRAH	20	—	ns
Column Address Setup Time	tASC	0	—	ns
Column Address Hold Time	tCAH	35	—	ns
Transition Time (Rise and Fall)	tT	—	50	ns
Read Command Setup Time	tRCS	0	—	ns
Read Command Hold Time	tRCH	0	—	ns
Read Command Hold Time Referenced to RAS	tRRH	0	—	ns
Write Command Hold Time	tWCH	35	—	ns
Write Command Hold Time Referenced to RAS	tWCR	95	—	ns
Write Command Pulse Width	tWP	35	—	ns
Write Command to Row Strobe Lead Time	tRWL	45	—	ns
Write Command to Column Strobe Lead Time	tCWL	45	—	ns
Data in Setup Time	tDS	0		ns
Data in Hold Time	tDH	35	—	ns
Data in Hold Time Referenced to RAS	tDHR	95	—	ns
Column to Row Strobe Precharge Time	tCRP	0	—	ns
RAS Hold Time	tRSH	85	—	ns
Refresh Period	tRFSH	—	2.0	ns
WRITE Command Setup Time	tWCS	0	—	ns
CAS to WRITE Delay	tCWD	45	—	ns
RAS to WRITE Delay	tRWD	120	—	ns
CAS Hold Time	tCSH	200	—	ns



VIDEO SYSTEM BLOCK DIAGRAM

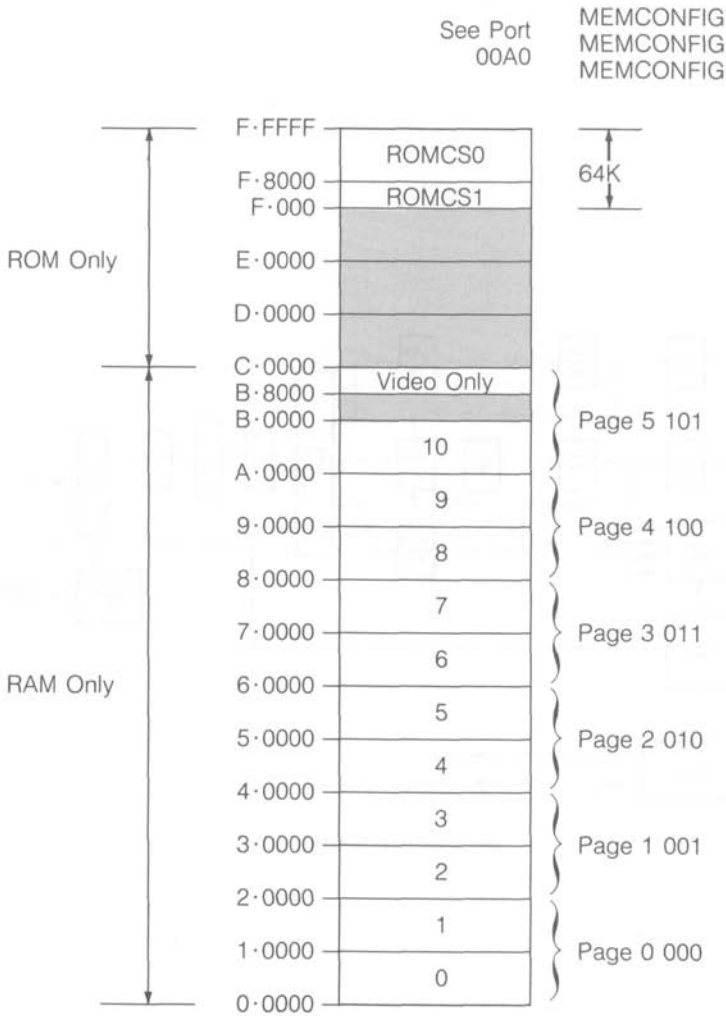
Figure 13



VIDEO ARRAY BLOCK DIAGRAM

Figure 14

Memory Map


See Port 00A0
MEMCONFIG, 3
MEMCONFIG, 2
MEMCONFIG, 1
F·FFFF
F·8000
F·000
E·0000
D·0000
C·0000
B·8000
B·0000
A·0000
9·0000
8·0000
7·0000
6·0000
5·0000
4·0000
3·0000
2·0000
1·0000
0·0000
ROMCS0
ROMCS1
64K
ROM Only
Video Only
10
9
8
7
6
5
4
3
2
1
0
Page 5 101
Page 4 100
Page 3 011
Page 2 010
Page 1 001
Page 0 000
RAM Only

Video System Modes

Display Modes

The video circuitry is designed to operate with three types of display devices: a standard TV using an optional RF modulator, a composite monitor and an RGBI color monitor. To support these different display types, both a composite video output and a 9-pin RGBI connector are provided.

The video display system is very flexible and can be programmed for a number of video modes. These modes use varying numbers of colors (2, 4, or 16). These 16 colors are defined by combinations of the RGBI as shown in the color chart below and can be used for foreground, background, and character blinking. If you are using a black and white monitor. (These colors will appear as shades of gray for use as reverse video, highlighting, and blinking.) In addition any 1 of the 16 colors or shades of gray can be used for the screen border.

Color	I	R	G	B
Black	0	0	0	0
Blue	0	0	0	1
Green	0	0	1	0
Cyan	0	0	1	1
Red	0	1	0	0
Magenta	0	1	0	1
Brown	0	1	1	0
Light Gray	0	1	1	1
Dark Gray	1	0	0	0
Light Blue	1	0	0	1
Light Green	1	0	1	0
Light Cyan	1	0	1	1
Pink	1	1	0	0
Light Magenta	1	1	0	1
Yellow	1	1	1	0
White	1	1	1	1

Available Colors Table

Operating Modes

The operating modes supported by the system software may be grouped into two categories: alphanumeric and graphic.

The alphanumeric mode has two basic types of operation: 80 character by 25 rows and 40 character by 25 rows. In both modes the characters are generated by a 256 character ROM. The character ROM is divided into the following groups:

96 Standard ASCII characters
48 Block Graphics characters
64 Foreign Language/Greek characters
16 Special Graphics characters
32 Word Processing/Scientific-Notation characters

In both modes all characters are 7 dots wide by 7 dots high and are placed in an 8 dot wide by 8 or 9 dot high matrix.

In both the 40 x 25 mode and the 80 x 25 mode, two bytes of data are used to define each character on the screen. The even address (0,2,4 etc.) is the character code and is used in addressing the character generator ROM. The odd address (1,3,5 etc.) is the attribute byte, that defines the foreground and background color of the character. The following chart shows how the attribute byte functions to control colors.

ATTRIBUTE BYTE								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
3D9 Bit 5 = 0	Background				Foreground			
	I	R	G	B	I	R	G	B
3D9 Bit 5 = 1	Blink	R	G	B	I	R	G	B
Blink = A 1 in bit 7 enables blinking of the foreground.								

Graphics Mode

The Video Color/Graphics System can be programmed for a wide variety of modes. The Tandy 1000 and its system ROM BIOS supports the following Graphics Modes:

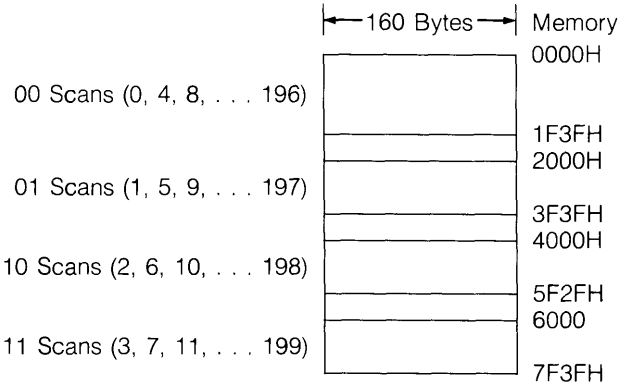
Mode	IMB PCjr	IBM PC
4-Color Medium-Resolution	x	x
16-Color Medium-Resolution	x	
16-Color Low-Resolution	x	
2-Color High-Resolution	x	x
4-Color High Resolution	x	

Low and medium resolution modes work on all types of display devices. The high-resolution mode may require a monitor for correct operation.

Graphics Memory Usage

Graphics memory uses either two or four banks of 8000 bytes. In either case pixel information for the display's upper-left corner is found at address 0000. The 4-color high-resolution and 16-color medium-resolution graphics use four banks of 8000 bytes.

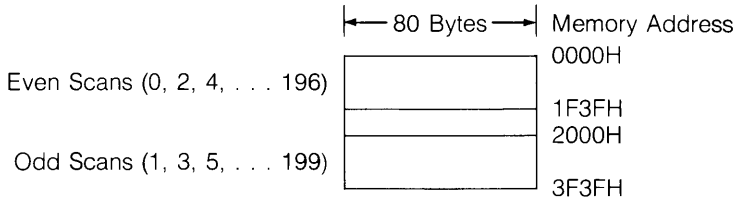
The following is a table of the graphics storage organization for four banks of 8000 bytes:



Graphics Storage Organization

The 2-color high-resolution graphics, the 4-color medium-resolution graphics, and the 16-color low-resolution graphics use only two banks of 8000 bytes.

The following is a table of the graphics storage organization for two banks of 8000 bytes:



Graphics Storage Organization

High-resolution 2-Color Graphics

The high-resolution 2-color mode may require a high-resolution monitor for correct operation. This mode can display 2 of 16 possible colors. It contains 200 rows of 640 pixels, requires 16K bytes of read/write memory, and formats 8 pixels per byte. This mode is available in the IBM PC and IBM PCjr.

Byte 0 = eighth pixel
Byte 1 = seventh pixel
Byte 2 = sixth pixel
Byte 3 = fifth pixel
Byte 4 = fourth pixel
Byte 5 = third pixel
Byte 6 = second pixel
Byte 7 = first pixel

High-Resolution 4-Color Graphics

The high-resolution 4-color mode may require a high-resolution monitor for correct operation. This mode can display 4 out of 16 colors. (Each pixel selects 1 of 4 colors.) It contains 200 rows of 640 pixels, requires 32K bytes of read/write memory and formats 8 pixels per two bytes (1 even-byte and 1 odd-byte). This mode is only supported on the IBM PCjr.

	Even Bytes	**Odd Bytes**
First Display Pixel	PA0 (7)	PA1 (7)
Second Display Pixel	PA0 (6)	PA1 (6)
Third Display Pixel	PA0 (5)	PA1 (5)
Fourth Display Pixel	PA0 (4)	PA1 (4)
Fifth Display Pixel	PA0 (4)	PA1 (3)
Sixth Display Pixel	PA0 (3)	PA1 (2)
Seventh Display Pixel	PA0 (1)	PA1 (2)
Eighth Display Pixel	PA0 (0)	PA1 (0)

Medium-Resolution 16-Color Graphics

The medium-resolution 16-color graphics mode works with all types of display devices. This mode specifies 1 of 16 colors for each pixel. It requires 32K bytes of read/write memory, contains 320 rows of 200 pixels, and formats each byte in the same manner as the low-resolution mode. This mode is available in the IBM PCjr only.

Second Pixel				First Pixel			
0	1	2	3	4	5	6	7
PA0	PA–	PA2	PA3	PA0	PA1	PA2	PA3

Low-Resolution 16-Color Graphics

The low-resolution mode works with all types of display devices. This mode contains 200 rows of 160 pixels, requires 16K bytes of read/write memory, specifies 16 colors for each pixel by the RGBI bits, and formats 2 pixels per byte. This mode is available in the IBM PCjr only.

Second Pixel				First Pixel			
0	1	2	3	4	5	6	7
PA0	PA1	PA2	PA3	PA0	PA1	PA2	PA3

Medium-Resolution 4-Color Graphics

The medium-resolution mode works with all types of display devices. This mode supports 4 of 16 possible colors. It requires 16K bytes of read/write memory, contains 320 rows of 200 pixels, selects 1 of 4 colors for each pixel, and formats 4 pixels per byte. This mode is available in the IBM PC and IBM PCjr.

Fourth Pixel		Third Pixel		Second Pixel		First Pixel	
0	1	2	3	4	5	6	7
PA0	PA1	PA0	PA1	PA0	PA1	PA0	PA1

System Logic Registers

Video Array Registers

The Video Array is addressed at I/O addresses 3D8, 3D9, 3DA, and 3DE. Address 3D8 and 3D9 are PC compatible control registers. Address 3DA is an address register for port selection inside the Video Array. Address 3DE is the data port. You can program all Video Array registers, except 3D8 and 3D9. Registers are programmed by first writing an address to 3DA and the data to 3DE. The following chart shows the address at each of these Video Array registers.

Register	Address Hex
Palette Mask	01
Border Color	02
Mode Control	03
Palette Registers	10 — 1F

Palette Mask Register

This 4-bit (write-only) register has a video array address of 01H. The following table lists each bit.

Bit	Palette Mask
0	0
1	1
2	2
3	3

This register allows any of the address lines into the palette where they are then forced to 0.

Border Color Register

This 4-bit (write-only) register can be addressed in the video array at 02H. The following table gives the register's bit functions.

Bit	Description
0	B (Blue) Border Color Select
1	G (Green) Border Color Select
2	R (Red) Border Color Select
3	I (Intensity) Border Color Select

Border Color Register

The screen-border color is defined by bits 0-3, that selects one of 16 colors. See the Colors Definition Table listed in this section.

Mode Control Register

This 5-bit (write-only) register is accessed at the video array address 03H. The following table gives the register's bit functions.

Bit	Description
0	Not used
1	Not used
2	Border Enable
3	4 Color High Res.
4	16 Color Mode

Mode Control Register

Bit 0 Not Used

Bit 1 Not Used

Bit 2 This bit enables the border color register. For PC compatibility this bit should be 0. For PCjr compatibility this bit should be 1.

Bit 3 For the 4 color 640 x 200 graphics mode, this bit should be set to 1 and for all other modes set to 0.

Bit 4 Set this bit to 1 for 16 color modes and to 0 for all other modes.

Palette Registers

The palette is a 16 x 4 high speed RAM that lets you redefine any color. To load the palette, write the hex address to the video array address register at 3DA. (The 16 palette registers are located at addresses 10 -1F.) Then the new palette color is written to 3DE. Only the 4 least significant bits are used as shown by the following table:

Bit	Description
0	Blue
1	Green
2	Red
3	Intensity

Palette Register Format

Bit 4 of the video array address register is used to select the palette. Once the palette is selected, hashing or noise will be observed on the display. To avoid this effect, the palette should be accessed during vertical or horizontal blanking, and the address register should be changed to less than 10 prior to returning to normal operation.

During the normal display operation, the RGBI information is used to address the palette as shown in the chart below. If a graphics mode (which uses fewer than 16 colors) is selected, the palette is addressed by the extra bits defined by the control registers at 3D8 and 3D9. Optionally, the extra bits may be masked off (PA3 and PA2 are set to 0 or PA3, PA2 and PA1 are set to 0) by using the palette mask register. When you use the mask register, only palette registers 0 and 1 will be used for 2 color modes. Only registers 0,1,2 and 3 will be used for 4 color modes.

Palette Address Bits	Palette Register															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PA0 (B)	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1
PA1 (G)	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
PA1 (R)	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
PA3 (I)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Video Memory Map and Registers

Video Memory Map

Address	Description
3D0	Not used
3D1	Not used
3D2	Not used
3D3	Not used
3D4	6845 Address Register
3D5	6845 Data Register
3D6	Not used
3D7	Not used
3D8	Mode Select Register
3D9	Color Select Register
3DA	Video Array Address & Status
3DB	Clear Light Pen Latch
3DC	Set Light Pen Latch
3DD	Not used
3DE	Gate Array Data
3DF	CRT Processor Page Register

Operation of the video subsystem and mode selection is controlled by the registers listed in the above table. The video array registers at 3DA were explained earlier. The remaining control registers operate as follows:

6845 Address Register (3D4)

This 5-bit write-only register addresses 1 of the 18 internal data registers of the 6845 CRT controller. The selected register is then read or written through the 6845 data register.

6845 Data Register (3D5)

This port is used to access the internal data register previously selected through the 6845 address register.

PROGRAMMING TABLE FOR THE 6845 All Values in Hex (Decimal)

	Register Address	40 x 25 Alpha	80 x 25 Alpha	Low Res. Graphics	High Res. Graphics	40 x 25 Alpha	80 x 25 Alpha	Low Res. Graphics	High Res. Graphics
00	Horizontal Total	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)
01	Horizontal Displayed	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)
02	Horizontal Sync Position	2D (45)	5A (90)	2D (45)	5A (90)	2C (44)	58 (88)	2C (44)	58 (88)
03	Horizontal Sync Width	0A (10)	0A (10)	0A (10)	0A (10)	08 (8)	10 (16)	08 (8)	10 (16)
04	Vertical Total	1C (28)	1C (28)	7F (127)	3F (63)	1F (31)	1F (31)	7F (127)	3F (63)
05	Vertical Total Adjust	01 (1)	01 (1)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
06	Vertical Displayed	19 (25)	19 (25)	64 (100)	32 (50)	19 (25)	19 (25)	64 (100)	32 (50)
07	Vertical Sync Position	1A (26)	1A (26)	70 (112)	38 (56)	1C (28)	1C (28)	70 (112)	38 (56)
08	Interlace Mode	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)
09	Max Scan Line Address	08 (8)	08 (8)	01 (1)	03 (3)	07 (7)	07 (7)	01 (1)	03 (3)
10	Cursor Start	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
11	Cursor End	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)
12	Start Address (High)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)
13	Start Address (Low)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)
		Monitor Mode				**TV Mode**			

Mode Register (3D8)

This mode register controls the basic operating characteristics of the video. It consists of a 6-bit write-only register, and each bit controls one aspect of the operation of the video subsystem.

Bit	Description
0	High Resolution Dot Clock. This bit controls the operating speed of the video system. A "0" selects the lower speed for 40 character text or low resolution graphics modes. A "1" selects high speed for 80 character text or high resolution graphics modes.
1	Graphics Select. This bit selects alpha or graphics modes. A "0" selects the alpha mode. A "1" selects the graphics mode.
2	Black and White Select. This bit selects black and white or color mode for TV or composite monitors. A "1" will disable the color signal and give a black and white image. In RGB monitors, a different color palette is selected by this bit in 320 x 200 4 color graphics mode. This bit will have no other effect on RGB operation.
3	Video Enable. This bit enables or disables the video display. A "1" enables the video display.
4	640 Dot Graphics. This bit is used to select either of the two 640 x 200 graphics modes. A "1" selects 640 x 200.
5	Blink Enable. This control bit is used in the alpha mode only. A "1" selects blinking if the attribute bit is set (bit 7). A "0" selects 16 background colors. (With blinking selected only 8 background colors are available.)

Color Select Register (3D9)

This register is used to control several color features in the alpha modes and the 320 x 200 4 color mode.

Bit	Description
0-3	Alpha Border. In either alpha mode, these bits are used to select the screen color. In the 320 x 200 4 color mode, these bits determine the background color if PA0 and PA1 are both 0. In the 640 x 200 2 color mode, they select the foreground color.
0	Blue
1	Green
2	Red
3	Intensity
4	Alpha Background/320 Graphics Foreground Intensity. When blink is enabled in the alpha mode, this bit is used to select the intensity. In the 320 x 200 4 color mode, the bit selects the intensity of the foreground.
5	320 x 200 4 Color Blue Control. This bit is used to control the blue output in 320 x 200 color graphics.

Status Register

The 4-bit "read only" register provides video and light pen status. It is addressed by a read operation at 3DA. (The video array address register is not used to select this port.) The following table gives the register's bit functions:

Bit	Status
0	Display Inactive
1	Light Pen Trigger Set
2	Light Pen Switch Made*
3	Vertical Retrace

Status Register

Bit 0 When bit 0 is (0), the display is active. When (1), this indicates video is not displayed.

Bit 1 When bit 1 is "high," this indicates that the light pen input has a positive-going edge, and has set the light pen trigger. When this trigger is "low," during a system power-on, it may be cleared by performing an I/O command to address 3DB. No specific data is required due to address-activated action.

Bit 2 Bit 2 is the status of the light pen switch. When bit 2 is "low," the light pen switch is on. The switch is not latched or debounced.

Bit 3 When bit 3 is "high," this indicates that the vertical retrace is active.

Light Pen Latch

Set 3DC

Reset 3DB

Any output to the port sets or resets the light pen latch (data byte has no effect). Before the 6845 can read the light pen again, the latch (3DB) must be cleared.

CRT/Processor Page Register

This 8-bit (write-only) register is addressed at 3DF. The descriptions below are of the register functions:

Bit	Description
0	CRT Page 0
1	CRT Page 1
2	CRT Page 2
3	Processor Page 0
4	Processor Page 1
5	Processor Page 2
6	Video Address Mode 0
7	Video Address Mode 1

CRT / Processor Page Register

CRT Page 0-2

Bits 0-2 select the 16K page used by the video. In 32K modes, bit 0 is ignored.

Processor Page 0-2

These processor page bits are combined with the CPU address to select the 32K segment of memory accessed at B8000. If an odd page number is selected (1,3,5, etc.) the window is reduced to 16K.

Video Address Mode 0-1

These bits are used in conjunction with the graphics control bit (bit 1 at 3D8) to select the video address supplied to the RAM. The following chart lists the values to be used for each video mode.

	Video Address Mode	
Mode Description	1 (Bit 7)	0 (Bit 6)
All Alpha Modes	0	0
Low-Resolution-Graphics Modes	0	1
High-Resolution-Graphics Modes	1	1
Unused, Reserved	1	0

CRT / Processor Page Register

General Memory Information

Mode Selection Summary

	40x25 Alpha B/W	40x25 Alpha Color	80x25 Alpha Color	160x200 16 Color Graphics	320x200 4 Color Graphics	320x200 4 Shades Of B/W	320x200 16 Color Graphics	640x200 2 Color Graphics	640x200 4 Color Graphics
3D8 Bit 0 HRESCK	0	0	1	0	0	0	1	0	1
3D8 Bit 1 GRPH	0	0	0	1	1	1	1	1	1
3K8 Bit 2 BW	1	0	0	0	0	1	0	0	0
3D8 Bit 4 HRESAD	0	0	1	0	0	0	0	1	1
3DA REG 03 Bit 3 4 Color	0	0	0	0	0	0	0	0	1
3DA Reg 03 Bit 4 16 Color	0	0	0	1	0	0	1	0	0

I/0 Map

Address Block	Usage	Function
0000 — 001F	0000 — 000F	DMA Function
0020 — 003F	0020 — 0021	Interrupt Controller
0040 — 005F	0040 — 0043	Timer
0060 — 007F	0060 — 0063	PIO
0080 — 009F	0080 — 0083	DMA Page Register
00A0 — 00BF	00A0	NMI Mask Register
00C0 — 00DF	00C0 — 00C1	Sound Generator
00E0 — 01FF		Reserved
0200 — 020F	0200 — 0201	Joystick I/F
0210 — 031F		Reserved
0320 — 032F		Reserved Hard Disk
0330 — 036F		Not Assigned
0370 — 037F	0378 — 037B	Printer
0380 — 03CE		Not used
03D0 — 03DF	All	System Video
03E0 — 03EF		Reserved
03F0 — 03FF	03F2, F4, F5	Floppy Disk Controller
0400 — FFFF		Not Usable

System Configuration Port I/O Address: 00A0

Data Bit	Function	
D1	MEMCONFIG 1	Selects 1 Of 8 — 128K Memory Pages Where Video/System Ram Memory To Be Located. See Memory Map For Details. Register Located Main Logic.
D2	MEMCONFIG 2	
D3	MEMCONFIG 3	
D4		Reserved
D5		Reserved
D6		Reserved
D7	NMIEN	Enables NMI Input To CPU 0 = Mask 1 = Enable Register Located Main Logic.

ROM

System ROM

Size: 16K x 8 (128K)
32K x 8 (256K) optional

Quantity: 1 or 2, socketed

Address Range — ROM: F0000 To FFFFF

Two 32K address segments are decoded in hardware. There will always be one system ROM located at the boot segment F8000 — FFFFF. The second system ROM will be limited to the second address segment F0000 — F7FFF.

No error detection capability.

RAM

RAM address range: 00000 to B8000

RAM memory used by the CPU must be continuous beginning at 00000.

Address selection granularity — 64K.

Video memory access at B8000/C0000.

Presence (quantity) of RAM in addition to video/system RAM determined by initialization routing.

Video system RAM memory address select defined by "MEMCONFIG" register at 00A0. On power-up or reset, address defaults to B8000.

No memory error detection capability.

Detailed Memory Map

Address[1]	Description
0000	8237A-5 DMA Controller
0001	8237A-5 DMA Controller
0002	8237A-5 DMA Controller
0003	8237A-5 DMA Controller
0004	8237A-5 DMA Controller
0005	8237A-5 DMA Controller
0006	8237A-5 DMA Controller
0007	8237A-5 DMA Controller
0008	8237A-5 DMA Controller
0009	8237A-5 DMA Controller
000A	8237A-5 DMA Controller
000B	8237A-5 DMA Controller
000C	8237A-5 DMA Controller
000D	8237A-5 DMA Controller
000E	8237A-5 DMA Controller
000F	8237A-5 DMA Controller

Address[2]	Description
0020	8259A Interrupt Controller
0021	8259A Interrupt Controller
0022	8259A Interrupt Controller
0023	8259A Interrupt Controller
0024	8259A Interrupt Controller
0025	8259A Interrupt Controller
0026	8259A Interrupt Controller
0027	8259A Interrupt Controller
0028	Not used
0029	Not used
002A	Not used
002B	Not used
002C	Not used
002D	Not used
002E	Not used
002F	Not used

1. A4 - A15 are used to generate the chip select for the 8237A-5. A0, A1, A2, A3 are connected directly to the 8237A-5. The assigned addresses are 0000 - 000F. The DMA is optional.
2. A3 - A15(B) are used to generate the chip select for the 8259A. A0 is decoded directly by the 8259A. The assigned addresses are 0020-0021(B).

Address[3]	Description
0040	8253-5 Timer
0041	8253-5 Timer
0042	8253-5 Timer
0043	8253-5 Timer
0044	8253-5 Timer
0045	8253-5 Timer
0046	8253-5 Timer
0047	8253-5 Timer
0048	Not used
0049	Not used
004A	Not used
004B	Not used
004C	Not used
004D	Not used
004E	Not used
004F	Not used

Address[4]	Description
0060	8255A-5 PPI
0061	8255A-5 PPI
0062	8255A-5 PPI
0063	8255A-5 PPI
0064	8255A-5 PPI
0065	8255A-5 PPI
0066	8255A-5 PPI
0067	8255A-5 PPI
0068	Not used
0069	Not used
006A	Not used
006B	Not used
006C	Not used
006D	Not used
006E	Not used
006F	Not used

3. A3 - A15 are used to generate the chip select for the 8253-A. A0 is decoded directly by the 8253-A. The assigned addresses are 0040 - 0043.
4. A3 - A15 are used to generate the chip select for the 8255A-5. A1 and A0 are decoded directly by the 8255A-5. The assigned addresses are 0060 - 0063.

Detailed Memory Map——Continued

0060 — PORT A

Bit	Description
0	Keyboard Bit 0 — LSB
1	Keyboard Bit 1 —
2	Keyboard Bit 2 —
3	Keyboard Bit 3 —
4	Keyboard Bit 4 —
5	Keyboard Bit 5 —
6	Keyboard Bit 6 —
7	Keyboard Bit 7 — MSB

See Keyboard Specifications

0061 — PORT B — READ OR WRITE

Bit	Description
0	1 = 8253 Gate #2 Enabled
1	Speaker Data Out
2	Not used
3	Not used
4	Not Used
5	Sound Control 0
6	Sount Control 1
7	1 = Keyboard Clear

0062 — PORT C — READ/WRITE[5]

Bit	Description
0	(Out) Not Used
1	(Out) Multi-Data
2	(Out) Multi-Clock
3	(Out) Not Used
4	(In) Not Used
5	8253 Cut #
6	(In) Not Used
7	(In) Not Used

5. The hardware logic is configured so that Port C is split with an input at PC4 - PC7 and an output at PC0 - PC3.

Address[6]	Description
0080	DMA Page Reg. (Not Used)
0081	DMA Page Reg. (Ch 2)
0082	DMA Page Reg. (Ch 3)
0083	DMA Page Reg. (Ch 0, 1)
0084	Not used
0085	Not used
0086	Not used
0087	Not used
0088	Not used
0089	Not used
008A	Not used
008B	Not used
008C	Not used
008D	Not used
008E	Not used
008F	Not used

0081 — WRITE ONLY

Address	Description
Bit 0	DMA Ch 2 Address A16
Bit 1	DMA Ch 2 Address A17
Bit 2	DMA Ch 2 Address A18
Bit 3	DMA Ch 2 Address A19
Bit 4	Not used
Bit 5	Not used
Bit 6	Not used
Bit 7	Not used

0082 — WRITE ONLY

Address	Description
Bit 0	DMA Ch 3 Address A16
Bit 1	DMA Ch 3 Address A17
Bit 2	DMA Ch 3 Address A18
Bit 3	DMA Ch 3 Address A19
Bit 4	Not used
Bit 5	Not used
Bit 6	Not used
Bit 7	Not used

6. A3 - A15 are used to generate the chip select for the page register. The DMA is optional.

0083 — WRITE ONLY

Address	Description
Bit 0	DMA CH 0 — 1 Address A16
Bit 1	DMA CH 0 — 1 Address A17
Bit 2	DMA CH 0 — 1 Address A18
Bit 3	DMA CH 0 — 1 Address A19
Bit 4	Not used
Bit 5	Not used
Bit 6	Not used
Bit 7	Not used

Address[7]	Description
00A0	NMI Mask Register
00A1	NMI Mask Register
00A2	NMI Mask Register
00A3	NMI Mask Register
00A4	NMI Mask Register
00A5	NMI Mask Register
00A6	NMI Mask Register
00A7	NMI Mask Register
00A8	Not used
00A9	Not used
00AA	Not used
00AB	Not used
00AC	Not used
00AD	Not used
00AE	Not used
00AF	Not used

7. A0, A1, A2 = X.
   X = don't care

Detailed Memory Map——Continued

Address[8]	Description
00C0	Sound SN76496
00C1	Sound SN76496
00C2	Sound SN76496
00C3	Sound SN76496
00C4	Sound SN76496
00C5	Sound SN76496
00C6	Sound SN76496
00C7	Sound SN76496
00C8	Not used
00C9	Not used
00CA	Not used
00CB	Not used
00CC	Not used
00CD	Not used
00CE	Not used
00CF	Not used

00A0, 00A1[9]

Bit	Description
0	Not Used
1	MEMCONFIG 1
2	MEMCONFIG 2
3	MEMCONFIG 3
4	X
5	X
6	X
7	1 = Enable NMI

8. The chip select is decoded for Write Only, and approximately 42 wait states are inserted.
9. X = don't care.

Detailed Memory Map——Continued

Address[10]	Description
0200	Joystick
0201	Joystick
0202	Joystick
0203	Joystick
0204	Joystick
0205	Joystick
0206	Joystick
0207	Joystick
0208	Not used
0209	Not used
020A	Not used
020B	Not used
020C	Not used
020D	Not used
020E	Not used
000F	Not used

0201 — READ[11]

Bit	Description
0	R — X Position
1	R — Y Position
2	L — X Position
3	L — Y Position
4	R Button #1
5	R Button #2
6	L Button #1
7	L Button #2

10. The assigned addresses are 0020 - 0021. A0, A1, and A2 = X.
11. A Write to 0200 restarts the integrator. Therefore, Write to 0201 before the port for joystick valves.

Detailed Memory Map——Continued

0378

Bit	Description
0	Data Bit 0 — LSB
1	Data Bit 1 —
2	Data Bit 2 —
3	Data Bit 3 —
4	Data Bit 4 —
5	Data Bit 5 —
6	Data Bit 6 —
7	Data Bit 7 — MSB

0379

Bit	Description
0	Not used
1	Not used
2	Not used
3	0 = Error
4	1 = Printer Selected
5	0 = End Of Form
6	0 = Acknowledge
7	0 = Busy

Address[12]	Description
0370	Not used
0371	Not used
0372	Not used
0373	Not used
0374	Not used
0375	Not used
0376	Not used
0377	Not used
0378	Printer — Data Latch
0379	Printer — Read Status
037A	Printer — Control Latch
037B	Printer — Not used
037C	Printer - Data Latch
037D	Printer - Read Status
037E	Printer - Control Latch
037F	Printer — Not used

12. A0 and A1 are decoded by printer logic. The assigned addresses are 0378 - 0378. A2 = X, and X = don't care.

Detailed Memory Map——Continued

037A (037E)

Bit	Description
0	0 = Strobe
1	0 = Auto FD XT
2	0 = Initialize
3	0 = Select Printer
4	1 = Enable Interrupt
5	0 = Enable Output Data
6	Not used
7	Not used

Address	Memory Map
3D0	Not used
3D1	Not used
3D2	Not used
3D3	Not used
3D4	6845 Address Register
3D5	6845 Data Register
3D6	Not used
3D7	Not used
3D8	Mode Select Register
3D9	Color Select Register
3DA	Write Video Array Address & Read Status
3DB	Clear Light Pen Latch
3DC	Preset Light Pen Latch
3DD	Not used
3DE	Write Video Array Data
3DF	CRT Processor Page Register

Memory Map
Video Array 3DA & 3DE

Video Array[13] Address (3DA)	Read (3DA)	Write (3DE)
00 Bit 0	Display Inactive	Not Used
00 Bit 1	Light Pen Set	Not Used
00 Bit 2	Light Switch Status	Not Used
00 Bit 3	Vertical Retrace	Not Used
00 Bit 4	Not Used	Not Used
01 Bit 0		Palette Mask 0
01 Bit 1		Palette Mask 1
01 Bit 2		Palette Mask 2
01 Bit 3		Palette Mask 3
02 Bit 0		Border Blue
02 Bit 1		Border Green
02 Bit 2		Border Red
02 Bit 3		Border Intensity
03 Bit 0		Not Used
03 Bit 1		Not Used
03 Bit 2		Border Enable
03 Bit 3		4 Color High Resolution
03 Bit 4		16 Color Mode
10 — 1F Bit 0		Palette Blue
10 — 1F Bit 1		Palette Green
10 — 1F Bit 2		Palette Red
10 — 1F Bit 3		Palette Intensity

13. A Read at 3DA retrieves the status of the Video Array. To write to a register within the Video Array, first write the register address at 3DA and then write the register data at 3DE.

Detailed Memory Map——Continued

MEMORY MAP

Address	Description
3D8 Bit 0	High Resolution Clock
3D8 Bit 1	Graphics Select
3D8 Bit 2	Black And White
3D8 Bit 3	Video Enable
3D8 Bit 4	640 Dot Graphics
3D8 Bit 5	Blink Enable
3D9 Bit 0	Background Blue
3D9 Bit 1	Background Green
3D9 Bit 2	Background Red
3D9 Bit 3	Background Intensity
3D9 Bit 4	Foreground Intensity
3D9 Bit 5	Color Select

MEMORY MAP (3DF)

Bit	Description
0	CRT Page 0
1	CRT Page 1
2	CRT Page 2
3	Processor Page 1
4	Processor Page 2
5	Processor Page 3
6	Video Address Mode 0
7	Video Address Mode 1

Address	Description
03F0	DOR Register
03F0	DOR Register
03F1	DOR Register
03F2	DOR Register
03F3	DOR Register (Write Only)
03F4	FDC — Status (Read Only)
03F5	FDC — Data (R/W)
03F6	FDC — Status (Read)
03F7	FDC — Data (R/W)
03F8	Not used
03F9	Not used
03FA	Not used
03FB	Not used
03FC	Not used
03FD	Not used
03FE	Not used
03FF	Not used

A1 = X
DOR A2 = 0
FDC A2 = 1

Detailed Memory Map——Continued

3F2 (WRITE ONLY)

Bit	Description
0	Drive Select A*
1	Drive Select B*
2	0 = FDC Reset
3	1 = Enable DMA Req/Interrupt
4	1 = Drive A Motor On
5	1 = Drive B Motor On
6	1 = FDC Terminal Count
7	Not Used

To Select Drive A: Bit 0 · Bit 1*
To Select Drive B: Bit 0 · Bit 1*

256K MEMORY EXPANSION JUMPER OPTIONS AND CONFIGURATIONS

Memory Jumper Options

Listed below are the jumper options necessary for the correct operation of the Tandy 1000:

1. With E1-E2 jumper installed, memory on board will be 256K in size, without a jumper at this location, memory will be 128K.
2. With E3-E4 jumpered, no DMA is present and the memory starting address is 40000 hex. Without a jumper at this location, DMA is present and the memory starting address is 00000 hex.

If jumper E3-E4 is present, U13 (DMA) MUST NOT BE INSTALLED.

The first memory board MUST have DMA (U113) installed regardless whether 128K or 256K of memory is present.

With two boards installed, the first memory board must be 256K. See the chart below:

	E1-E2	E3-E4
Jumper in	256K	NO DMA MEM BASE ADDRESS 40000
Jumper out	128K	DMA PRESENT MEM BASE ADDRESS 00000

256K MEMORY EXPANSION THEORY OF OPERATION

Memory I/O

The 256K Memory Expansion board is a byte wide (8 bits at a time) memory array that will provide up to 256K bytes of RAM. With two fully populated RAM boards installed the maximum RAM of 640K allowed by the system memory map will be available. (128K on the main logic board and 512K on the two expansion RAM boards.) Memory Timing comes from the 14.31818 MHz signal on the bus. This signal is located at B30 on the expansion bus and is three times the CPU's operating frequency. This is also the operating frequency for the clocked delay line.

A Memory Read or Memory Write command starts the memory cycle as indicated by one of the RAS* (Row Address Strobe) 0,1,2, or 3 going active low. Memory options E1-E2 and E3-E4 in conjunction with address lines A16-A19 determines which one of the four RAS* signals goes active. The memory command starts a clocked delay line at 30ns starting AMUX (Address Multiplex) and WR* (Write/Read) and a full clock at 70ns for CAS* (Column Address Strobe) due to the alignment of the memory command to OSC (Oscillator).

The REFRESH signal identifies the MR* (Memory Read) signal that follows as a REFRESH cycle. REFRESH cycles have all four RAS* signals active simultaneously. No AMUX* or CAS* signals go active during a REFRESH cycle.

The Dynamic Memory lines between A0-A7 and A8-A15 are multiplexed by U6 and U10 with the normal state buffering A0-A7 to the dynamic memory array.

Direct Memory Access Controller

The DMA Controller U13 is a four channel device. Each channel is dedicated to a specific I/O function via a REQUEST/ACKNOWLEDGE handshake. The Controller transfers data between the particular I/O function and memory by emulation. The CPU read and write strobes the transfer from source to destination which takes place on the same cycle thus increasing through put.

A block diagram of the DMA function is shown in Figure 15. During DMA operation the DMA Controller is bus master and generates the bus address (A0-A19 and the required memory at I/O read/write strobe pairs. (MEMORY READ - I/O WRITE or I/O READ - MEMORY WRITE). The DMA Controller is also an I/O function. It is through this port that the DMA transfer parameters are programmed (start address, transfer count, etc.).

The controller occupies sixteen contiguous addresses (A0 thru AF). Because the controller can only output sixteen address bits, a four bit address extension register is required to allow DMA addressing capability to the entire one megabyte memory address space. The address extension register resides at a separate peripheral address of 080 - 083 hex.

For programming purposes, what is written on data lines D0-D3 to the address extension register will come out on address lines A16-A19 respectively during the appropriate DMA cycles. The following is a list of DMA Channels:

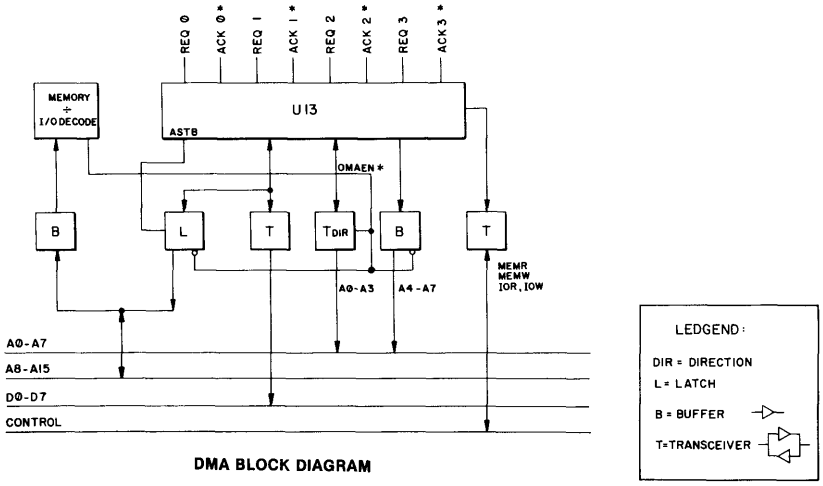
Register 80	Not Used
Register 81	Channel 2
Register 82	DMA Channel 3
Register 83	DMA Channels 0 and 1

The DMA Controller (Channel 0) is dedicated to memory refresh. The Channel 0 request line is tied to a flip-flop (U115 on the main logic board) that is pulsed at 15μs intervals. The DMA acknowledge line for Channel 0 (REFRESH) clears the flip-flop and instructs the system that the memory cycle in progress is a refresh cycle. The DMA Controller is programmed to step sequentially through memory addresses so that all 256 rows will be refreshed. DMA Channel 2 is assigned to the Floppy Disk Controller. DMA Channels 1 and 3 are uncommitted and are available on the bus.

The DMA Controller multiplexes data bits D0-D7 with address bits A8-A15. The presence of address information on these lines is indicated by a ADSTB (Address Strobe) being high. The falling edge of ADSTB latches address data into a 74LS373 (U14) latch. U14 is then enabled for output by a DMAAEN* (DMA Address Enable), output by the DMA Controller during DMA cycles. DMAAEN* also enables U16 (74LS125), buffering A4-A7, U18 (74LS670), A16,A19,U15 (74LS245), A0-A3, memory read, memory write, I/O read and I/O write.

DMAAEN* is used by U9 (82S153 IFL) to enable the data buffer U17 (74LS245) during DMA as well as during memory and I/O accesses to the board by the CPU.

U12 (74LS74) and U51 (74LS00) perform two functions. First the DMA Controller synchronizes READY to its input clock. Secondly, in order to mimic the CPU during DMA cycles, one wait state is inserted during either IOR* or IOW*.



DMA BLOCK DIAGRAM

Figure 15

INTRODUCTION TO RS-232 ASYNCHRONOUS COMMUNICATION BOARD

The RS-232 board is a single-channel asynchronous serial communications board. The heart of the board is the WD8250 Asynchronous Communications Element (ACE), that functions as a serial data input/output interface. It performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. Status information reported includes the type and condition of the transfer operations performed by the ACE as well as any error conditions. The WD8250 includes a programmable baud rate generator that allows operation from 50 to 9600 baud. The WD8250 can be software tailored to the user's requirements. It will add and remove start bits, stop bits, and parity bits. It supports 5-, 6-, 7-, or 8- bit characters with 1, 1½, or 2 stop bits. Diagnostic capabilities provide loopback functions of transmit/receive and input/output signals. Other features include:

- Full double buffering which eliminates the need for precise synchronization.
- Independent receiver clock input.
- False start bit detection.
- Line break generation and detection.
- Modem control functions: Clear To Send (CTS), Request To Send (RTS), Data Set Ready (DRS), Data Terminal Ready (DTR), Ring Indicator (RI), and Carrier Detect (CD).

Theory of Operation for RS-232

The RS-232 asynchronous communications board has various modes of operation that can be selected by programming the WD8250 ACE. The WD8250 is programmed by selecting the I/O address (3F8 to 3FE primary, and 2FB to 2FE secondary), and writing data out to the board. Address bits A0, A1, and A2 are used to define the modes of operation by selecting the different registers. The selection of certain registers is done by using the divisor latch access bit (Bit 7) of the line control register.

One interrupt is provided to the system for IRQ4 for primary operation, and IRQ3 for secondary operation. This interrupt is active high. Bit 3 of the modem control register must be set high in order to send interrupts to the system. When this bit is high, any interrupts allowed by the interrupt enable register will cause an interrupt.

Refer to Figure 16 for the Functional Pin Definitions, and Figures 17 and 18 for Timing Diagrams of the WD8250.

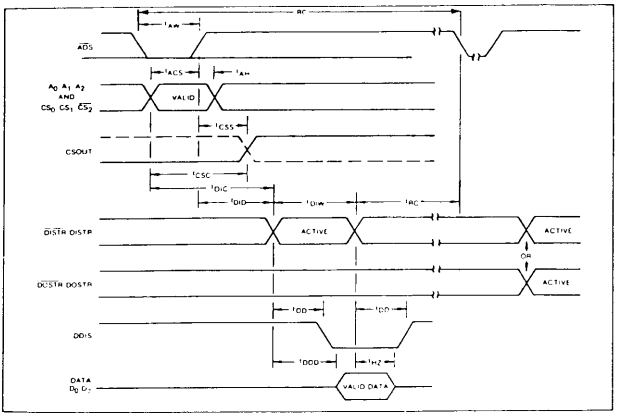
Figure 19 shows the Block Diagram for the RS-232 Adapter.

Figure 20 shows the Functional Pin Definitions for the 82S153 IFL.

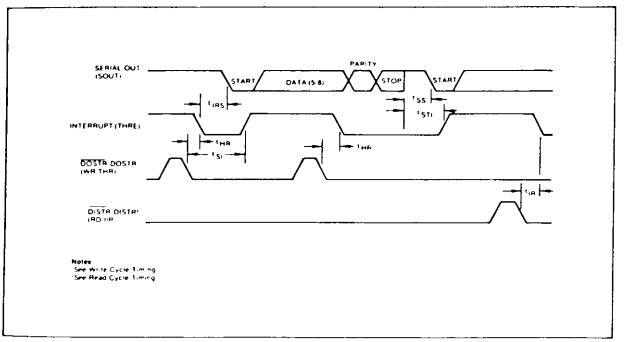
PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1-8	DATA BUS	D0-D7	3-state input/output lines. Bi-directional communication lines between WD8250 and Data Bus. All assembled data TX and RX, control words, and status information are transferred via the D0-D7 data bus.
9	RECEIVE CLK.	RCLK	This input is the 16X baud rate clock for the receiver section of the chip (may be tied to BAUDOUT pin 15).
10	SERIAL INPUT	SIN	Received Serial Data In from the communications link (Peripheral device, modem or data set).
11	SERIAL OUTPUT	SOUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12 13 14	CHIP SELECT CHIP SELECT CHIP SELECT	CS0 CS1 $\overline{CS2}$	When CS0 and CS1 are high, and $\overline{CS2}$ is low, chip is selected. Selection is complete when the address strobe $\overline{ADS}$ latches the chip select signals.
15	BAUDOUT	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the WD8250. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to (pin 9) RCLK.
16 17	EXTERNAL CLOCK IN EXTERNAL CLOCK OUT	XTAL 1 XTAL 2	These pins connect the crystal or signal clock to the WD8250 baud rate divisor circuit.
18 19	DATA OUT STROBE DATA OUT STROBE	$\overline{DOSTR}$ DOSTR	When the chip has been selected, a low $\overline{DOSTR}$ or high DOSTR will latch data into the selected WD8250 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DOSTR}$ — high or DOSTR — low.
20	GROUND	V_{SS}	System signal ground.
21 22	DATA IN STROBE DATA IN STROBE	$\overline{DISTR}$ DISTR	When chip has been selected, a low $\overline{DISTR}$ or high DISTR will allow a read of the selected WD8250 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DISTR}$ — high or DISTR — low.
23	DRIVER DISABLE	DDIS	Output goes low whenever data is being read from the WD8250. Can be used to reverse data direction of external transceiver.
24	CHIP SELECT OUT	CSOUT	Output goes high when chip is selected. No data transfer can be initiated until CSOUT is high.
25	ADDRESS STROBE	$\overline{ADS}$	When low, provides latching for register. Select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$) NOTE: An active $\overline{ADS}$ signal is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, the $\overline{ADS}$ input can be tied permanently low.
26 27 28	REGISTER SELECT A2 REGISTER SELECT A1 REGISTER SELECT A0	A2 A1 A0	These three inputs are used to select a WD8250 internal register during a data read or write.
29	NO CONNECT	NC	No Connect
30	INTERRUPT	INTRPT	Output goes high whenever an enabled interrupt is pending.
31	OUTPUT 2	$\overline{OUT2}$	User-designated output that can be programmed by Bit 3 of the modem control register = 1, causes $\overline{OUT2}$ to go low.
32	REQUEST TO SEND	$\overline{RTS}$	Output when low informs the modem or data set that the WD8250 is ready to transmit data.
33	DATA TERMINAL READY	$\overline{DTR}$	Output when low informs the modem or data set that the WD8250 is ready to communicate.
34	OUTPUT 1	$\overline{OUT1}$	1 causes $\overline{OUT1}$ to go low.
35	MASTER RESET	MR	When high clears the registers to states
36	CLEAR TO SEND	$\overline{CTS}$	Input from DCE indicating remote device is ready to transmit.
37	DATA SET READY	$\overline{DSR}$	Input from DCE used to indicate the status of the local data set.
38	RECEIVED LINE SIGNAL DETECT	$\overline{RSLD}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions.
39	RING INDICATOR	$\overline{RI}$	Input, when low, indicates that a ringing signal is being received by the modem or data set.
40	+5V	V_{CC}	+5 Volt Supply.

Figure 16

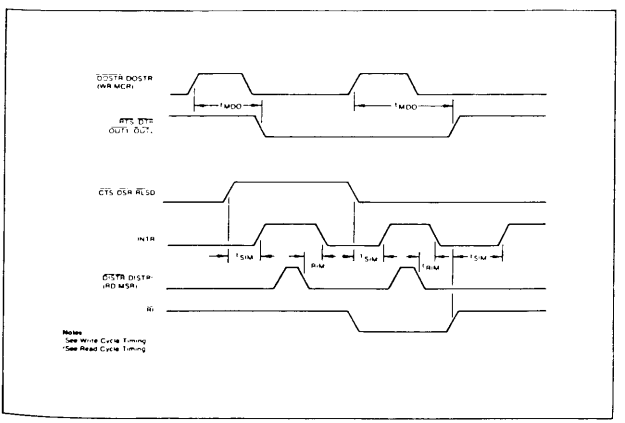
WD8250



READ CYCLE TIMING



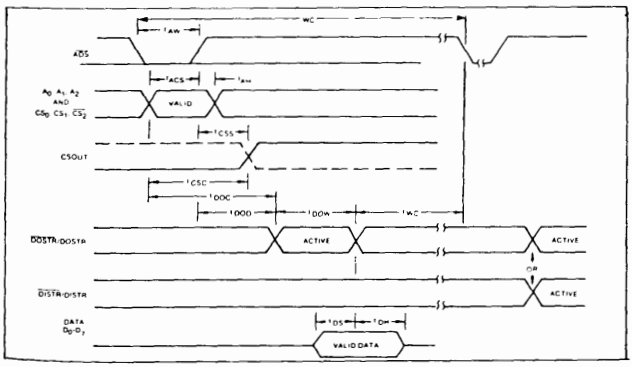
TRANSMITTER TIMING



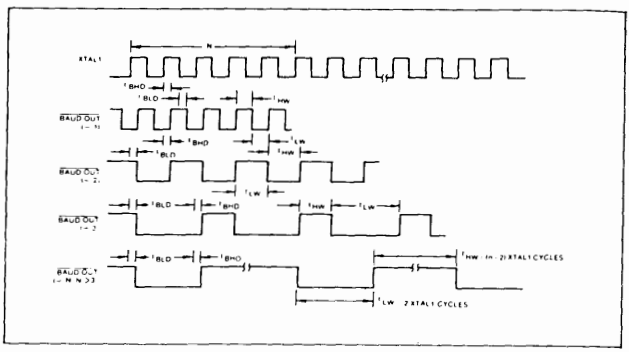
MODEM CONTROLS TIMING

Figure 17

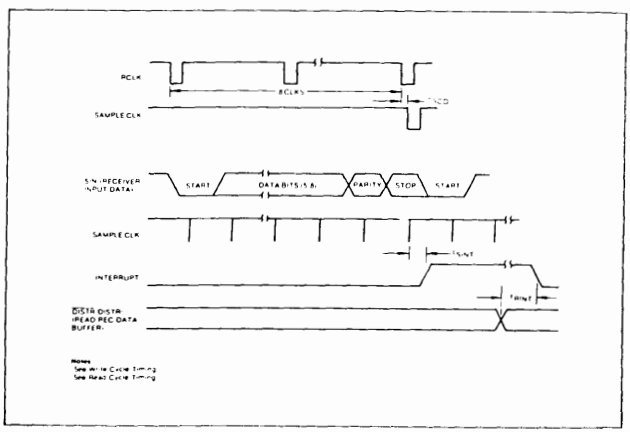
WD8250



WRITE CYCLE TIMING



BAUDOUT TIMING



RECEIVER TIMING

Figure 18

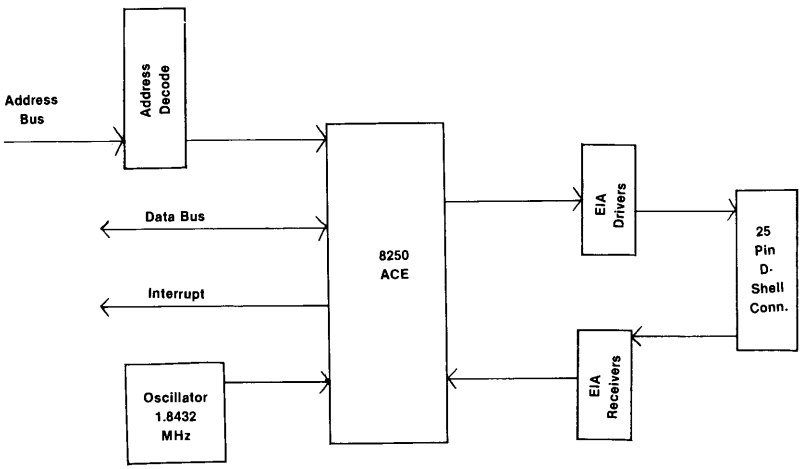


Figure 19
RS-232 Asynchronous Communications Adapter Block Diagram

82S153 IFL Pin Descriptions

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	ADDRESS ENABLE	AEN	Indicates DMA cycle when high, CPU cycle when low.
2-8	ADDRESS LINES	A3-A9	These address lines are used for decoding the address space 2F8-2FF (secondary) or 3F8-3FF (primary).
9	SECONDARY INTERRUPT REQUEST	IORQ3 address space.	Sends interrupts to the CPU while operating in the secondary
10	GROUND		
11	PRIMARY INTERRUPT REQUEST	IORQ4	Sends interrupts to the CPU while operating in the primary address space.
12	PRIMARY OR SECONDARY UARTS	P or S	An input that determines which address space will be used. Primary (3F8-3FF) when high or secondary (2F8-2FF) when low.
13	UART INTERRUPT	INT	Receives interrupt signal from the 8250.
14	UART CHIP SELECT	UCS	Enables the 8250 ACE when low.
15	NOT USED		
16	NOT USED		
17	DATA CHIP SELECT	DCS	Enables the data bus buffers when low.
18	NOT USED		
19	NOT USED		
20	VCC		

Figure 20

INTRODUCTION TO THE 300 BAUD MODEM

The 300 baud modem is a plug-in option for the Tandy 1000. This modem is an auto answer-auto originate device with tone and pulse-type dialer circuitry. See Figure 21. It is controlled by a 6805 single-chip microprocessor (U7), and simple ASCII commands control the operation of the modem.

These ASCII commands are supplied through the on-board UART. The UART converts parallel commands to serial data for the modem. The microprocessor converts the serial data into parallel data and controls the modem using the input/output ports.

The modem circuitry is divided into six major subsections:

- Modem filter
- Carrier detect section
- UART
- Microprocessor section
- Tone dialer section
- Telephone interface section

Theory of Operation for the 300 Baud Modem

Modem Filter

The modem filter section consists of U3, parts of U9 and U6, and the modem chip U1. U3 is an MC145440 filter chip. It contains two switched capacitor filters and an operational amplifier. Depending on the mode of operation, one filter processes the receive carrier, while the other filter processes the transmit carrier. The operational amplifier is used as a duplexer. This device allows transmit carrier to be amplified to the telephone interface transformer but not to the receive side of the filter.

The filter chip is powered by +5.0 volts from the computer's main power supply. Internal circuitry generates a false ground at Pin 5, which is one-half the Vcc power of the chip. All signals within the filter chip swing around this level. The false ground is shown as a chassis ground symbol on the schematic, and the true ground (0.0 VDC) is shown with a signal ground symbol (a triangle).

U3 uses a 4.00 MHz (Y1) crystal to generate an internal clock. The frequency is also divided by 4 to generate a 1.00 MHz clock for the modem chip. This clock reference is supplied at Pin 11 of U3.

Transmit Section

Serial data from the UART is supplied at Pin 11 of U8. The modem chip, U1, frequency modulates the high and low state of the input at Pin 11 and generates transmit carrier. Transmit carrier is supplied to the filter from Pin 9 of U1. A digitally-generated sine wave is produced at this pin and is DC decoupled by C2. R1, a 10K pot, adjusts the level of transmitter carrier to the filter chip at Pin 2. The signal is passed through summing amplifier U2 and applied to the duplexer input. R3 passes most of the signal energy to C1 and on to the secondary of T1.

Receive Section

The receive carrier passes through T1 and is applied to pin 17. Transmit carrier is sensed at pin 15 of U3 and is subtracted from the smaller received carrier by the duplexer op-amp in U3. The duplexer's output is at Pin 16, and the receive filter input is tied to this pin. Once the receive carrier is processed by the receive filter, the output at Pin 14 is decoupled away from false ground by C13 and allowed to swing around system ground. R16, R21, and part of U6 give about 10 dB of gain, and the received carrier is filtered by R29 and C23. C22 decouples the signal back to the false ground reference, and the signal is applied to the limiter, U9. After being squared by the limiter, the modem chip U1 detects any FSK activity and generates a serial output for the UART at pin 7.

Carrier Detect

The carrier signal from the receive side of the modem filter is measured to determine whether there is sufficient strength to allow error-free communications. Once the receive carrier is amplified by U6, C21 decouples the signal, and it is applied to a half-wave amplifier rectifier U6. Using a gain of almost 4, this op-amp circuit passes through the positive half of the carrier signal to a filter capacitor. CR6 passes the positive half of the carrier, while CR5 "shorts out" the negative half.

C2D filters resulting positive DC signal, and the resulting voltage is compared to a reference voltage at Pin 7 of U9. R19 and R20 hold this voltage to about 0.8 Volts. At Pin 6 of U9, Pin 1 changes from a high voltage to a low voltage. R32 and Pin 8 of U9 make up another voltage comparator, but notice that this time, the positive input to the comparator is referenced at false ground (2.5 volts). When the voltage at R32 falls below 2.5 volts, the output at Pin 14 of U9 goes from a low to a high. This output is designed to "short out" the output of the limiter at Pin 2. When Pin 14 goes high, it actually forces a transistor to turn off and allow limited carrier to be applied to Pin 1 of U1. Of course, if there are fewer than 0.8 volts at Pin 6 of U9, Pin 14 keeps the limited output shorted, and there is no received FSK for U1 to demodulate.

Unlike other modems, the carrier detect level at Pin 1 of U9 is *not* directed to a voltage translator for use at Pin 8 of the RS-232 connector. Instead, the 300 baud modem signals the microprocessor with the carrier detect signal, applying the output of U9 to Pin 26 of U7. The microprocessor makes the decision and controls Pin 38 of the UART at the proper time.

UART Section

The UART section consists of U8 (the UART), its crystal Y2, a transmission buffer U12, and a gate array U11. In operation, the 1000 port is connected to these 3 devices. Depending on the selection of jumper plug E1-3, the primary or secondary serial channel addresses are decoded by U11. Bus data is switched by U12. The UART controls its direction at Pin 1, and the gate array U11 controls the master enable. U8 operates just like any UART in that it converts parallel data from the port into serial data for the modem's microprocessor. Notice that DTR is *not* used for this modem.

Microprocessor Section

The 6805 microprocessor has 1024 bytes of ROM and 64 bytes of RAM. It communicates with the user by using the serial inputs and outputs supplied by the RS-232 connector. It also controls all protocol timing and telephone signaling.

U7 receives a 4.00 MHz clock reference from the filter crystal. The crystal is tapped at Pin 8 of U3 and is not buffered. When power is applied to the modem and capacitor C26 charges high, the microprocessor starts its internal control program.

Serial input from the UART interface is applied to the microprocessor's interrupt input at Pin 2. When the microprocessor is echoing commands or listing user options, it signals Pin 12 in a serial manner. Because two inputs must share one line of the UART, R15 is used as a resistive multiplexer. The output of U1 Pin 7 cannot be made to "turn off." Hence, it might have a low voltage at this pin. R15 isolates the microprocessor's output from the modem chip's output. If U1 Pin 7 is low, a high at Pin 12 of U7 supplies current to R15 and to the UART. Even though the low at Pin 7 of U1 somewhat loads the output at Pin 28 of U7, there is still sufficient voltage to supply U8 with the proper high level signal.

When the modem is in an ON-LINE condition, Pin 12 of U7 is configured as an input pin. At this time, the microprocessor is monitoring any data being received by the modem. Since R15 is not driven high by pin 12 any more, the normal transitions on Pin 7 of U1 control the translation of signals at Pin 38 of U8.

The microprocessor is at the same time controlling the relays in the telephone interface. K2 determines whether or not the modem is connected to the telephone line. It is controlled by the microprocessor through relay drive U4, Pins 12 and 13. K1 is used during pulse dialing. It is controlled by relay driver U4, Pins 1 and 14. The diodes across the two relay coils prevent counter-EMF chatter and protect the driver from any high voltage spikes.

Tone Dialer Section

The tone dialer chip U10 controls the telephone interface circuitry using tone signaling. This chip has its own crystal (Y3, a 3.579545 MHz device). A binary coded decimal number is applied to the BCD input of this chip by U7. When Pins 10, 11, 12, and 13 have a digit applied to them, the microprocessor supplies a timed high signal to Pin 15. This high enables the tone generator, and Pin 17 outputs a digitally-generated sine wave of the proper frequency.

The tone output is DC decoupled by C24, forcing it to swing around system ground. U2, along with R17 and R4, amplifies the tone signal by a factor of 4 and applies it to the same duplexer used by the modem transmit carrier. (There is no carrier at this time.) Once it passes through the transformer, it is applied to the telephone line.

Telephone Interface Section

The telephone interface section consists of a coupling transformer, two sets of relay contacts, transient suppressors, and a ring detector.

The coupling transformer isolates modem ground and passes tone signals through in both directions. It also protects the telephone line from high voltage due to its breakdown characteristics.

As mentioned before, K2 is the hook relay, and K1 is the pulse dial relay. When the modem is ON-LINE, K2 is on, shorting out Pins 1 and 8. (Also notice that it shorts out 9 and 15.) Assuming that you are not pulse dialing at this time, K1 is not active, and a connection occurs between the contacts of K2 and the primary of T1.

When the modem pulse dials, K1 switches on and off, breaking and making the T1 connection to TIP and RING. The Central Office detects these makes and breaks, and the number is pulse-dialed. R9 and C36 form a stubbing network for protection of K1's contacts. CR2 prevents harmful voltage transients from being passed to the telephone line.

Bridge rectifier CR8 accomplishes ring detection. When ring voltage is applied to TIP and RING, CR8 full-wave rectifies the sine wave and applies DC to filter C12. This voltage is allowed to turn on transistor Q1 which, in turn, lights the LED within opto-isolator U5. The transistor inside U5 follows the pulsating ring voltage and outputs a 5.0 volt square wave to Pin 19 of the microprocessor. The microprocessor makes the decision whether or not to activate K2 and answer the call.

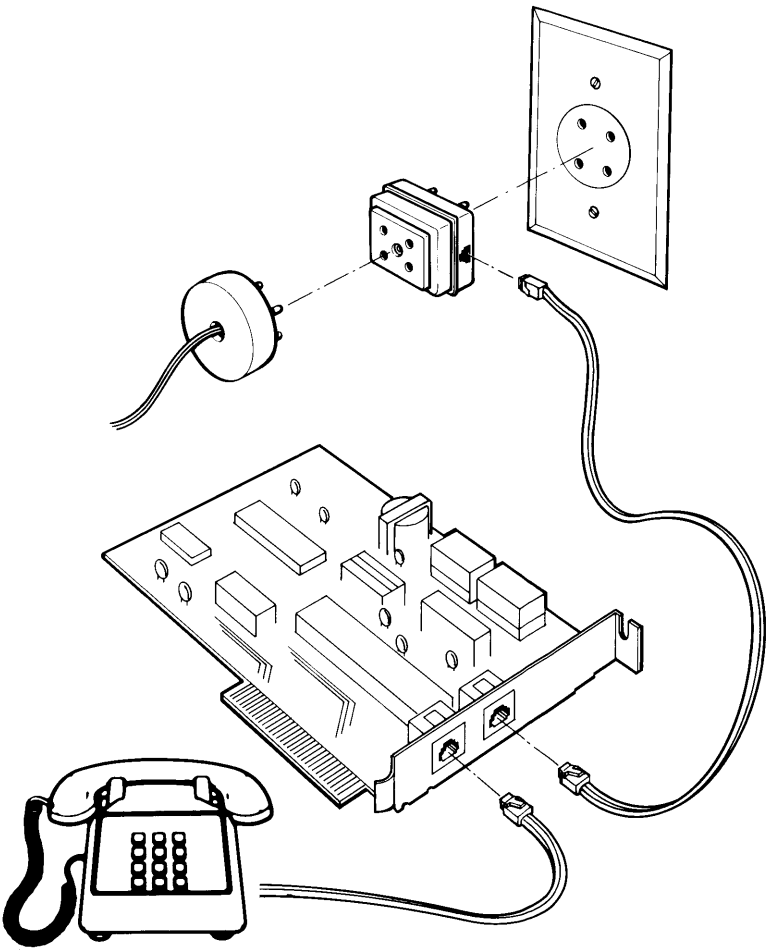


Figure 21

TANDY 1000 MOUSE/CLOCK/CALENDAR

Introduction

The Mouse Clock/Calendar Board interfaces the DIGI—Mouse pointing device (Cat. No. 26-1197) to the Tandy 1000. The application programs that require the DIGI-Mouse pointing device can be used on the Tandy 1000. Also the battery backed clock/calendar allows the user to run the software provided on the diskette that comes with the owner's manual.

Specifications

Dimensions: Standard half size board (5 x 4.2 inches).

Battery: 3.0-Volt Lithium coin cell, type 2320 (Cat. No. 23-163). The battery life is one year.

Processor: 8042 8-bit single chip processor.

Clock Speed: 7.16 MHz

Ambient Temperature Range:
55° to 95° F (12° to 35° C)

Storage Temperature Range:
−40° to +160° F (−40° to 71° C)

Theory of Operation (Hardware)

Look at the block diagram (Figure 22) while reading the information below.

Bus I/F

Data, address, and control signals of the 1000 interface bus are buffered by U9 (an octal bus transceiver) and U7 (an octal buffer/line driver with 3-state outputs).

Chip Select and Reset Logic

The address lines are decoded by U2, U5, and U6. When the 1000 writes or reads to Ports 2FC or 2FE, a chip select signal is generated at Pin 6 of U2. The cip select controls U9 (the data buffer) and U3 (the 8042 processor).

During DMA cycles, the AEN signal from the 1000 bus, disables the chip select signal at Pin 1 of U7. An active AEN signal disables the 1Y outputs of U7, causing the A08 signal from Pin 12 of U7 to float and to be pulled high by R20. U5 then inverts the A08 signal, ensuring that the chip select is disabled during DMA.

One half of U1 (a dual D-type flip-flop) is used in a "divide by 2" configuration. The 14.32 MHz oscillator signal from the 1000 interface bus is divided in half for a clock speed of 7.14 MHz, to be used by the 8042 processor. The 7.14 MHz clock is at Pin 5 of U1.

The other half of U1 is used as a reset latch. A reset signal is provided for the 8042 processor by ORing together the System Reset signal from the computer interface bus and the signal from the reset latch at Pin 11 of U2. The 8042 processor can be reset by a system reset or a write to I/O port 2FF. A write to I/O port 2FD clears the reset signal.

8042 Processor

In the heart of the option board is the 8042 processor (U3). This processor acts as an input port for serial information from the DIGI-Mouse and the Clock/Calendar chip (U8). It then translates this information to a parallel format and controls its transfer to the computer interface bus. The Clock/Calendar option board uses interrupt request IR3 to inform the 1000 when it is ready to transfer data.

DIGI-Mouse Buffers and Filters

A 9-Pin DB jack at J2 connects the DIGI-Mouse to the clock/calendar board. RC filtering is used to reduce noise in the inputs. U4 (a CMOS hex schmitt trigger) provides further buffering and waveshaping of the DIGI-Mouse inputs, which are interfaced to the processor chip through its peripheral port bits P10 to P16.

Clock Chip

The Phillips-Signetics Clock/Calendar Chip (U8) interfaces directly to U3 at its peripheral port bits P17, P20-P23, and P27. The time base for the clock ship is a 32.768KHz crystal, which is similar to that found in watches. The battery MUST be installed for the clock function to work. When a power failure occurs, the chip indicates this by sending a low-battery signal (POWF) to the 8042 processor.

Theory of Operation (Software)

User specifications:

- The motion sensor is oriented with the connecting cable and buttons pointing away from the user, the positive x axis extends to the right and the positive y axis extends toward the user.
- Maximum motion allowed before it is detected is 1/80 of an inch along either axis. This distance is called a mickey.
- The minimum unit of time for the Clock/Calendar chip is 1 minute. Maximum accuracy is $\pm$ ½ minute. The units of time accepted by the chip are minutes, (24) hours, day of month, and month.

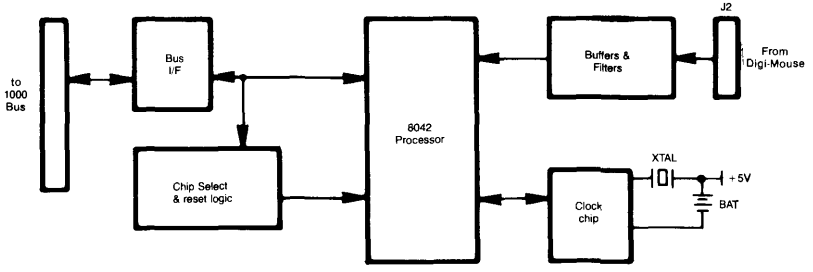


Figure 22

DIGI-Mouse/Clock Controller Board
Block Diagram I/F

- There are 3 modes for the mouse's motion data and button data that can be transfered to the host: the internal timed data poll mode, the event data poll mode, and the host request data poll mode.
- To communicate with the clock/calendar chip, the user employs the set time command and a read time command.

I/O Ports used by the Clock/Calendar Board:

8042 Data Port	2FC
8042 Command/Status Port	2FE
8042 Set RESET 8042 Port	2FF
8042 Clear RESET 8042 Port	2FD

Layout of the 8042's status port (2FE):

Read by the 8088:

Bit #0 = Output register full flag	1 = full
Bit #1 = Input register full flag	1 = full
Bit #2 = F0 flag - not used	
Bit #3 = F1 flag - command flag	1 = button up
Bit #4 = Primary button status	1 = button up
Bit #5 = Secondary button status	1 = button up
Bit #6 = Tertiary button status	1 = button up
Bit #7 = Calendar power status	1 = power has failed

Written to by the 8088:

This is the same as for the data written to Data Port 2FC, except the F1 (command) flag in 8042's status port is set.

Output:

When sending data or commands from the 8088 to the 8042, the following procedure must be used:

1. Check the status port (2FE) of the 8042 to see if the input port full flag is set (Bit 1).
2. If the flag is set, wait until the 8042 clears it. If it is not cleared within 1 millisecond, reset the 8042 chip because it is locked up.
3. If the flag is clear, proceed.
4. Check the length of the command. If it is equal to 1, then send the data to 2FE, and stop here.
5. If the length equals 2 or more, then send the data to 2FC, and proceed.
6. Wait until the input port full flag is cleared by the 8042 before sending the next byte of data.
7. When the length equals 1, send it to 2FE, and stop here.

Formats of Commands to the 8042:

Command	Header	Data
Set Time	01	All data must be in BCD format. 1st byte = minutes. 2nd byte = hurs (24 hour clock). 3rd byte = day of the montth. 4th byte = month.
Read Time	02	None Returns data packet "R".
Set Mouse Motion Interrupt and	08	Output is 2 bytes. 0 = disable function. 1 – 255 = net number of "mickeys" to be moved before interrupt is triggered. Returns data packet "M".
Button Interrupt		0 = disable function. 1 – 255 = enable function Returns data packet "B".
Set Timer Interrupt	20	Outputs 1 byte of data 0 = disable function. 1 – 255 = enable function Returns data packet "A".

(Timer is set to interrupt approximately 40 times per second if the data is available to send.)

What is happening:

The 8042 is interrupted every time data is written to the input port 2FC (or 2FE, which set the command flag). The 8042 moves the data from the input register into the input buffer and increments a counter. It then returns to the point in the mouse data sampling and processing cycle at the point of interruption.

During each cycle, the 8042 checks the command flag to see if a command has been received. If the command flag is set, the 8042 checks the header byte to determine which command is in its input buffer. It then compares the counter to the number of bytes in that command. If any of these tests fails, the 8042 resets the pointer to the input buffer, clears the counter and the command flag, and continues with its normal cycle. If all the ttests succeed, the 8042 jumps to the routine that handles that command. Each command has the requirement to reset the buffer pointer, the counter, the command flag and then return control to the normal process.

Input:

Data transfer between the 8042 and the main processor (8088) uses the interrupt mode, the poll mode, or both. the 8042 interrupts the 8088 by toggling Port 2, Bit 4, which is connected through a buffer to the 8259A interrupt controller chip. The clock/calendar board uses IR3 as an interrupt. Internally, the 8042 knows if the 8088 has read/written a byte from/to it by checking the status of the OBF/IBF flags. Three procedures are available to transfer the data from the 8042 to the 8088. They are discussed below.

Mode 1: Full interrupt mode

This mode uses the interrupt line to signal each byte to e transmitted. As each byte is transmitted, the common procedure below is executed except Mode 3 must have the latched interrupt cleared after each byte is processed. This mode may be the fastest mode when only the clock interrupt is actively being triggered.

Mode 2: Initial interrupt and poll mode

This mode uses the interrupt line to signal the start of a data packet, and polls the rest of the packet. It clears the latched interrupt only after all the data packet is transmitted. it uses the common procedure outlined below.

Mode 3: Poll only mode

This mode does not use the interrupt signal at all. It uses only the output register full flag in the 8042's status register (Port 2FE).

Common procedure:

The 8088 must have the following initialized before any interrupt mode is used:

- A hardware interrupt vector at 002C.
- An interrupt controller at port 21 (ANDed with a F7).

The 8042 has a data packet set up in its output buffer and begins transmitting by placing the "header" into the output register (Port 2FC). Placing the header byte into the output register sets the output register full flag in the status register (Port 2FE, Bit 0) and sends a signal on the interrupt line to the 8088 (via the 8259). The 8042 begins its normal processing cycle, testing the output register full flag on each cycle.

If the flag is set, the 8042 sends another signal on the interrupt line. If the flag is cleared and the packet still continues to send, the 8042 places the next data byte into the output register and sends a signal on the interrupt line to the 8088. If the flag is cleared and the data packet is empty, the 8042 does NOT send an interrupt signal, but continues with its normal processing.

On the 8088 side, the "mouse" interrupt has a priority behind the 8253 timer, keyboard, and hard disk. This means that when the interrupt enters its routine, the higher-level interrupts are enabled. The interrupt handler routine should do all the following:

- Ensure that the 8042 is generating the interrupt by placing a data byte in its output register.
- Identify the type of data packet by its "header" byte and switch to the appropriate routine when the entire data packet is received.
- After the data packet is processed, clear or reset the buffer pointers, counters and the latched interrupt.

Format of Data Packets from the 8042:

Data Packet	Header	Data
Mouse data All data Motion data only	 "A" "M"	4 bytes of data 1st byte = MSB of Delta x 2nd byte = LSB of Delta x 3rd byte = MSB of Delta y 4th byte = LSB of Delta y

(The button data is found in the status register (Port 2FE.)

Mouse data Button data only	 "B"	none data found in status register (Port 2FE bits # 4, 5, 6)
Read time data	"R"	4 bytes of data in BCD format 1st byte = minutes 2nd byte = hours (24-hour clock) 3rd byte = day of month 4th byte = month

Initialization Procedures of 8088:

The following hardware and software interrupts should be initialized:

Description	Address Type
Hardware interrupt vector (INT 0B)	002C Doubleword Pointer
Application interrupt vector (INT 33)	00CC Doubleword Pointer
Hardware interrupt controller (IR3)	Port 21 (reset Bit 3)
Video display interrupt (INT 10)	0040 Doubleword Pointer

Operation of the Clock/Calendar:

When the 8042 receives either the Set Time or Read Time command, it shuts off all other operations until it is finished with the command. All the resources of the 8042 are required to communicate with the clock/calendar chip.

In the Set Time command, the 8042 breaks up the 4 bytes of time data into 4 packets and sends them serially a bit at a time. Upon completion, the 8042 resumes normal operation.

In the Read Time command, the 8042 sets up bit serial communications with the clock/calendar chip and builds 4 time data packets. The 4 packets are converted to bytes and placed in the output buffer behind the "R" header byte. The 8042 sets up a Read Time data packet to be sent to the 8088 and returns to normal operation.

If the power fails, bit data is set in the status register (Port 2FE Bit 7). First, check to see if the power failure is temporary. (Perhaps the battery lost contact with the clock circuit because of a bump or jarring of the equipment.) To check for temporary failure, issue a Set Time command. If the power failure bit is set to zero everything is normal. If the power fialure bit is not reset, then the battery either is dead or is dislodged from its holder clip. After replacing or resetting the battery, issue the Set Time command to ensure proper operation.

Operation of the 8042:

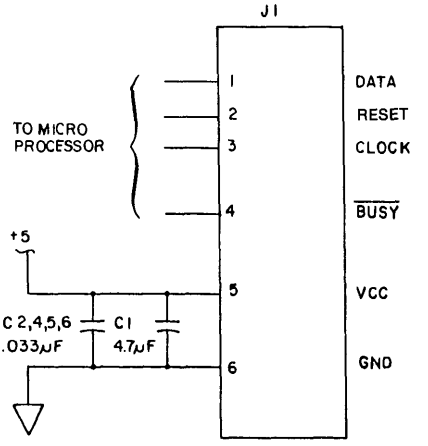
Upon power up/RESET, the 8042 initializes the system by zeroing all RAM and clearing all flags, ports, and registers. It then sets up the default conditions and enters the normal mouse data procesing cycle, which follows:

1. The 8042 takes a copy of the Mouse/Clock/Calendar data port (P1) and saves copy.
2. It then checks to see if there is any change in the status of the buttons. If there is, the 8042 sends a copy to the status register.
3. Next, the 8042 determines the Delta x changes or Delta y changes. Both Deltas use the same process.
4. The 8042 retrieves the copy of Port P1 and compares the bit pattern of xA and xB to the old copy to see if any changes have occured. If a change has occured then, the 8042 determines whether the change is +1, −1, or null. (Null occurs when the 8042 misses 2 state changes of xA and xB.)
5. The Delta x (or y) working accumulator ±32735 units) is then either incremented or decremented respectively. A null result does not affect the accumulators.
6. At this point, the 8042 checks the event-triggered data polls for motion and button data. If either occurred, then the 8042 transfers the values in the working accumulators to the output buffer behind the appropriate header byte and clears the working accumulators to zero. If not, then the 8042 checks to see if any input from the 8088 has been received by checking the F1 command flag. If there is input in the input buffer, the 8042 tests the header to see which bit is "on" and jumps to the routine that handles that command.
7. After checking for input, the 8042 then checks the internal timer to see if anything has timed out. Two items are connected to the timer flag, the 8042 and the timed data transfer interrupt. All outputs to the 8088 are tied to the timer. Each time the timer times out, the 8042 checks the output register full flag to see if it is set.

If the flag is set, the 8042 sends off a signal on the interrupt line to the 8088, resets the timer, and returns to normal operation. The 8042 checks to see if it needs to send any more data. If it does, it moves the next data byte to the output register, sends a signal on the interrupt line, and returns to normal operations. If the output buffer is empty, the 8042 simply returns to normal operation. Connected to the timer is the timed data transfer interrupt. When the timer interrupt is enabled, the 8042 also checks to see if the timer has timed out. If it has, then the 8042 transfers the mouse data from the working accumulators to the output buffer behind the header byte and ships it to the 8088. It then clears the working accumulators and returns to the start of the cycle.

KEYBOARD ASSEMBLY

The Tandy 1000 has a 90-key keyboard that includes 12 function keys, a numeric keypad, and special purpose keys for paging. The keyboard is connected to the Main Unit by a coiled cable and operated at a maximum distance of 4 feet from the main unit. Figure 23 shows the interconnecting cable connector to the keyboard assembly. The cable assembly can be disconnected from the keyboard assembly during repair.



Keyboard Assembly Connector

Figure 23

Keyboard Specifications

The keyboard is fully encoded with microprocessor control, and requires +5 VDC supplied from the Main Unit.

1. Key Type — all keys generate "make" and "break" codes. See the Key Code Chart. Break codes are formed by adding 80H to the make code. Keys 49 and 71 have alternate action that "makes" on one actuation of the key and "breaks" on succeeding actuation. No code is generated for these two keys when the key is released.

2. Number of Keys — 90

3. Repeat Strobe — there is a repeat strobe of 66 to 111 mSec when any key is depressed for more than 1 second, with the exception of SHIFT, CTRL, CAPS, ENTER, and NUMBER LOCK.

Key Code Chart

Key Number	Legend	Scan Code
1	F1	3B
2	F2	3C
3	F3	3D
4	F4	3E
5	F5	3F
6	F6	40
7	F7	41
8	F8	42
9	F9	43
10	F10	44
11	F11	59
12	F12	5A
13	INSERT +	55
14	DELETE -	53
15	BREAK	54
16	ESC	01
17	1 !	02
18	2 @	03
19	3 #	04
20	4 $	05
21	5 %	06
22	6 ^	07
23	7 &	08
24	8 *	09
25	9 (	0A
26	0)	0B
27	- _	0C
28	= +	0D
29	BACKSPACE	0E
30	ALT	38
31	PRINT	37
32	7 (backslash)	47
33	8 (Tilde)	48
34	9 PG UP	49
35	TAB	0F
36	Q	10
37	W	11
38	E	12
39	R	13
40	T	14
41	Y	15
42	U	16
43	I	17
45	P	19

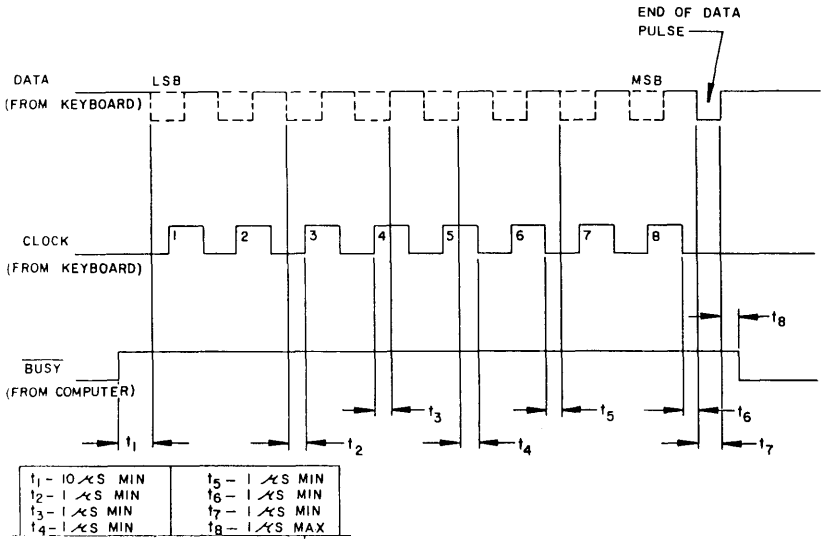
Key Number	Legend	Scan Code
46	{ [	1A
47	}]	1B
48	HOLD	46
49	NUM LOCK	45
50	4 :	4B
51	5	4C
52	6	4D
53	CTRL	1D
54	A	1E
55	S	1F
56	D	20
57	F	21
58	G	22
59	H	23
60	J	24
61	K	25
62	L	26
63	; :	27
64	' "	28
65	ENTER	1C
66		29
67	HOME	58
68	1 END	4F
69	2 (Grave)	50
70	3 PG DN	51
71	CAPS	3A
72	SHIFT	2A
73	Z	2C
74	X	2D
75	C	2E
76	V	2F
77	B	30
78	N	31
79	M	32
80	, <	33
81	. ‡	34
82	/ ?	35
83	SHIFT	36
84		2B
85		4A
86		4E
87	0	52
88		56
89	ENTER	57

90 (Space Key)

91 thru 95 — reserved for International

Keyboard Timing

Figure 24 is the timing chart for the Tandy 1000 Keyboard Assembly.



Keyboard Assembly Timing Chart

Figure 24

Keyboard Layout

Shown below is the keyboard layout and number designation of the keys on the Tandy 1000 keyboard. They should be used with the Key Code Chart for determining data value transmitted by the keyboard.

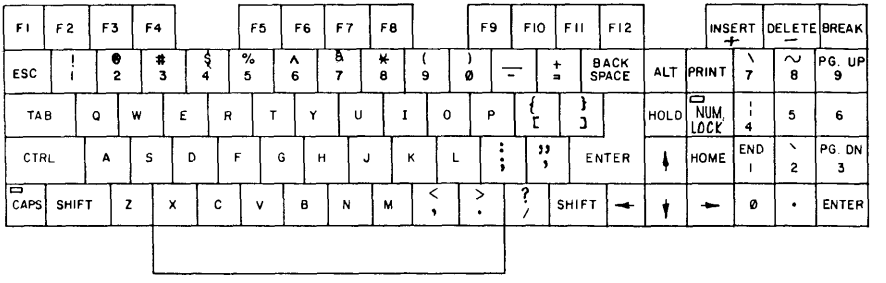
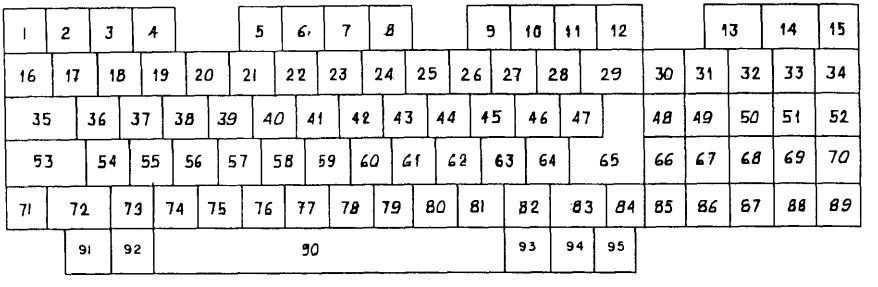


Figure 25. Keyboard Identification



NOTE: KEYS 91 THRU 95 NOT USED ON U.S. VERSION, USED ON INTERNATIONAL VERSION ONLY

Figure 26. Key Number Identification

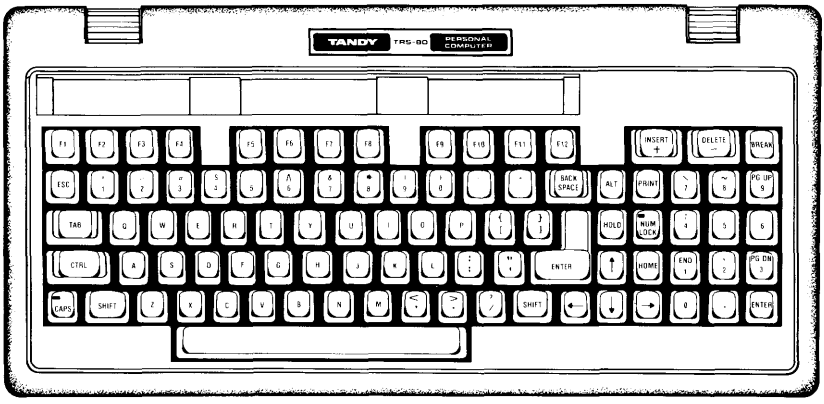


Figure 27
Tandy 1000 Keyboard

APPENDICES

The following sections contain reprints of manufacturer's documentation of components used in the Tandy 1000.

Tandy Corporation gratefully acknowledges permission by the following to reprint their copyrighted material in this manual.

Teac Corporation
3-7-3 Naka-Cho
Musashimo, Tokyo, Japan

IBM PC® and IBM PCjr™
P.O. Box 1328-W
Boac Raton, Florida 33432

Motorola Semiconductors
5005 E. McDowell Road
Phoenix, Arizona 85008

Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051

Texas Instruments
P.O. Box 1087
Richardson, Texas 75080

Comparative Tables for IBM PC and PCjr. Computers

	IBM PC	IBM PCjr	TANDY 1000
Ø Ø Ø Ø	8237A-5 DMA CONTROLLER		8237A-5 DMA CONTROLLER
1			
2			
3			
4			
5			
6			
7	(32 PORTS THRU ØØ1F)		
8			
9			
A			
B			
C			
D			
E			
Ø Ø Ø F	8237A-5 DMA CONTROLLER		8237A-5 DMA CONTROLLER
	A1Ø – A15 NOT DECODED CHIP SELECT FROM A5 – A9 AØ, A1, A2, A3 TO 1C A4 = X ADDRESS RANGE: ØØØØ – ØØ1F ASSIGNED ADDRESS: ØØØØ – ØØØF.	NO DMA FUNCTION AVAILABLE.	CHIP SELECT FROM A4 – A15 AØ, A1, A2, A3 TO 1C ASSIGNED ADDRESS: ØØØØ – ØØØF DMA FUNCTION OPTIONAL.

	IBM PC	IBM PCjr	TANDY 1000
0020	8259A INTERRUPT CONTROLLER	8259A INTERRUPT CONTROLLER	8259A INTERRUPT CONTROLLER
0021			
0022			
0023			
0024			
0025			
0026			
0027		8259A INTERRUPT CONTROLLER	8259A INTERRUPT CONTROLLER
0028			
0029			
002A			
002B	SAME AS 0020 – 0027		
002C			
002D			
002E			
002F	8259A INTERRUPT CONTROLLER		
	A10 – A15 NOT DECODED (X) CHIP SELECT FROM A9 – A5 A0 ⟶ I.C. A4, A3, A2, A1 = X ADDRESS RANGE = 020 – 03F ASSIGNED ADDRESS = 020, 021.	A10 – A15 NOT DECODED (X) A1, A2 = X A0 ⟶ I.C. ADDRESS RANGE = 020 – 027 ASSIGNED ADDRESS = 020, 021.	DECODE A3 – A15 (B) A0 ⟶ I.C. ASSIGNED ADDRESS: 0020 – 0021 (B).

	IBM PC	IBM PCjr	TANDY 1000
0 0 6 0	8255A-5 PPI	8255A-5 PPI	8255A-5 PPI
0 6 1			
0 6 2			
0 6 3			
0 6 4			
0 6 5			
0 6 6			
0 6 7		8255A-5 PPI	8255A-5 PPI
8			
9			
A			
B			
C			
D			
E			
0 0 6 F	8255A-5 PPI		
	A1Ø – A15 NOT DECODED (X) CHIP SELECT FROM A9 – A5 A1, AØ ⟶ I.C. A4, A3, A2 = X ADDRESS RANGE: Ø6Ø – Ø7F ASSIGNED ADDRESS: Ø6Ø – Ø63.	A1Ø – A15 NOT DECODED (X) CHIP SELECT FROM A9 – A3 A1, AØ ⟶ I.C. A2 = X ADDRESS RANGE: Ø6Ø – Ø67 ASSIGNED ADDRESS: Ø6Ø – Ø63.	A1, AØ ⟶ DECODED I.C. CHIP SELECT FROM A3 – A15 ASSIGNED ADDRESS: ØØ6Ø – ØØ63.

	IBM PC	IBM PCjr	TANDY 1000
0 0 4 0	8253-5 TIMER	8253-5 TIMER	8253-5 TIMER
0 4 1			
0 4 2			
0 4 3			
4			
5			
6			
7		8253-5 TIMER	8253-5 TIMER
8			
9			
A			
B	DUPLICATES 40 – 47		
C			
D			
E			
0 F	8253-5 TIMER		
	A10 – A15 NOT DECODED (X) CHIP SELECT FROM A9 – A5 A1 A0 ⟶ I.C. A4, A3, A2 = X ADDRESS RANGE: 040 – 05F ASSIGNED ADDRESS = 040 – 043.	A10 – A15 NOT DECODED CHIP SELECT FROM A9 – A3 A1 A0 ⟶ I.C. A2 = X ADDRESS RANGE: 040 – 047 ASSIGNED ADDRESS = 040 – 043.	DECODE A3 – A15 A0 ⟶ DECODE BY I.C. ASSIGNED ADDRESS: 0040 – 0043.

DATA	IBM PC 0060 – PORT A	IBM PCjr 0060 – PORT A	TANDY 1000 0060 – PORT A
BIT 0	KEYBOARD SCAN CODE / CONFIG SW1	RESERVED	KEYBOARD BIT 0 – LSB
BIT 1	2		1
BIT 2	3		2
BIT 3	4		3
BIT 4	5		4
BIT 5	6		5
BIT 6	7		6
BIT 7	KEYBOARD SCAN CODE / CONFIG SW8	RESERVED	KEYBOARD BIT 7 –MSB
	SEE IBM TECH REFERENCE		SEE 1000 KEYBOARD
	MANUAL 2.02 FOR DETAILS		SPECIFICATION FOR DETAILS

DATA	IBM PC 0061 – PORT B – READ OR WRITE	IBM PCjr 0061 – PORT B – READ OR WRITE	TANDY 1000 0061 – PORT B – READ OR WRITE
BIT 0	1 = 8253 GATE #2 ENABLED	SAME	SAME
BIT 1	SPEAKER DATA OUT	SAME	SAME
BIT 2	1 = ENABLE READING	1 = ALPHA (GRAPHICS)	NO FUNCTION
↓	CONFIG SW 13 THRU 16		
↓	(I/O CHAN. ROM SIZE) OR		
↓	0 = ENABLE READING		
↓	CONFIG SW 12 (@PC0 – PC3)		
BIT 3	1 = CASSETTE MOTOR OFF	SAME	NO FUNCTION
BIT 4	0 = ENABLE RAM PARITY	1 = DISABLE CASSETTE MTR RELAY, INTERNAL BEEPER	NOT USED
BIT 5	0 = ENABLE I/O CH PARITY	SPKR SW 0	SOUND CONTROL 0
BIT 6	0 = HOLD KEYBOARD CLK LOW	SPKR SW 1	SOUND CONTROL 1
BIT 7	0 = ENABLE KEYBOARD	1 = KEYBOARD CLEAR	1 = KEYBOARD CLEAR
↓	1 = CLEAR KEYBOARD AND		
↓	ENABLE CONFIG SW 1-8		

DATA	IBM PC 0062 – PORT C – READ ONLY	IBM PCjr 0062 – PORT C – READ ONLY	TANDY 1000 0062 – PORT C – READ/WRITE
BIT 0	CONFIG SW16 OR	1 = KEYBOARD LATCHED	(OUT) NOT USED
	CONFIG SW12		
	SEE PORT 0061, BIT 2		
BIT 1	CONFIG SW15	0 = INTERNAL MODEM INSTALLED	(OUT) MULTI-DATA
BIT 2	CONFIG SW14	0 = DISKETTE DRIVE INSTALLED	(OUT) MULTI-CLOCK
BIT 3	CONFIG SW13	0 = 64K RAM EXPANSION	(OUT) NOT USED
		INSTALLED	
BIT 4	CASSETTE DATA IN	SAME	(IN) NOT USED
BIT 5	8253 CUT #2	SAME	(IN) SAME
BIT 6	1 = I/O CH CK (PARITY ERROR)	KEYBOARD DATA	(IN) NOT USED
BIT 7	1 = RAM PARITY ERROR	KEYBOARD CABLE INSTALLED	(IN) NOT USED
	HARDWARE LOGIC ATTACHED IS FOR INPUT ONLY.		IN TANDY 1000 THE HARDWARE LOGIC IS CONFIGURED SO THAT PORT C IS SPLIT WITH INPUT: PC4 – PC7 OUTPUT: PC0 – PC3

	IBM PC	IBM PCjr	TANDY 1ØØØ
Ø Ø 8 Ø	DMA PAGE REG. (NOT USED)		DMA PAGE REG. (NOT USED)
1	(CH 2)		(CH 2)
2	(CH 3)		(CH 3)
3	(CH Ø, 1)		DMA PAGE REG. (CHØ, 1)
4	REPEATED THRU ØØ9F		
5			
6			
7			
8			
9			
A			
B			
C			
D			
E			
Ø Ø 8 F	DMA PAGE REG.		
	A1Ø – A15 NOT DECODED CHIP SELECT FROM A5 – A9 AØ, A1 TO 1C A2, A3, A4 = X ADDRESS RANGE: ØØ8Ø – ØØ9F ASSIGNED ADDRESS: ØØ8Ø – ØØ83.	NO DMA FUNCTION.	CHIP SELECT FROM A3 – A15 AØ, A1 TO 1C. DMA OPTIONAL ON TANDY 1ØØØ.

	IBM PC	IBM PCjr	TANDY 1ØØØ
Ø Ø A Ø	NMI MASK REGISTER	PORT AØ	NMI MASK REGISTER
1			
2			
3			
4			
5			
6			
7		PORT AØ	NMI MASK REGISTER
8			
9			
A			
B			
C			
D			
E			
Ø Ø A F	NMI MASK REGISTER		
	A1Ø – A15 NOT DECODED (X) CHIP SELECT FROM A9 – A5, 1ØW AØ – A4 = X ADDRESS RANGE: ØAØ – ØBF ASSIGNED ADDRESS: ØAØ.	A1Ø – A15 NOT DECODED CHIP SELECT FROM A9 – A3 AØ – A2 = X ADDRESS RANGE: ØAØ – ØA7 ASSIGNED ADDRESS: ØAØ.	A0, A1, A2 = X.

	IBM PC	IBM PCjr	TANDY 1000
Ø Ø C Ø	RESERVED	SOUND SN76496	SOUND SN76496
1			
2			
3			
4			
5			
6			
7		SOUND SN 76496	SOUND SN76496
8			
9			
A			
B			
C			
D			
E			
Ø Ø C F	RESERVED		
	NO FUNCTION.	WRITE ONLY FUNCTION. READ WILL CAUSE HANG-UP. WAIT REQUIRED ~ 42 STATES AØ – A2 = X.	CHIP SELECT DECODED FOR WRITE ONLY. WAIT REQUIRED ~ 42 STATES. AØ, A1, A2 = X.

	IBM PC	IBM PCjr	TANDY 1000
0200	GAME CONTROL ADAPTER	JOYSTICK	JOYSTICK
2 01			
2			
3			
4			
5			
6			
7		JOYSTICK	JOYSTICK
8			
9			
A			
B			
C			
D			
E	GAME CONTROL ADAPTER		
000F			
	A10 – A15 NOT DECODED (X) CHIP SELECT FROM A9 – A0 ADAPTER & DATA BUS DRIVER MUST BE INACTIVE WHEN AEN IS ACTIVE LOW FILES POSITION ONE-SHOTS.	A10 – A15 NOT DECODED (X) CHIP SELECT FROM A9 – A0 ADAPTER & DATA BUS DRIVER MUST BE INACTIVE WHEN AEN IS ACTIVE LOW FILES POSITION ONE-SHOTS.	A0, A1, A2 = X ASSIGNED ADDRESS: 0020 – 0021.

	IBM PC	IBM PCjr	TANDY 1000
Ø 3 7 Ø			
1			
2			
3			
4			
5			
6			
7			
8	PRINTER – DATA LATCH	PRINTER – DATA LATCH	PRINTER – DATA LATCH
9	– READ STATUS	– READ STATUS	– READ STATUS
A	– CONTROL LATCH	– CONTROL LATCH	– CONTROL LATCH
B	– NO FUNCTION	– NO FUNCTION	– NO FUNCTION
C	– DATA LATCH	– DATA LATCH	
D	– READ STATUS	– READ STATUS	
E	– CONTROL LATCH	– CONTROL LATCH	
Ø 3 7 F	PRINTER – NO FUNCTION	PRINTER – NO FUNCTION	PRINTER – NO FUNCTION
	A1Ø – A15 NOT DECODED (X) A2 = X AØ, A1 ⟶ I.C. ADDRESS RANGE: Ø37Ø – Ø37F ASSIGNED ADDRESS: DATA LATCH Ø378 STATUS Ø379 CONTROL LATCH Ø37A	A1Ø – A15 NOT DECODED (X) A2 = X AØ, A1 ⟶ I.C. ADDRESS RANGE: Ø37Ø – Ø37F ASSIGNED ADDRESS: DATA LATCH Ø378 STATUS Ø379 CONTROL LATCH Ø37A	AØ, A1 – DECODED BY PRINTER LOGIC A2 = X ASSIGNED ADDRESS: Ø378 – Ø37B

	PC MEMORY MAP	PCjr MEMORY MAP	TANDY 1ØØØ MEMORY MAP
Ø3DØ			
Ø3D1			
Ø3D2			
Ø3D3			
Ø3D4	6845 ADDRESS REGISTER	6845 ADDRESS REGISTER	6845 ADDRESS REGISTER
Ø3D5	6845 DATA REGISTER	6845 DATA REGISTER	6845 DATA REGISTER
Ø3D6			
Ø3D7			
Ø3D8	MODE SELECT REGISTER	NOT AVAILABLE	MODE SELECT REGISTER
Ø3D9	COLOR SELECT REGISTER	NOT AVAILABLE	COLOR SELECT REGISTER
Ø3DA	READ STATUS REGISTER	WRITE GATE ARRAY ADDRESS, DATA & READ STATUS	WRITE VIDEO ARRAY ADDRESS & READ STATUS
Ø3DB	CLEAR LIGHT PEN LATCH	CLEAR LIGHT PEN LATCH	CLEAR LIGHT PEN LATCH
Ø3DC	PRESET LIGHT PEN LATCH	PRESET LIGHT PEN LATCH	PRESET LIGHT PEN LATCH
Ø3DD			
Ø3DE			WRITE VIDEO ARRAY DATA
Ø3DF		CRT PROCESSOR PAGE REGISTER	CRT PROCESSOR PAGE REGISTER
SYSTEM TIMING	MEMORY READ = 1 WAIT I/O READ/WRITE = 1 WAIT	RAM READ/WRITE ≈ 6 WAITS ROM READ = Ø WAITS I/O READ/WRITE = 0 WAITS	RAM READ/WRITE ≈ 2 WAITS ROM READ = 0 WAITS I/O READ/WRITE = 1 WAITS

	IBM PC	IBM PCjr	TANDY 1000
Ø 3 F Ø	FDC, DOR REGISTER (WRITE ONLY)		DOR REGISTER
1			
2			
3	DOR REGISTER (WRITE ONLY)		DOR REGISTER (WRITE ONLY)
4	– STATUS (READ ONLY)		FDC – STATUS (READ ONLY)
5	FDC – DATA (R/W)		– DATA (R/W)
6			– STATUS (READ)
7			FDC – DATA (R/W)
8			
9			
A			
B			
C			
D			
E			
Ø 3 F F			
	FDC FUNCTION SELECT IS FROM A3 – A9. FDC AØ = AØ, FDC CSV = A1 SELECT FOR 'DOR' IS FDC FUNCTIONAL SELECT · A2 IBM SPECIFIES FDC – STATUS – 3F4 FDC – DATA – 3F5 DOR – 3F2	IBM PCjr FDC @ ØØFX	A1 = X DOR A2 = Ø FDC A2 = 1

VIDEO ARRAY ADDRESS (3DA)	PC MEMORY MAP 3DA		PCjr MEMORY MAP GATE ARRAY 3DA		TANDY 1000 MEMORY MAP VIDEO ARRAY 3DA & 3DE	
	READ	WRITE	READ	WRITE	READ (3DA)	WRITE (3DE)
00 BIT 0	DISPLAY INACTIVE	NOT USED	DISPLAY ENABLE	HIBW/LOBW	DISPLAY INACTIVE	NOT USED
00 BIT 1	LIGHT PEN SET	NOT USED	LIGHT PEN SET	GRAPHICS	LIGHT PEN SET	NOT USED
00 BIT 2	LIGHT SWITCH STATUS	NOT USED	LIGHT SWITCH STATUS	B/W	LIGHT SWITCH STATUS	NOT USED
00 BIT 3	VERTICAL RETRACE	NOT USED	VERTICAL RETRACE	VIDEO ENABLE	VERTICAL RETRACE	NOT USED
00 BIT 4	NOT USED	NOT USED	VIDEO DOTS	16 COLOR GRAPHICS	NOT USED	NOT USED
01 BIT 0		NOT USED		PALETTE MASK 0		PALETTE MASK 0
01 BIT 1		NOT USED		PALETTE MASK 1		PALETTE MASK 1
01 BIT 2		NOT USED		PALETTE MASK 2		PALETTE MASK 2
01 BIT 3		NOT USED		PALETTE MASK 3		PALETTE MASK 3
02 BIT 0		NOT USED		BORDER BLUE		BORDER BLUE
02 BIT 1		NOT USED		BORDER GREEN		BORDER GREEN
02 BIT 2		NOT USED		BORDER RED		BORDER RED
02 BIT 3		NOT USED		BORDER INTENSITY		BORDER INTENSITY
03 BIT 0		NOT USED		RESERVED = 0		NOT USED
03 BIT 1		NOT USED		ENABLE BLINK		NOT USED
03 BIT 2		NOT USED		RESERVED = 0		BORDER ENABLE
03 BIT 3		NOT USED		2 COLOR GRAPHICS		4 COLOR HIGH RES.
03 BIT 4		NOT USED		NOT USED		16 COLOR MODE
04 BIT 0		NOT USED		ASYNCHRON. RESET		NOT USED
04 BIT 1		NOT USED		SYNCHRONOUS RESET		NOT USED
10 – 1F BIT 0		NOT USED		PALETTE BLUE		PALETTE BLUE
10 – 1F BIT 1		NOT USED		PALETTE GREEN		PALETTE GREEN
10 – 1F BIT 2		NOT USED		PALETTE RED		PALETTE RED
10 – 1F BIT 3		NOT USED		PALETTE INTENSITY		PALETTE INTENSITY
	READS STATUS AT 3DA		READS STATUS AT 3DA AND SET ADDRESS/DATA FLIP-FLOP TO ADDRESS	WRITE ADDRESS AT 3DA WRITE DATA AT 3DA	READS STATUS AT 3DA	WRITE ADDRESS AT 3DA WRITE DATA AT 3DE

DATA	IBM PC 0081 – WRITE ONLY	IBM PCjr	TANDY 1000
BIT 0	DMA CH2 ADDRESS A16		
1	A17		
2	A18	SAME	SAME
3	DMA CH2 ADDRESS A19		
4	NO USE		
5			
6			
BIT 7	NO USE		
		DMA OPTIONAL ON PCjr	DMA OPTIONAL ON TANDY 1000.

DATA	IBM PC 0082 – WRITE ONLY	IBM PCjr	TANDY 1000
BIT 0	DMA CH3 ADDRESS A16		
1	A17		
2	A18	SAME	SAME
3	DMA CH3 ADDRESS A19		
4	NO USE		
5			
6			
BIT 7	NO USE		

DATA	IBM PC ØØ83 – WRITE ONLY	IBM PCjr	TANDY 1ØØØ
BIT Ø	DMA CHØ – 1 ADDRESS A16		
1	A17		
2	A18	SAME	SAME
3	DMA CHØ – 1 ADDRESS A19		
4	NO USE		
5			
6			
BIT 7	NO USE		

	PC MEMORY MAP	PCjr MEMORY MAP	TANDY 1ØØØ MEMORY MAP
3DF BIT Ø	NOT USED	CRT PAGE Ø	CRT PAGE Ø
3DF BIT 1	NOT USED	CRT PAGE 1	CRT PAGE 1
3DF BIT 2	NOT USED	CRT PAGE 2	CRT PAGE 2
3DF BIT 3	NOT USED	PROCESSOR PAGE 1	PROCESSOR PAGE 1
3DF BIT 4	NOT USED	PROCESSOR PAGE 2	PROCESSOR PAGE 2
3DF BIT 5	NOT USED	PROCESSOR PAGE 3	PROCESSOR PAGE 3
3DF BIT 6	NOT USED	VIDEO ADDRESS MODE Ø	VIDEO ADDRESS MODE Ø
3DF BIT 7	NOT USED	VIDEO ADDRESS MODE 1	VIDEO ADDRESS MODE 1

DATA	IBM PC 3F2 (WRITE ONLY)	IBM PCjr SAME	TANDY 1000 SAME
BIT 0	DRIVE SELECT 0*	DRIVE ENABLE	DRIVE SELECT 0*
BIT 1	DRIVE SELECT 1*	NOT USED	DRIVE SELECT 1*
BIT 2	0 = FDC RESET	NOT USED	0 = FDC RESET
BIT 3	1 = ENABLE INTERRUPT, DMA	NOT USED	1 = ENABLE DMA REQ/INTERRUPT
BIT 4	1 = DRIVE MOTOR #1 ON	NOT USED	1 = DRIVE 0 MOTOR ON
BIT 5	#2	WATCH DOG TIMER ENABLE	1 = DRIVE 1 MOTOR ON
BIT 6	#3	WATCH DOG TIMER TRIGGER	1 - FDC TERMINAL COUNT
BIT 7	1 = DRIVE MOTOR #4 ON	FDC RESET	NOT USED
			* TO SELECT DRIVE 0: BIT 0* · BIT 1* TO SELECT DRIVE 1: BIT 0 · BIT 1*

	PC MEMORY MAP	PCjr MEMORY MAP	TANDY 1ØØØ MEMORY MAP
3D8 BIT Ø	HIGH RESOLUTION CLOCK	NOT USED	HIGH RESOLUTION CLOCK
3D8 BIT 1	GRAPHICS SELECT	NOT USED	GRAPHICS SELECT
3D8 BIT 2	BLACK AND WHITE	NOT USED	BLACK AND WHITE
3D8 BIT 3	VIDEO ENABLE	NOT USED	VIDEO ENABLE
3D8 BIT 4	640 DOT GRAPHICS	NOT USED	640 DOT GRAPHICS
3D8 BIT 5	BLINK ENABLE	NOT USED	BLINK ENABLE
3D9 BIT Ø	BACKGROUND BLUE	NOT USED	BACKGROUND BLUE
3D9 BIT 1	BACKGROUND GREEN	NOT USED	BACKGROUND GREEN
3D9 BIT 2	BACKGROUND RED	NOT USED	BACKGROUND RED
3D9 BIT 3	BACKGROUND INTENSITY	NOT USED	BACKGROUND INTENSITY
3D9 BIT 4	FOREGROUND INTENSITY	NOT USED	FOREGROUND INTENSITY
3D9 BIT 5	COLOR SELECT	NOT USED	COLOR SELECT

DATA	IBM PC 037A (037E)	IBM PCjr 037A (037E)	TANDY 1000 037A (037E)
BIT 0	0 = STROBE	0 = STROBE	0 = STROBE
BIT 1	0 = AUTO FD XT	0 = AUTO FD XT	0 = AUTO FD XT
BIT 2	0 = INITIALIZE	0 = INITIALIZE	0 = INITIALIZE
BIT 3	0 = SELECT PRINTER	0 = SELECT PRINTER	0 = SELECT PRINTER
BIT 4	1 = ENABLE INTERRUPT	1 = ENABLE INTERRUPT	1 = ENABLE INTERRUPT
BIT 5	UNUSED	UNUSED	0 = ENABLE OUTPUT DATA
BIT 6	UNUSED	UNUSED	UNUSED
BIT 7	UNUSED	UNUSED	UNUSED

DATA	IBM PC 0378 (037C) RW	IBM PCjr 0378 (037C)	TANDY 1000 0378
BIT 0	DATA BIT 0 – LSB	DATA BIT 0 – LSB	DATA BIT 0 – LSB
BIT 1	DATA BIT 1 –	DATA BIT 1 –	DATA BIT 1 –
BIT 2	DATA BIT 2 –	DATA BIT 2 –	DATA BIT 2 –
BIT 3	DATA BIT 3 –	DATA BIT 3 –	DATA BIT 3 –
BIT 4	DATA BIT 4 –	DATA BIT 4 –	DATA BIT 4 –
BIT 5	DATA BIT 5 –	DATA BIT 5 –	DATA BIT 5 –
BIT 6	DATA BIT 6 –	DATA BIT 6 –	DATA BIT 6 –
BIT 7	DATA BIT 7 – MSB	DATA BIT 7 – MSB	DATA BIT 7 – MSB
	0379 (037D) READ ONLY	0379 (037D) READ ONLY	0379
BIT 0	UNUSED	UNUSED	UNUSED
BIT 1	UNUSED	UNUSED	UNUSED
BIT 2	UNUSED	UNUSED	UNUSED
BIT 3	0 = ERROR CONDITION	0 = ERROR	0 = ERROR
BIT 4	1 = PRINTER SELECTED	1 = PRINTER SELECTED	1 = PRINTER SELECTED
BIT 5	0 = END OF FORM	0 = END OF FORM	0 = END OF FORM
BIT 6	0 = ACKNOWLEDGE	0 = ACKNOWLEDGE	0 = ACKNOWLEDGE
BIT 7	0 = BUSY	0 = BUSY	0 = BUSY

DATA	IBM PC 0201 – READ	IBM PCjr 0201 – READ	TANDY 1000 0201 – READ
BIT 0	A – X POSITION	A – X POSITION	L – X POSITION
BIT 1	A – Y	A – Y	L – Y
BIT 2	B – X	B – X	R – X
BIT 3	B – Y	B – Y	R – Y
BIT 4	A BUTTON #1	A BUTTON #1	L BUTTON #1
BIT 5	A BUTTON #2	A BUTTON #2	L BUTTON #2
BIT 6	B BUTTON #1	B BUTTON #1	R BUTTON #1
BIT 7	B BUTTON #2	B BUTTON #2	R BUTTON #2
	WRITE TO PORT STARTS TIMING PERIOD. (ENABLES ONE SHOT MODE OF QUAD 555.) THEREFORE WRITE TO PORT 201 BEFORE INTEGRATING PORT ON JOYSTICK VALUES.		WRITE TO 0200 RESTARTS INTEGRATOR. THEREFORE WRITE TO 201 BEFORE INTEGRATING PORT IN JOYSTICK VALUES.

DATA	IBM PC ØØAØ – WRITE	IBM PCjr ØØAØ – ØØA7	TANDY 1ØØØ ØØAØ, ØØA1
BIT Ø	X	X	MEMCONFIG Ø
BIT 1			MEMCONFIG 1
BIT 2			MEMCONFIG 2
BIT 3		X	MEMCONFIG 3
BIT 4		1 = DISABLE – HRQ (BUS HOLD REQ)	X
BIT 5		1: TIMER CLK #2 = 1.1925 MHZ Ø:TIMER CLK #2 = CLK #1 OUT	X
BIT 6	X	1 = 1R TEST	X
BIT 7	1 = ENABLE NMI	1 = ENABLE NMI	1 = ENABLE NMI
	READ FROM ØØAØ – NO FUNCTION.	READ FROM ØØAØ – ØØA7 CLEARS NMI ENABLE NO DATA INVOLVED.	READ FROM ØØAØ, ØØA1 HAS NO FUNCTION. DEFINES ONE OF FIVE 128K MEMORY. SEE MEMORY PAGE MAP.

Printer Specifications

X = follows standard A = alternate ( ) EG = enable graphics DG = disable graphics
*n = special (see notes n)

Types	-CGP-	-LP (Dot Matrix)-			------DMP (Dot Matrix)------							DWP (Daisy Wheel)			Tandy	IBM
Model	220	V	VI	VIII	110	120	200	400	420	500	2100	II	210	410	Spec	Spec
26	1192	1165	1166	1168	1271	1255	1254	1251	1267	1252	1256	1158	1257	1250		
Code																
20																
21	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!
22	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
23	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#
24	$	$	$	$	$	$	$	$	$	$	$	$	$	$	$	$
25	%	%	%	%	%	%	%	%	%	%	%	%	%	%	%	%
26	&	&	&	&	&	&	&	&	&	&	&	&	&	&	&	&
27	'	'	'	'	'	'	'	'	'	'	'	'	'	'	'	'
28	(	(	(	(	(	(	(	(	(	(	(	(	(	(	(	(
29	)	)	)	)	)	)	)	)	)	)	)	)	)	)	)	)
2A	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
2B	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
2C	,	,	,	,	,	,	,	,	,	,	,	,	,	,	,	,
2D	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
2E	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
2F	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
31	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
32	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
33	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
34	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
35	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
36	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
37	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
38	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
39	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
3A	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
3B	;	;	;	;	;	;	;	;	;	;	;	;	;	;	;	;
3C	<	<	<	<	<	<	<	<	<	<	<	<	<	<	<	<
3D	=	=	=	=	=	=	=	=	=	=	=	=	=	=	=	=
3E	>	>	>	>	>	>	>	>	>	>	>	>	>	>	>	>
3F	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
40	@	@	@	@	@	@	@	@	@	@	@	@	@	@	@	@
41	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
42	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
43	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
44	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
45	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
46	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
47	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
48	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
4A	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J
4B	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K	K
4C	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
4D	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M
4E	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
4F	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O

X = follows standard A = alternate ( ) EG = enable graphics DG = disable graphics
*n = special (see notes n)

Types	-CGP-	-LP (Dot Matrix)-			------DMP (Dot Matrix)------							DWP (Daisy Wheel)			Tandy	IBM
Model	220	V	VI	VIII	110	120	200	400	420	500	2100	II	210	410	Spec	Spec
26	1192	1165	1166	1168	1271	1255	1254	1251	1267	1252	1256	1158	1257	1250		
Code																
50 P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
51 Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q	Q
52 R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
53 S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
54 T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T
55 U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
56 V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
57 W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
58 X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
59 Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
5A Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
5B [	X	X	X	X	X	X	X	X (↑)	X (↑)	X	X (↑)	X	X (↑)	X	X (↑)	X
5C \	X	X	X	X	X	X	X	X (↓)	X (↓)	X	X (↓)	X	X (↓)	X	X (↓)	X
5D]	X	X	X	X	X	X	X	X (←)	X (←)	X	X (←)	X	X (←)	X	X (←)	X
5E ^	X	A (↑)	A (↑)	X	X	X	X	X (→)	X (→)	X	X (→)	X	X (→)	X	X (→)	X
5F _	X	A (←)	A (←)	X	X	X	X	X	X	X	X	X	X	X	X	X
60 `	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
61 a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a
62 b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b
63 c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
64 d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d	d
65 e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e	e
66 f	f	f	f	f	f	f	f	f	f	f	f	f	f	f	f	f
67 g	g	g	g	g	g	g	g	g	g	g	g	g	g	g	g	g
68 h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h
69 i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i
6A j	j	j	j	j	j	j	j	j	j	j	j	j	j	j	j	j
6B k	k	k	k	k	k	k	k	k	k	k	k	k	k	k	k	k
6C l	l	l	l	l	l	l	l	l	l	l	l	l	l	l	l	l
6D m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m	m
6E n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n	n
6F o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
70 p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p	p
71 q	q	q	q	q	q	q	q	q	q	q	q	q	q	q	q	q
72 r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
73 s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s	s
74 t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t	t
75 u	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u	u
76 v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v
77 w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
78 x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
79 y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
7A z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z
7B {	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7C ¦	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7D }	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7E ~	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7F	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

X = follows standard A = alternate ( ) EG = enable graphics DG = disable graphics
*n = special (see notes n)

Types Model 26 Code	DMP 2100P 1274	DMP 430 1277	DMP 105 1276	DMP 130 1280	DWP 220 1278	TRP 100 1275	LMP 2150 1272	TANDY	IBM
8Ø									Ç
81									ü
82									é
83									â
84									ä
85									à
86									å
87									ç (BEL)
88									ê (BS)
89									ë (HT)
8A									è (LF)
8B									ï (VT)
8C									î (FF)
8D									ì (CR)
8E									Ä (SO)
8F									Å (SI)
9Ø									É
91									æ
92									Æ (1Ø)
93									ô
94									ö (EE)
95									ò
96									û
97									ù
98									ÿ (CAN)
99									Ö
9A									Ü
9B									¢
9C									£
9D									¥
9E									Pt
9F									ƒ
AØ '	X	X				X	X	X	á
A1 à	X	X	X	X		X	X	X	í
A2 ç	X	X	X	X		X	X	X	ó
A3 £	X	X	X	X	X	X	X	X	ú
A4 `	X	X	X	X		X	X	X	ñ
A5 µ	X	X	X	X		X	X	X	Ñ
A6 ◦	X	X	X	X		X	X	X	a
A7 ▼	X	X	X	X		X	X		o
A8 †		X	X	X		X	X	X	¿
A9 §		X	X	X		X	X	X	⌐
AA ®	X	X	X	X		X	X	X	¬
AB ©	X	X	X	X		X	X	X	½
AC ¼	X	X	X	X		X	X	X	¼
AD ¾	X	X	X	X		X	X	X	¡
AE ½	X	X	X	X	X	X	X	X	«
AF ¶	X	X	X	X		X	X	X	»

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Types Model 26 Code	DMP 2100P 1274	DMP 430 1277	DMP 105 1276	DMP 130 1280	DWP 220 1278	TRP 100 1275	LMP 2150 1272	TANDY	IBM
BØ ¥	X	X	X	X		X	X	X	
B1 Ä	X	X	X	X		X	X	X	
B2 Ö	X	X	X	X		X	X	X	
B3 Ü	X	X	X	X		X	X	X	
B4 ¢	X	X	X	X		X	X	X	┤
B5 ~	X	X	X	X		X	X	X	╡
B6 ä	X	X	X	X		X	X	X	╢
B7 ö	X	X	X	X		X	X	X	╖
B8 ü	X	X	X	X		X	X	X	╕
B9 ß	X	X	X	X		X	X	X	╣
BA Tm	X	X	X	X		X	X	X	║
BB è	X	X	X	X		X	X	X	╗
BC ù	X	X	X	X		X	X	X	╝
BD ë	X	X	X	X		X	X	X	╜
BE "	X	X	X	X		X	X	X	╛
BF ƒ	X	X	X	X		X	X	X	┐
CØ â	X	X		X		X		X	└
C1 ê	X	X		X		X		X	┴
C2 î	X	X		X		X		X	┬
C3 ô	X	X		X		X		X	├
C4 û	X	X		X		X		X	─
C5 ^	X	X		X		X		X	┼
C6 ë	X	X		X		X		X	╞
C7 ï	X	X		X		X		X	╟
CB à	X	X		X		X		X	╚
C9 ì	X	X		X		X		X	╔
CA ò	X	X		X		X		X	╩
C8 ù	X	X		X		X		X	╦
CC ì	X			X		X		X	╠
CD ñ	X	X		X		X		X	═
CE ã	X	X		X		X		X	╬
CF õ	X	X		X		X		X	╧
DØ Æ	X	X		X		X		X	╨
D1 æ	X	X		X		X		X	╤
D2 Å	X	X		X		X		X	╥
D3 å	X	X		X		X		X	╙
D4 Φ	X	X		X		X		X	╘
D5 ϕ	X	X		X		X		X	╒
D6 Ñ	X	X		X		X		X	╓
D7 Ë	X	X		X		X		X	╫
D8 Ä	X	X		X		X		X	╪
D9 Ï	X	X		X		X		X	┘
DA Ö	X	X		X		X		X	┌
DB Ü	X	X		X		X		X	▪
DC ¿	X	X		X		X		X	▪
DD Ù	X	X		X		X		X	▪
DE Ë	X	X		X		X		X	▪
DF Ä	X	X		X		X		X	▪

X = follows standard A = alternate ( ) EG = enable graphics DG = disable graphics
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Types Model 26	DMP 2100P 1274	DMP 430 1277	DMP 105 1276	DMP 130 1280	DWP 220 1278	TRP 100 1275	LMP 2150 1272	TANDY	IBM
Code									
E0								X	α
E1 ▪	X	X	X	X		X	X	X	β
E2 ▪	X	X	X	X		X	X	X	Γ
E3 ▪	X	X	X	X		X	X	X	π
E4 ▪	X	X	X	X		X	X	X	Σ
E5 ▪	X	X	X	X		X	X	X	σ
E6 ▪	X	X	X	X		X	X	X	μ
E7 ▬	X	X	X	X		X	X	X	τ
E8 ▬	X	X	X	X		X	X	X	Φ
E9 ▮	X	X	X	X		X	X	X	Θ
EA ▮	X	X	X	X		X	X	X	Ω
EB ▛	X	X	X	X		X	X	X	δ
EC ▜	X	X	X	X		X	X	X	∞
ED ▙	X	X	X	X		X	X	X	Φ
EE ▟	X	X	X	X		X	X	X	∈
EF ■	X	X	X	X		X	X	X	∩
F0 ┌	X	X	X	X		X	X	X	≡
F1 ─	X	X	X	X		X	X	X	±
F2 ┐	X	X	X	X		X	X	X	≥
F3 ┬	X	X	X	X		X	X	X	≤
F4 ├	X	X	X	X		X	X	X	⌠
F5 │	X	X	X	X		X	X	X	⌡
F6 └	X	X	X	X		X	X	X	÷
F7 ┘	X	X	X	X		X	X	X	≈
F8 ┴	X	X	X	X		X	X	X	°
F9 ┤	X	X	X	X		X	X	X	∙
FA +	X	X	X	X		X	X	X	·
FB ◤	X	X	X	X		X	X	X	√
FC ◢	X	X	X	X		X	X	X	n
FD ◥	X	X	X	X		X	X	X	2
FE ◣	X	X	X	X		X	X	X	■
FF		X	X						

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Types Model 26 Code	DMP 2100P 1274	DMP 430 1277	DMP 105 1276	DMP 130 1280	DWP 220 1278	TRP 100 1275	LMP 2150 1272	TANDY	IBM
ØØ									
Ø1	NUL	NUL	NUL	NUL	NUL	NUL	NUL	NUL	NUL
Ø2									
Ø3									
Ø4									
Ø5									
Ø6									
Ø7				BEL				BEL	BEL
Ø8	BM			BM	BM		BS	BM	BS
Ø9						HT		LF	HT
ØA	LF	LF	LF	LF	LF	LF	LF	LF	LF
ØB									VT
ØC	FF	FF		FF		FF	FF	FF	FF
ØD	TR	CR	CR	CR	TR	CR	CR	TR	CR
ØE	EU	EU	EU	EU	EU	EU	EU	EU	SE
ØF	SU	SU	SU	SU	SU	SU	SU	SU	CM
1Ø									
11									
12	EG	EG	EG	EG		EG	EG	EG	1Ø
13	ED			ED			ED	ED	DS
14	EW	EW		EW			EW	EW	EE
15									
16									
17									
18									CAN
19		ED							
1A									
1B	AP	AP							
1C	RC	RC	RC	RC		RC	RC		
1D			BU						
1E	DG	DG	DG			DG	DG		
1F			BI						

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Types Model 26 Code	DMP 2100P 1274	DMP 430 1277	DMP 105 1276	DMP 130 1280	DWP 220 1278	TRP 100 1275	LMP 2150 1272	TANDY	IBM
1B 1-6	IM			IM	IM		IM		
1B 7	IM				IM			IM	BEL
1B 8	IM				IM			IM	BS
1B 9	IM				IM			IM	HT
1B A	FR	FR		SRF	FR			FR	LF
1B B									VT
1B C									FF
1B D									CR
1B E	SE	SE	SE	SE	CE	SE	SE	SE	SE
1B F	EE	EE	EE	EE	CN	EE	EE	EE	CM
1B 1Ø	HP	HP	HP	HP		HP	HP	HP	
1B 11	SP	SP		NLQ	SP			SP	
1B 12	CN	CN		NQP			CN	CN	1Ø
1B 13	1Ø	1Ø	1Ø	PF			1Ø	1Ø	
1B 14	16	16	16	16			16	16	EE
1B 15	CR	CR	CR	CR	CR		CR	CR	
1B 16	TR	TR	TR	TR	TR		TR	TR	
1B 17	12	12	12	EF			CM	12	
1B 18					XP			XP	CAN
1B 19					EX			EX	
1B 1A				48L	48L			48L	
1B 1C	HF	HF	HF	12L	HF	HF	12L	12L	12L
1B 1D	CE	CE		NQE				CE	
1B 1E	HR	HR		HR	HR		SSS	HR	HR
1B 1F	SB	SB	SB	SB	SB		SB	SB	
1B 2Ø	EB	EB	EB	EB	EB		EB	EB	
1B 21	MD	MD		MD				MD	RS
1B 22								RES	
1B 23								RES	
1B 24								RES	
1B 25								RES	
1B 26								RES	
1B 27								RES	
1B 28								RES	
1B 29								RES	
1B 2A								RES	
1B 2D									SEU
1B 2F		CP						CP	
1B 3Ø									BLF
1B 31								12Ø	72I
1B 32	12Ø	72L		72L		72L	DR	72L	ALF
1B 33				216				216	21n
1B 34	FL	FL		SPL		FL	FL	FL	TF
1B 35									TCR
1B 36	SF	SF	SF	6LF		SF	6LF	6LF	CS2
1B 37									CS1
1B 38	BLF	BLF	BLF	BLF	BLF	BLF	BLF	BLF	IP
1B 39		144		144				144	CIP
1B 3A	IB			CS2				IB	12
1B 3B	RS			MD				RS	
1B 3C									CR
1B 3D	CN							AØ	DCS
1B 3E	CE							A1	
1F 3F	SPF							AP	

X = follows standard A = alternate ( ) EG = enable graphics DG = disable graphics
*n = special (see notes n)

Types Model 26 Code	DMP 2100P 1274	DMP 430 1277	DMP 105 1276	DMP 130 1280	DWP 220 1278	TRP 100 1275	LMP 2150 1272	TANDY	IBM
1B 40		14n		14n				14n	
1B 41								RES	72N
1B 42		IOO		IOO				IC	SVT
1B 43								CS	FL
1B 44								RES	SHT
1B 45					SHT			SHT	SM
1B 46									EM
1B 47								7LF	SB
1B 48		PS		PS	PS			PS	EB
1B 49		HG						HG	FS
1B 4B								P1	6B
1D 4C								P2	12B
1B 4D		MF		MF				MF	
1B 4E								D11	PS
1B 4F									ES
1B 50								D43	Pn
1B 51		LM		LM				LM	
1B 52		RM		RM				RM	CT
1B 53		SS		SS	SS			SS	SS
1B 54								SC	EA
1B 55		BU		BU	BV			BU	BU
1B 57		DH						DH	SE
1B 58		EA		EA	EA			EA	Mn
1B 59				ISO				ISO	12G
1B 5A			72N					FE	24G
1B 5B			72S		72L			SF	
1B 5D									RLF
1B 5E									CC
1B 87									BEL
1B 88									BS
1B 89									HT
1B 8A									LF
1B 8B									VT
1B 8C									FF
1B 8D									CR
1B 8E									SO
1B 8F									SI
1B 92									10
1B 94									EE
1B 98									CAN

Symbol = description	# of bytes in control code
Ø5 = select Ø5 CPI monospaced characters	1
75 = select Ø7.5 CPI monospaced characters	2
1Ø = select 1Ø CPI monospaced characters	2
12 = select 12 CPI monospaced characters	2
16 = select (15, 16, 16.7) CPI monospaced characters (condensed)	2
6LF = full line feed (6 lines/inch or 1/6 inch line feed)	2
7LF = 4/5 line feed (7.5 lines/inch or 8/6Ø inch line feed)	2
BLF = 3/4 line feed (8 lines/inch or 1/8 inch line feed)	2
9L = 2/3 line feed (1/9 inch forward line feed)	2
1ØL = 3/5 line feed (1Ø lines/inch or 1/1Ø inch line feed)	2
12L = 1/2 line feed (12 lines/inch or 1/12 inch line feed)	2
36L = 1/6 line feed (36 lines/inch or 1/36 inch line feed)	2
48L = 1/8 line feed (48 lines/inch or 1/48 inch line feed)	2
72L = 1/12 line feed (72 lines/inch or 1/72 inch line feed)	2
72I = 7/12 line feed (7/72 inch line feed)	2
12Ø = 1/2Ø line feed (12Ø lines/inch or 1/12Ø inch line feed)	2
144 = 1/24 line feed (144 lines/inch or 1/144 inch line feed)	2
188 = 1/31 line feed (188 lines/inch or 1/188 inch line feed)	2
14n = n/24 line feed (144/n lines/inch or n/144 inch line feed)	3
18n = n/31 line feed (188/n lines/inch or n/188 inch line feed)	3
216 = 1/36 line feed (216 lines/inch or 1/216 inch line feed)	2
21n = n/36 line feed (216/n lines/inch or n/216 inch line feed)	3
72n = n/72 line feed (executes n/72 inch line feed)	3
72S = n/72 line feed (sets n/72 inch line feed, no motion)	3
6B = select 6Ø dots/inch bit image	4+n1n2
12B = select 12Ø dots/inch bit image	4+n1n2
12G = select 12Ø dots/inch graphics	4+n1n2
24G = select 24Ø dots/inch graphics	4+n1n2
AØ = font assignment for correspondence 1Ø CPI	3
A1 = font assignment for correspondence 12 CPI	3
AP = font assignment for proportional	3
ALF = line feed is set to ESC A (1B+41)	2
BEL = ring bell	1
BI = select bidirectional printing	1
BM = back space in microspaces	2
BS = back space 1 character width relative to current pitch	1
BU = bidirectional (n=Ø) -- unidirectional (n=1) carriage movement	3
CAN = clear print buffer and see manual for special conditions	1
CC = print control characters in Ø-2ØH range	2
CE = select correspondence 12 CPI character	2
CIP = cancel ignore paper end	2
CM = select compressed mode (1/2 current pitch selection)	1
CN = select correspondence 1Ø CPI character	2
CP = select compressed proportional character	2
CR = carriage return w/o line feed	1
CS = color-scan mode	2
CS1 = select character set #1	2
CS2 = select character set #2	2
CT = cancel tabs to default settings	2

continued on next page

Symbol = description	# of bytes in control code
D11 = define dot interval ratio (1:1)	2
D43 = define dot interval ratio (4:3)	2
DCS = download character set	3
DG = disable graphics	1
DH = double height	2
DR = advance paper one dot row	2
DS = de select printer (serial = X off)	1
EA = end superscript, subscript or double height	2
EB = end bold print	2
ED = enable data processing mode	1
EE = end of chracter elongation	2
EF = select standard elite 12 CPI characters	2
EG = enable graphics	1
EM = end emphasized (horizontal double strike)	2
ES = end skip perforation	2
ET = end 16 CPI (condensed) character mode	2
EU = end underline	1
EW = enable word processing mode	1
EX = exit external program mode	2
FE = forward linefeed execute	2
FF = form feed	1
FL = set form feed length	3
FR = full reverse line feed	2
FS = font select n=1 high speed n=2 middle font n=3 letter qual.	3
HF = half line-feed forward (no motion)	2
HG = transfers high-res graphic data	4+1(N1N2)
HP = moves the print head to a position specified	4
HR = half line feed reverse	2
HT = horizontal tab	1
IB = select IBM character set	2
IC = italic cursive character	2
IM = increment microspaces (proportional spacing)	2
IOO = italic on/off	3
IP = ignore paper end	2
ISO = selects ISO character sets n=country	3
LF = full forward line feed	1
LM = left margin set	3
MF = micro font	2
Mn = set horizontal margin	4
MD = toggles between Tandy and IBM modes	2
NLQ = near letter quality – proportional font	2
NQE = near letter quality – elite font	2
NQP = near letter quality – pica font	2
NUL = terminator	1
P1 = insert new paper in hopper #1	2
P2 = insert new paper in hopper #2	2
PF = select standard pica 10 CPI characters	2
PN = proportional spacing on/off	3
PS = set perforations skip	3

continued on next page

Symbol = description	# of bytes in control code
RC = repetitions of character	3
RES = reserved	∅
RLF = reverse line feed	2
RM = right margin set	3
RS = Tandy character set	2
SB = start bold	2
SC = select color	2
SCR = select CR=CR only	2
SE = start of character elongation	2
SEU = n=1 start underline n=∅ end underline	3
SF = set forward linefeed	2
SHT = set horizontal tab	2+list (terminal=∅)
SM = select emphasized (horizontal double strike)	2
SNL = select CR=CR+LF	2
SP = select proportional characters	2
SPF = select proportional font	3
SPL = sets page length	3
SRF = set reverse line feed	2
SS = superscript (n=∅) – subscript (n=1) character	3
SSS = selects superscript under the condition specified in the owners manual	2
SU = start underline	1
SVT = set vertical tab	2+list (terminal=∅)
TCR = n=∅ CR only n=1 CR + LF	3
TER = terminator of tab list	1
TF = top of form	2
TR = Tandy carriage return (CR + LF)	2
VT = vertical tab	1
XP = enter external program mode	2

intel®

PRELIMINARY

iAPX 88/10
8-BIT HMOS MICROPROCESSOR
8088/8088-2

- 8-Bit Data Bus Interface
- 16-Bit Internal Architecture
- Direct Addressing Capability to 1 Mbyte of Memory
- Direct Software Compatibility with iAPX 86/10 (8086 CPU)
- 14-Word by 16-Bit Register Set with Symmetrical Operations
- 24 Operand Addressing Modes
- Byte, Word, and Block Operations
- 8-Bit and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal, Including Multiply and Divide
- Compatible with 8155-2, 8755A-2 and 8185-2 Multiplexed Peripherals
- Two Clock Rates:
  5 MHz for 8088
  8 MHz for 8088-2

The Intel® iAPX 88/10 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It is directly compatible with iAPX 86/10 software and 8080/8085 hardware and peripherals.

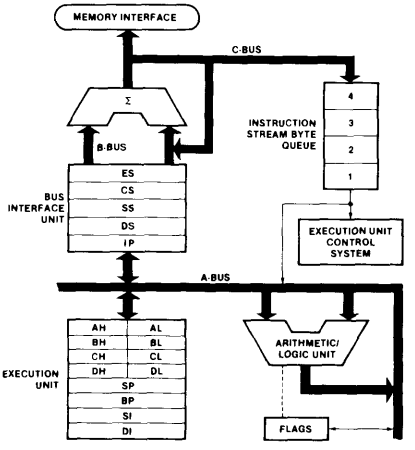


Figure 1. iAPX 88/10 CPU Functional Block Diagram

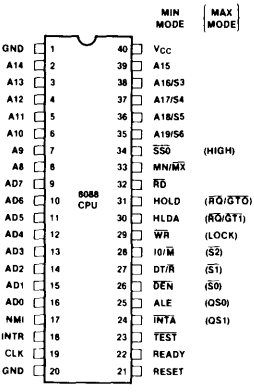


Figure 2. iAPX 88/10 Pin Configuration

NOVEMBER 1981
ORDER NUMBER: 210298-001

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . – 65°C to + 150°C
Voltage on Any Pin with
Respect to Ground . . . . . – 1.0 to + 7V
Power Dissipation . . . . . 2.5 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

(8088: T_A = 0°C to 70°C, V_{CC} = 5V ±10%)
(8088-2: T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current: 8088 8088-2		340 350	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC}+1.0	V	
C_{IN}	Capacitance if Input Buffer (All input except AD_0-AD_7, RQ/GT		15	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD_0-AD_7, RQ/GT		15	pF	fc = 1 MHz

A.C. CHARACTERISTICS

(8088: T_A = 0°C to 70°C, V_{CC} = 5V ±10%)
(8088-2: T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

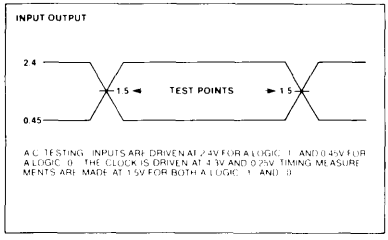
		8088		8088-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	(⅔ TCLCL) − 15		(⅔ TCLCL) − 15		ns	
TCHCL	CLK High Time	(⅓ TCLCL) + 2		(⅓ TCLCL) + 2		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 8088	(⅔ TCLCL) − 15		(⅔ TCLCL) − 15		ns	
TCHRYX	READY Hold Time into 8088	30		20		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	−8		−8		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

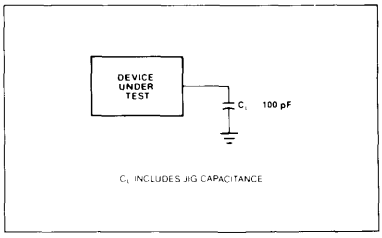
		8088		8088-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH-20		TCLCH-10		ns	
TCLLH	ALE Active Delay		80		50	ns	
TCHLL	ALE Inactive Delay		85		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		TCHCL-10		ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	C_L = 20-100 pF for all 8088 Outputs in addition to internal loads
TCHDX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time After $\overline{WR}$	TCLCH-30		TCLCH-30		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-45		TCLCL-40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL-75		2TCLCL-50		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL-60		2TCLCL-40		ns	
TAVAL	Address Valid to ALE Low	TCLCH-60		TCLCH-40		ns	
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". THE CLOCK IS DRIVEN AT 4.3V AND 0.25V. TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0".

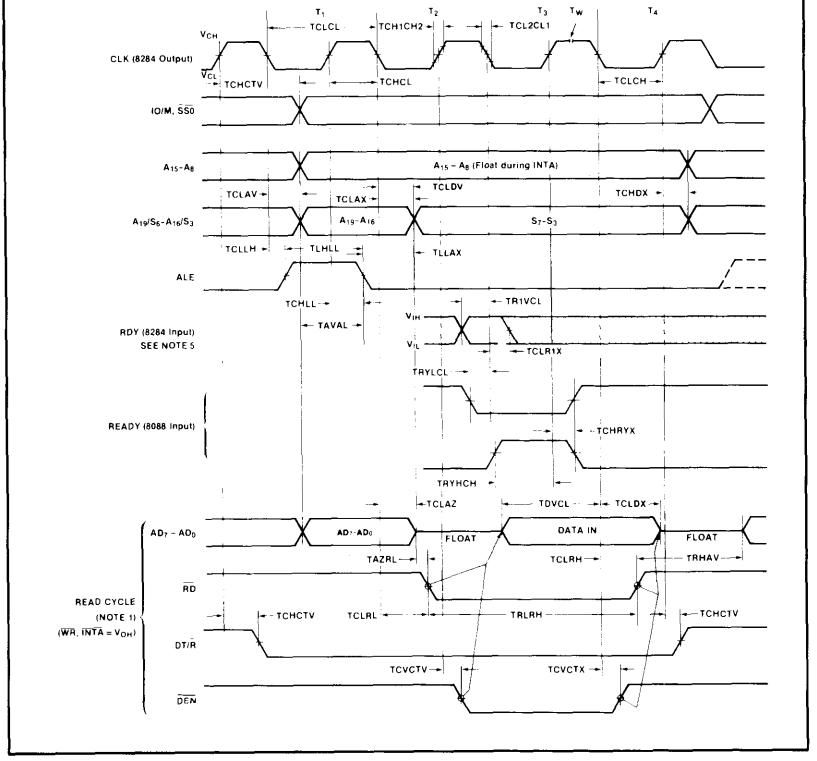
A.C. TESTING LOAD CIRCUIT



C_L INCLUDES JIG CAPACITANCE

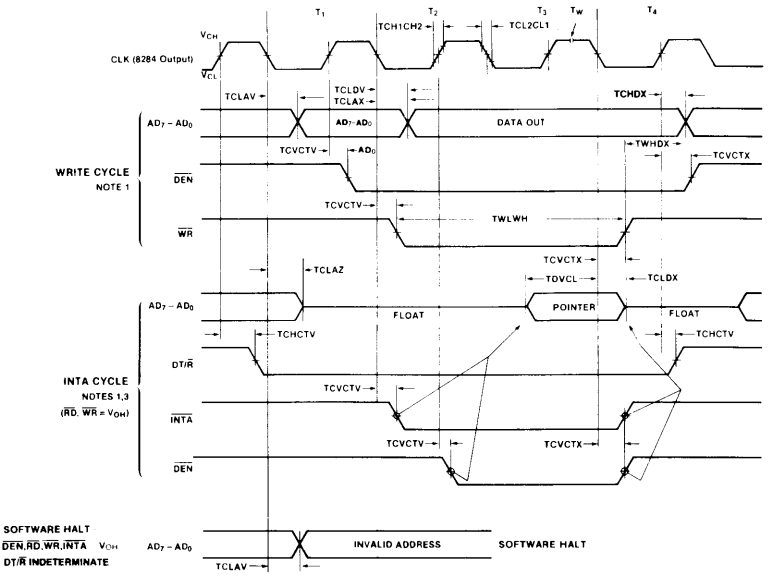
WAVEFORMS

BUS TIMING—MINIMUM MODE SYSTEM



WAVEFORMS (Continued)

BUS TIMING—MINIMUM MODE SYSTEM (Continued)



NOTES:
1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL SIGNALS ARE SHOWN FOR THE SECOND INTA CYCLE.
4. SIGNALS AT 8284 ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

A.C. CHARACTERISTICS

MAX MODE SYSTEM (USING 8288 BUS CONTROLLER)

TIMING REQUIREMENTS

		8088		8088-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	(2/3 TCLCL) − 15		(2/3 TCLCL) − 15		ns	
TCHCL	CLK High Time	(1/3 TCLCL) + 2		(1/3 TCLCL) + 2		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data In Setup Time	30		20		ns	
TCLDX	Data In Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 8088	(2/3 TCLCL) − 15		(2/3 TCLCL) − 15		ns	
TCHRYX	READY Hold Time into 8088	30		20		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	−8		−8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) (See Note 2)	30		15		ns	
TGVCH	RQ/GT Setup Time	30		15		ns	
TCHGX	RQ Hold Time into 8086	40		30		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

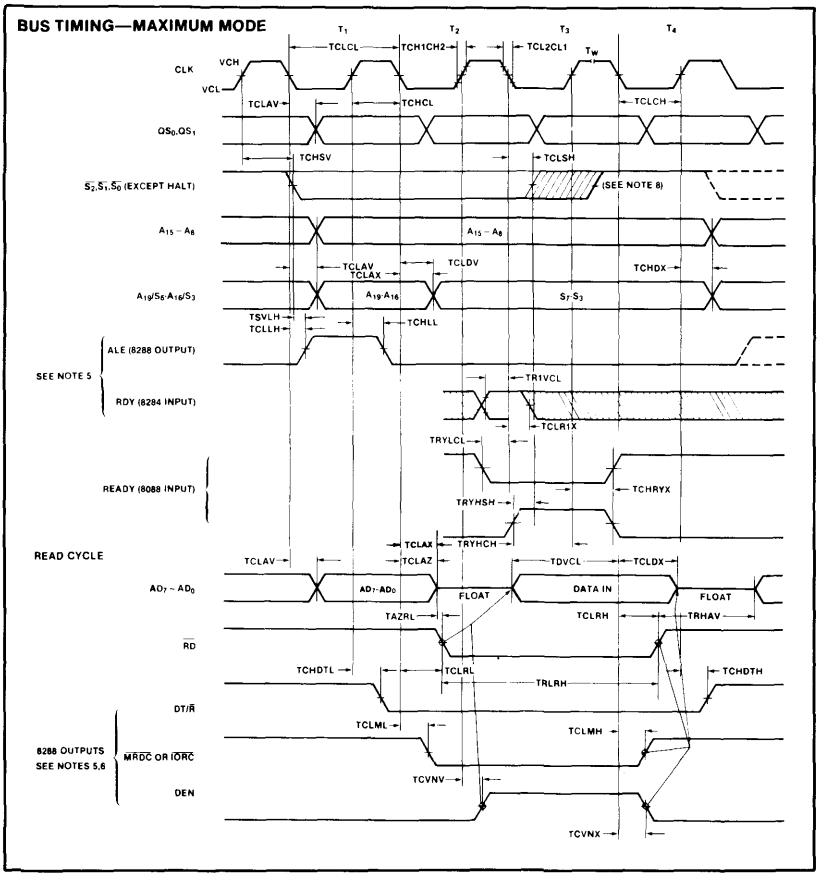
NOTES:
1. Signal at 8284 or 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3 state).
4. Applies only to T2 state (8 ns into T3 state).

A.C. CHARACTERISTICS

TIMING RESPONSES

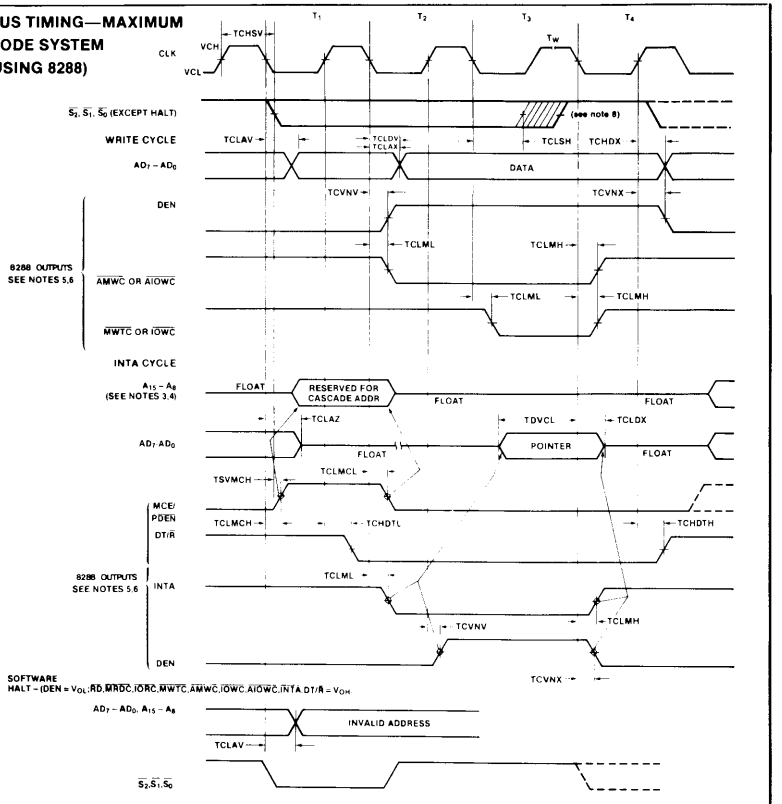
		8088		8088-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLML	Command Active Delay (See Note 1)	10	35	10	35	ns	
TCLMH	Command Inactive Delay (See Note 1)	10	35	10	35	ns	
TRYHSH	READY Active to Status Passive (See Note 3)		110		65	ns	
TCHSV	Status Active Delay	10	110	10	60	ns	
TCLSH	Status Inactive Delay	10	130	10	70	ns	
TCLAV	Address Valid Delay	10	110	10	60	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15		15	ns	
TSVMCH	Status Valid to MCE High (See Note 1)		15		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15		15	ns	
TCLMCH	CLK Low to MCE High (See Note 1)		15		15	ns	
TCHLL	ALE Inactive Delay (See Note 1)		15		15	ns	
TCLMCL	MCE Inactive Delay (See Note 1)		15		15	ns	C_L = 20-100 pF for all 8088 Outputs in addition to internal loads
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		ns	
TCLRL	RD Active Delay	10	165	10	100	ns	
TCLRH	RD Inactive Delay	10	150	10	80	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL-45		TCLCL-40		ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30		30	ns	
TCLGL	GT Active Delay		110		50	ns	
TCLGH	GT Inactive Delay		85		50	ns	
TRLRH	RD Width	2TCLCL-75		2TCLCL-50		ns	
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

WAVEFORMS


BUS TIMING—MAXIMUM MODE
T1
T2
T3
T4
TCLCL
TCH1CH2
TCL2CL1
TW
CLK
VCH
VCL
TCLAV
TCHCL
TCLCH
QS0,QS1
TCHSV
TCLSH
S2,S1,S0 (EXCEPT HALT)
(SEE NOTE 8)
A15 - A8
TCLAV
TCLAX
TCLDV
TCHDX
A19/S6-A16/S3
A19-A16
S7-S3
TSVLH
TCLLH
TCHLL
ALE (8288 OUTPUT)
SEE NOTE 5
RDY (8284 INPUT)
TR1VCL
TCLR1X
TRYLCL
READY (8088 INPUT)
TCHRYX
TRYHSH
TRYHCH
TCLAX
READ CYCLE
TCLAV
TCLAZ
TDVCL
TCLDX
AD7 - AD0
AD7-AD0
FLOAT
DATA IN
FLOAT
TAZRL
TCLRH
TRHAV
RD
TCHDTL
TCLRL
TRLRH
TCHDTH
DT/R
TCLML
TCLMH
8288 OUTPUTS
SEE NOTES 5,6
MRDC OR IORC
DEN
TCVNV
TCVNX

WAVEFORMS (Continued)

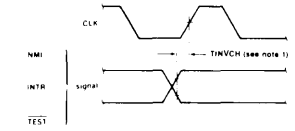
BUS TIMING—MAXIMUM MODE SYSTEM (USING 8288)



NOTES:
1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. CASCADE ADDRESS IS VALID BETWEEN FIRST AND SECOND INTA CYCLES.
4. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL FOR POINTER ADDRESS IS SHOWN FOR SECOND INTA CYCLE.
5. SIGNALS AT 8284 OR 8288 ARE SHOWN FOR REFERENCE ONLY.
6. THE ISSUANCE OF THE 8288 COMMAND AND CONTROL SIGNALS (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA AND DEN) LAGS THE ACTIVE HIGH 8288 CEN.
7. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.
8. **STATUS INACTIVE IN STATE JUST PRIOR TO T_4.**

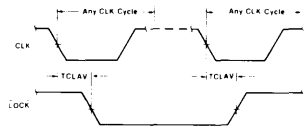
WAVEFORMS (Continued)

ASYNCHRONOUS SIGNAL RECOGNITION

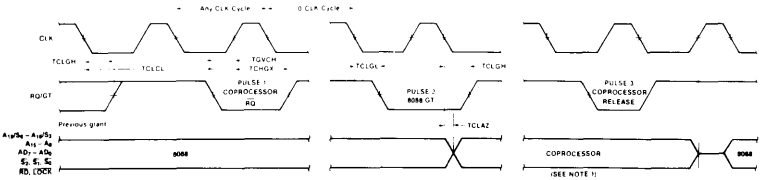


NOTE: 1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK

BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

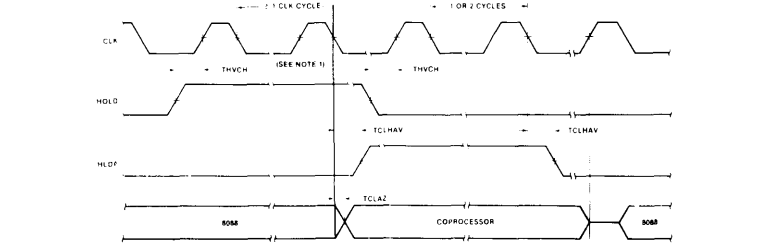


REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTE: 1. THE COPROCESSOR MAY NOT DRIVE THE BUSSES OUTSIDE THE REGION SHOWN WITHOUT RISKING CONTENTION.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, California 95051

Printed in U.S.A./T-3054/40K/1281/JC JL

intel®

8253/8253-5
PROGRAMMABLE INTERVAL TIMER

- **MCS-85™ Compatible 8253-5**
- **3 Independent 16-Bit Counters**
- **DC to 2 MHz**
- **Programmable Counter Modes**
- **Count Binary or BCD**
- **Single +5V Supply**
- **Available in EXPRESS**
  —Standard Temperature Range
  —Extended Temperature Range

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

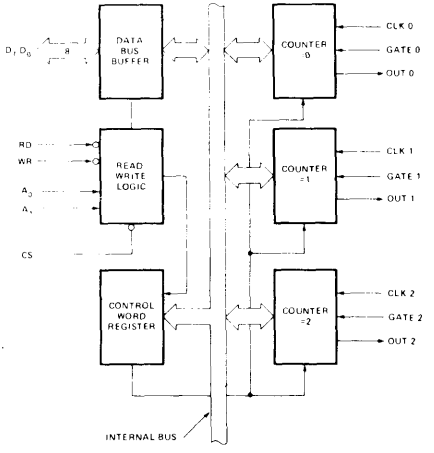


Figure 1. Block Diagram

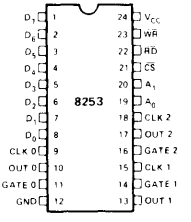


Figure 2. Pin Configuration

AFN-00745C

FUNCTIONAL DESCRIPTION

General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

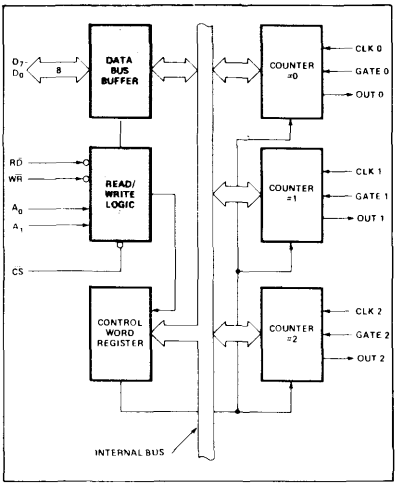


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

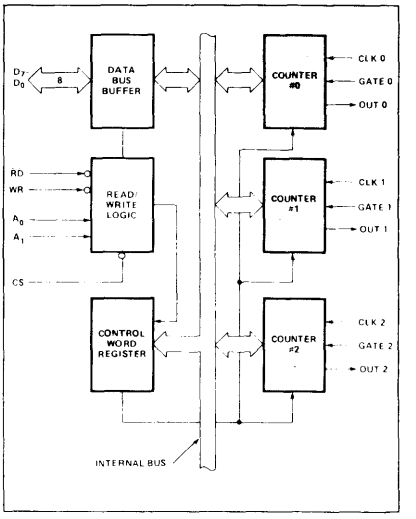


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.

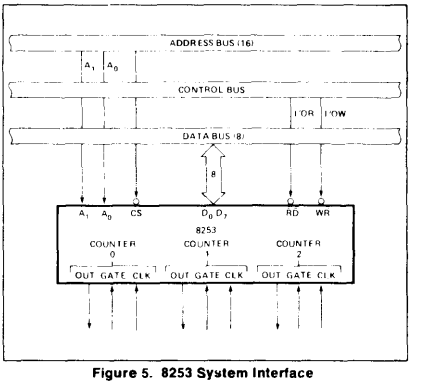


Figure 5. 8253 System Interface

OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. Prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register (A0, A1 = 11).

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL — Read/Load:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE Definition

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.
(2) Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for $(N+1)/2$ counts and low for $(N-1)/2$ counts.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

Modes \ Signal Status	Low Or Going Low	Rising	High
0	Disables counting	— —	Enables counting
1	— —	1) Initiates counting 2) Resets output after next clock	— —
2	1) Disables counting 2) Sets output immediately high	1) Reloads counter 2) Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	— —	Enables counting
5	— —	Initiates counting	— —

Figure 6. Gate Pin Operations Summary

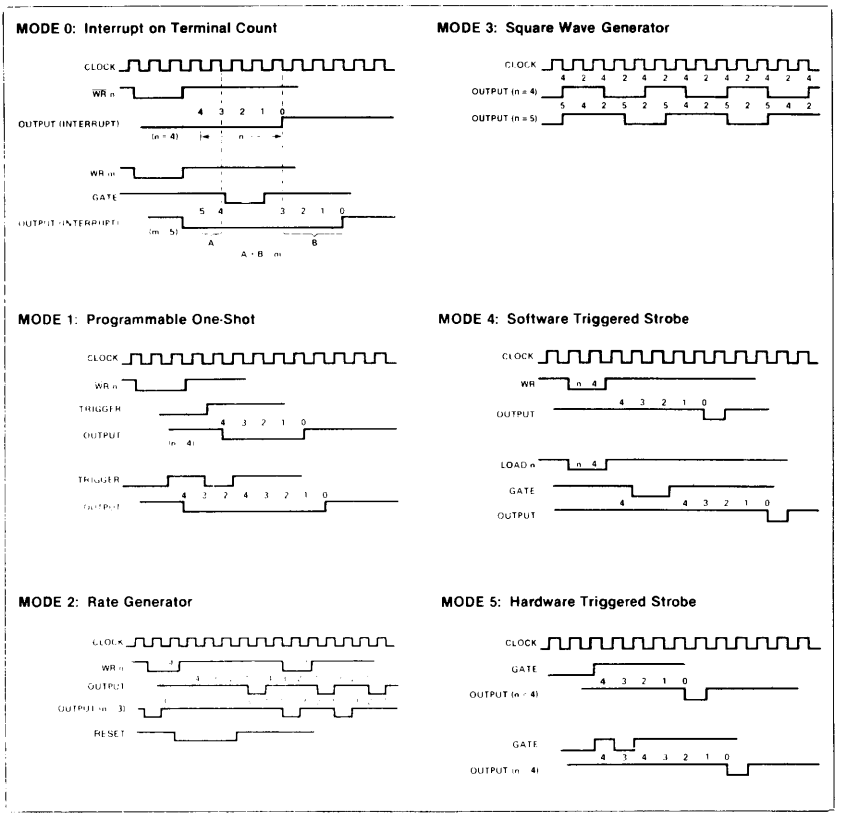


Figure 7. 8253 Timing Diagrams

8253 READ/WRITE PROCEDURE

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 8. Programming Format

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 9. Alternate Programming Formats

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple *I/O read operations of the selected* counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The *programmer then issues a normal read command to the* selected counter and the contents of the latched register is available.

MODE Register for Latching Count

A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1,SC0 — specify counter to be latched

D5,D4 — 00 designates counter latching operation

X — don't care

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.

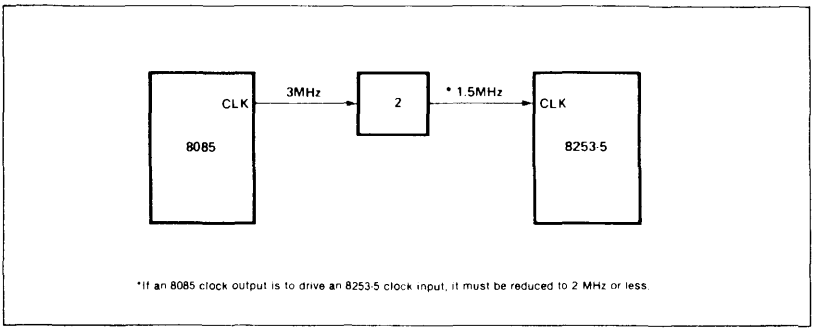


Figure 10. MCS-85™ Clock Interface*

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	0.5 V to +7 V
Power Dissipation	1 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±10%) *

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}+.5V	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to .45V
I_{CC}	V_{CC} Supply Current		140	mA	

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%, GND = 0V) *

Bus Parameters (Note 3)

READ CYCLE

Symbol	Parameter	8253		8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before $\overline{READ}$	50		30		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
t_{RD}	Data Delay From $\overline{READ}$ [4]		300		200	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns
t_{RV}	Recovery Time Between READ and Any Other Control Signal	1		1		μs

intel 8253/8253-5

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	8253		8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before $\overline{WRITE}$	50		30		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		250		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
t_{RV}	Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs

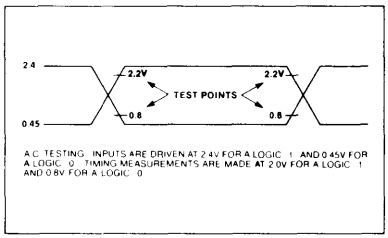
CLOCK AND GATE TIMING

Symbol	Parameter	8253		8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{CLK}	Clock Period	380	dc	380	dc	ns
t_{PWH}	High Pulse Width	230		230		ns
t_{PWL}	Low Pulse Width	150		150		ns
t_{GW}	Gate Width High	150		150		ns
t_{GL}	Gate Width Low	100		100		ns
t_{GS}	Gate Set Up Time to CLK↑	100		100		ns
t_{GH}	Gate Hold Time After CLK↑	50		50		ns
t_{OD}	Output Delay From CLK↓[4]		400		400	ns
t_{ODG}	Output Delay From Gate↓[4]		300		300	ns
t_{WC}	Write to CLK Set Up	450		350		

NOTES:
1. I_{OL} = 2.2 mA.
2. I_{OH} = −400 μA.
3. AC timings measured at V_{OH} 2.2, V_{OL} = 0.8.
4. C_L = 150pF.

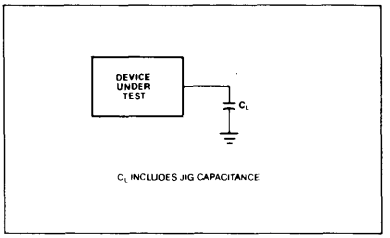
* For Extended Temperature EXPRESS, use M8253 electrical parameters.

A.C. TESTING INPUT, OUTPUT WAVEFORM



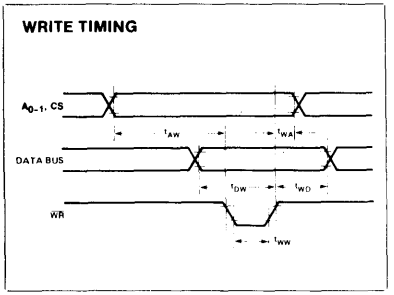
A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

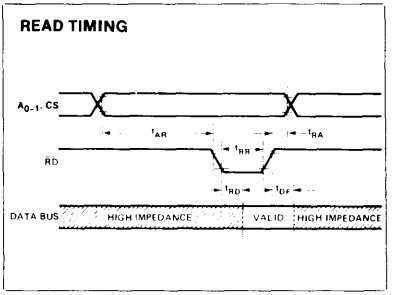
A.C. TESTING LOAD CIRCUIT

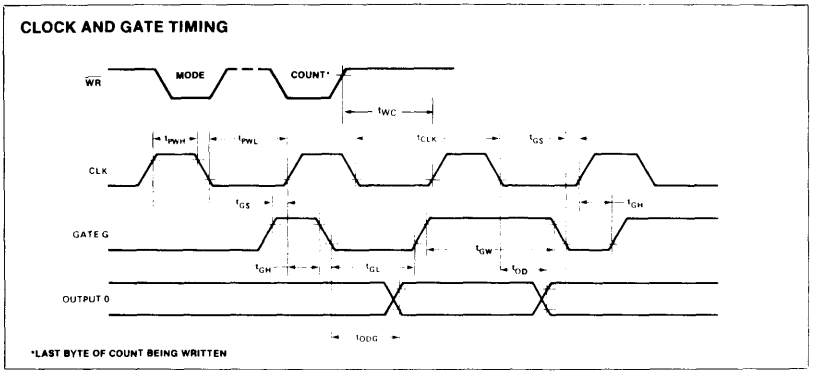


C_L INCLUDES JIG CAPACITANCE

WAVEFORMS


WRITE TIMING
A_{0-1}, CS
DATA BUS
$\overline{WR}$
t_{AW}
t_{WA}
t_{DW}
t_{WD}
t_{WW}


READ TIMING
A_{0-1}, CS
$\overline{RD}$
DATA BUS
HIGH IMPEDANCE
VALID
HIGH IMPEDANCE
t_{AR}
t_{RA}
t_{RR}
t_{RD}
t_{DF}


CLOCK AND GATE TIMING
$\overline{WR}$
MODE
COUNT*
t_{WC}
t_{PWH}
t_{PWL}
t_{CLK}
t_{GS}
CLK
t_{GH}
GATE G
t_{GW}
t_{GL}
t_{OD}
OUTPUT 0
t_{ODG}
*LAST BYTE OF COUNT BEING WRITTEN

intel

8259A/8259A-2/8259A-8
PROGRAMMABLE INTERRUPT CONTROLLER

- **iAPX 86, iAPX 88 Compatible**
- **MCS-80®, MCS-85® Compatible**
- **Eight-Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **28-Pin Dual-In-Line Package**
- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**

The Intel® 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel® 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).

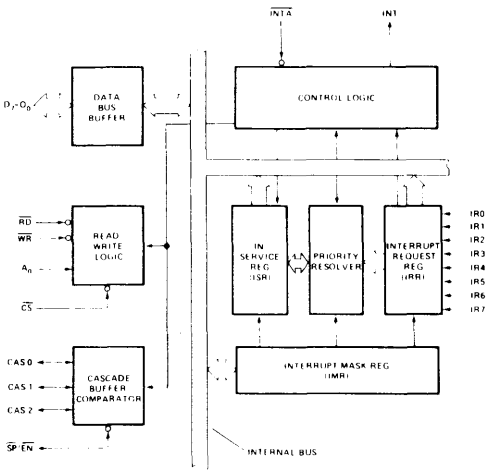


Figure 1. Block Diagram

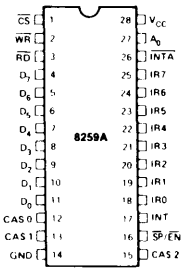


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	28	I	**Supply:** +5V Supply.
GND	14	I	**Ground.**
$\overline{CS}$	1	I	**Chip Select:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 8259A. INTA functions are independent of CS.
$\overline{WR}$	2	O	**Write:** A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**Read:** A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.
D_7-D_0	4-11	I/O	**Bidirectional Data Bus:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0-CAS_2	12, 13, 15	I/O	**Cascade Lines:** The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**Slave Program/Enable Buffer:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**Interrupt:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0-IR_7	18-25	I	**Interrupt Requests:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**Interrupt Acknowledge:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**A0 Address Line:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for iAPX 86, 88).

FUNCTIONAL DESCRIPTION

Interrupts in Microcomputer Systems

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

The 8259A

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

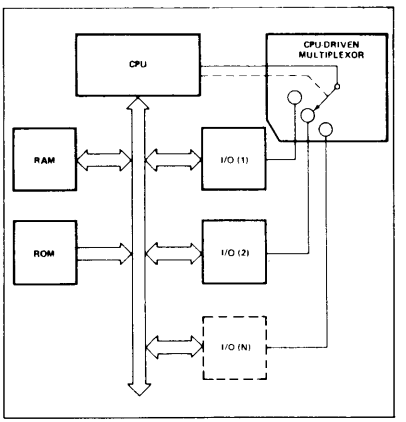


Figure 3a. Polled Method

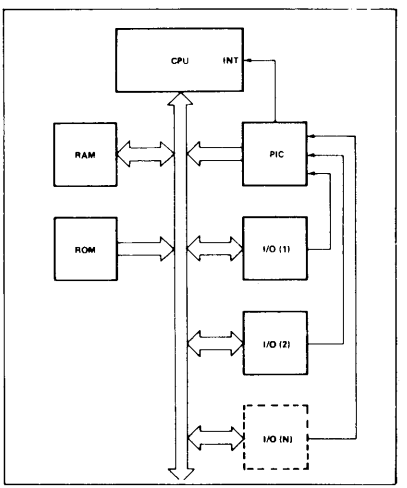


Figure 3b. Interrupt Method

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

$\overline{INTA}$ (INTERRUPT ACKNOWLEDGE)

$\overline{INTA}$ pulses will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 8259A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

$\overline{CS}$ (CHIP SELECT)

A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (WRITE)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

$\overline{RD}$ (READ)

A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

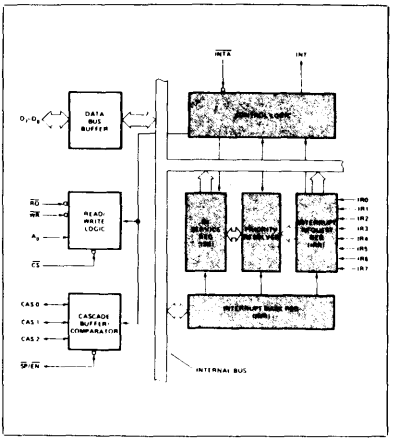


Figure 4a. 8259A Block Diagram

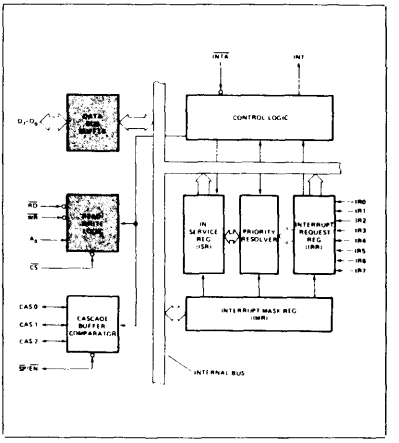


Figure 4b. 8259A Block Diagram

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 8259A".)

INTERRUPT SEQUENCE

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the 8259A from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. *The lower 8-bit address is released at the first* $\overline{INTA}$ pulse and and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an iAPX 86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive the Data Bus during this cycle.
5. The iAPX 86,10 will initiate a second $\overline{INTA}$ pulse. During this pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (*i.e., the request was too short in duration*) the 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

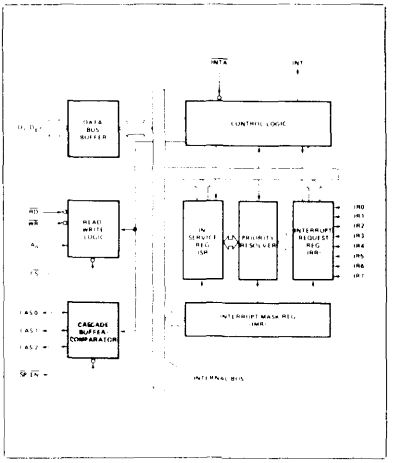


Figure 4c. 8259A Block Diagram

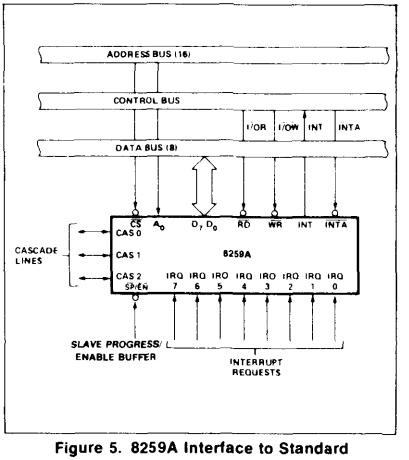


Figure 5. 8259A Interface to Standard System Bus

INTERRUPT SEQUENCE OUTPUTS

MCS-80®, MCS-85®

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the 8259A. When Interval = 8 only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8 - A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

iAPX 86, iAPX 88

iAPX 86 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the INTA pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in iAPX 86 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in iAPX 86 mode):

Content of Interrupt Vector Byte for iAPX 86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 8259A

The 8259A accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs):* Before normal operation can begin, each 8259A in the system must be brought to a starting point — by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.

2. *Operation Command Words (OCWs):* These are the command words which command the 8259A to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

INITIALIZATION COMMAND WORDS (ICWS)

GENERAL

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. The slave mode address is set to 7.
e. Special Mask Mode is cleared and Status Read is set to IRR.
f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

***Note:** Master/Slave in ICW4 is only used in the buffered mode

INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1, ICW2)

A_5-A_{15}: *Page starting address of service routines.* In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the 8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the 8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an iAPX 86 system A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then Interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for iAPX 86 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for iAPX 86 are released by it on the Data Bus.

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM = 1 the special fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 8259A for MCS-80, 85 system operation, μPM = 1 sets the 8259A for iAPX 86 system operation.

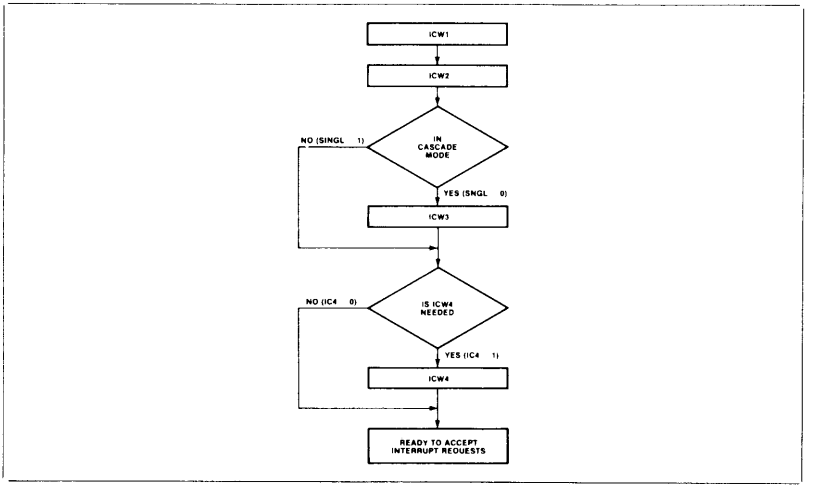


Figure 6. Initialization Sequence

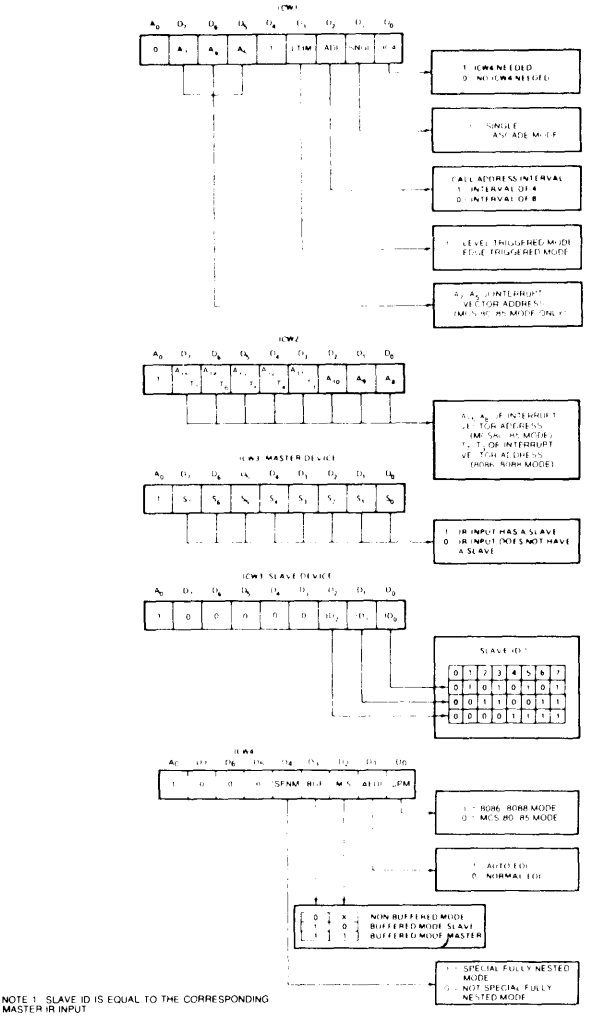


Figure 7. Initialization Command Word Format

OPERATION COMMAND WORDS (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)

OCW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2

0	R	SL	EOI	0	0	L2	L1	L0

OCW3

0	0	ESMM	SMM	0	1	P	RR	RIS

OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). $M_7 - M_0$ represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI — These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0—These bits determine the interrupt level acted upon when the SL bit is active.

OPERATION CONTROL WORD 3 (OCW3)

ESMM — Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit becomes a "don't care".

SMM — Special Mask Mode. If ESMM = 1 and SMM = 1 the 8259A will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 8259A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

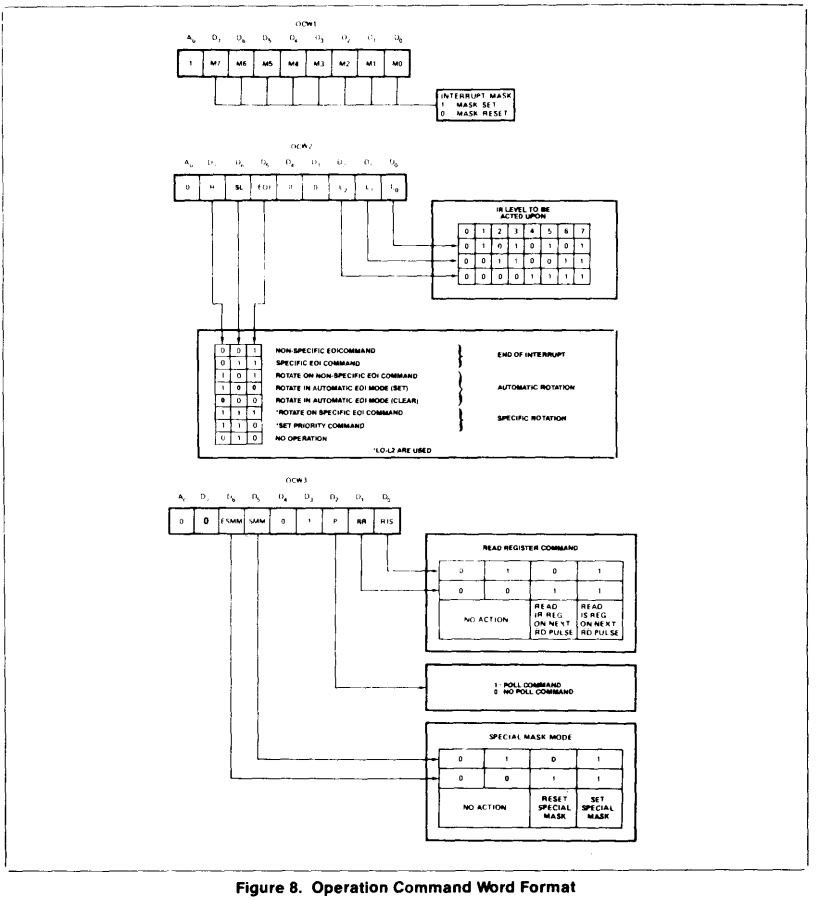


Figure 8. Operation Command Word Format

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority form 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal Interrupt enable flip-flop has been re-enabled through software).

After the Initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence INTA pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 8259A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 8259A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and LO-L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 8259A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

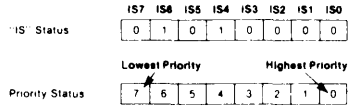
If AEOI = 1 in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in iAPX 86). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

The AEOI mode can only be used in a master 8259A and not a slave.

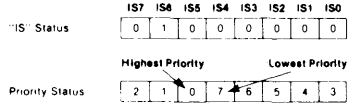
AUTOMATIC ROTATION (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)



After Rotate (IR4 was serviced, all other priorities rotated correspondingly)



There are two ways to accomplish Automatic Rotation using OCW2; the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

SPECIFIC ROTATION (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1; LO-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and LO-L2 = IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

POLL COMMAND

In this mode the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = "1" in OCW3. The 8259A treats the next $\overline{RD}$ pulse to the 8259A (i.e., $\overline{RD}$ = 0, $\overline{CS}$ = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	–	–	–	–	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

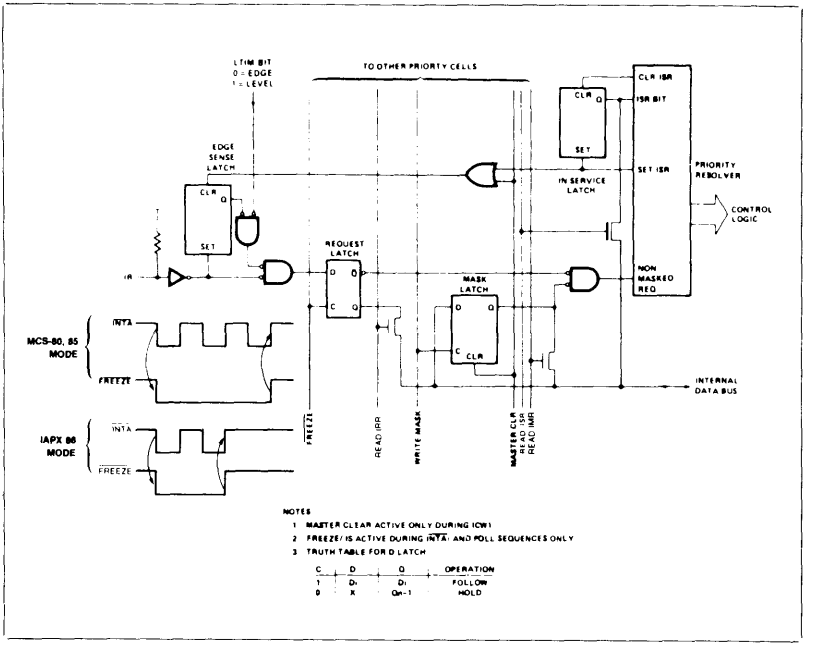


Figure 9. Priority Cell—Simplified Logic Diagram

READING THE 8259A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 (IMR)).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0.)

The ISR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and AO = 1 (OCW1).

Polling overrides status read when P = 1, RR = 1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

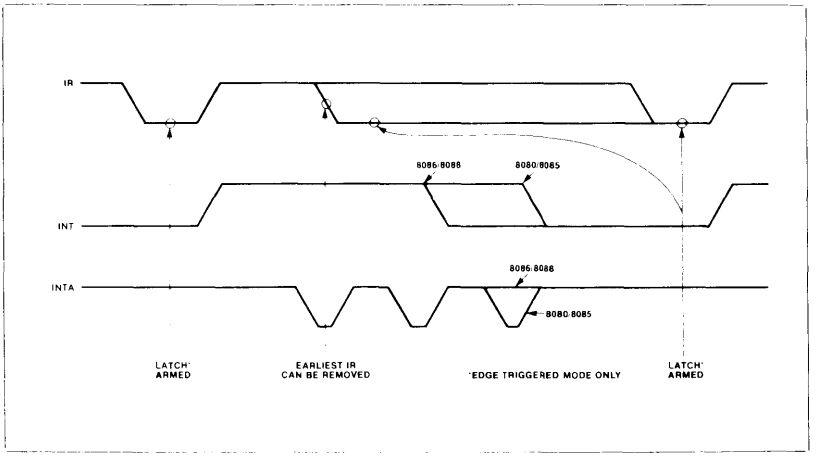


Figure 10. IR Triggering Timing Requirements

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

BUFFERED MODE

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each 8259A.

The cascade lines of the Master 8259A are activated only for slave inputs, non slave inputs leave the cascade line inactive (low).

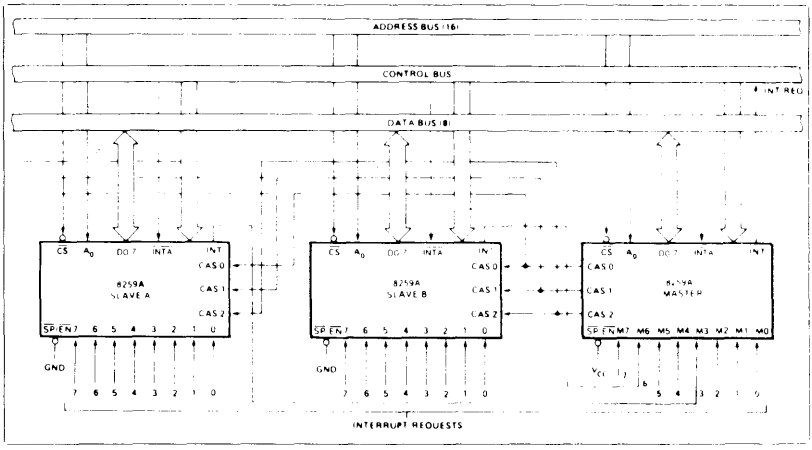


Figure 11. Cascading the 8259A

intel 8259A/8259A-2/8259A-8

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin
with Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS [T_A = 0°C to 70°C, V_{CC} = 5V ±5% (8259A-8), V_{CC} = 5V ±10% (8259A, 8259A-2)]

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0*	V_{CC} +0.5V	V	
V_{OL}	Output High Voltage		0.45	V	I_{OL} = 2.2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5		V	I_{OH} = −100μA
		2.4		V	I_{OH} = −400μA
I_{LI}	Input Load Current	−10	+10	μA	$0V \leq V_{IN} \leq V_{CC}$
I_{LOL}	Output Leakage Current	−10	+10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	V_{CC} Supply Current		85	mA	
I_{LIR}	IR Input Load Current		−300	μA	V_{IN} = 0
			10	μA	V_{IN} = V_{CC}

*Note: For Extended Temperature EXPRESS V_{IH} = 2.3V.

CAPACITANCE (T_A = 25°C; V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHZ
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS [T_A = 0°C to 70°C, V_{CC} = 5V ±5% (8259A-8), V_{CC} = 5V ± 10% (8259A, 8259A-2)]

TIMING REQUIREMENTS

Symbol	Parameter	8259A-8		8259A		8259A-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	50		0		0		ns	
TRHAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	5		0		0		ns	
TRLRH	$\overline{RD}$ Pulse Width	420		235		160		ns	
TAHWL	A0/$\overline{CS}$ Setup to $\overline{WR}$↓	50		0		0		ns	
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$↑	20		0		0		ns	
TWLWH	$\overline{WR}$ Pulse Width	400		290		190		ns	
TDVWH	Data Setup to $\overline{WR}$↑	300		240		160		ns	
TWHDX	Data Hold after $\overline{WR}$↑	40		0		0		ns	
TJLJH	Interrupt Request Width (Low)	100		100		100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave Only)	55		55		40		ns	
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		160		160		ns	
TWHWL	End of $\overline{WR}$ to next $\overline{WR}$	190		190		190		ns	

A.C. CHARACTERISTICS (Continued)

Symbol	Parameter	8259A-8		8259A		8259A-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
*TCHCL	End of Command to next Command (Not same command type)	500		500		500		ns	
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence.								

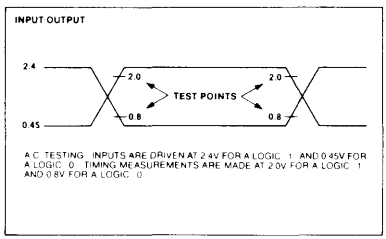
*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6μs, 8085A-2 = 1μs, 8086 = 1μs, 8086-2 = 625 ns)

NOTE: This is the low time required to clear the input latch in the edge triggered mode.

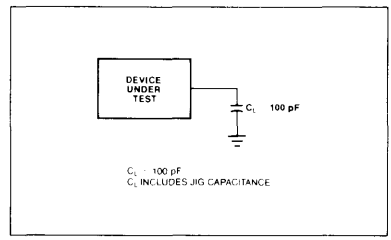
TIMING RESPONSES

Symbol	Parameter	8259A-8		8259A		8259A-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$		300		200		120	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$	10	200	10	100	10	85	ns	C of Data Bus Max test C = 100 pF Min test C = 15 pF
TJHIH	Interrupt Output Delay		400		350		300	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$ (Master Only)		565		565		360	ns	C_{INT} = 100 pF
TRLEL	Enable Active from $\overline{RD}$ or $\overline{INTA}$		160		125		100	ns	$C_{CASCADE}$ = 100 pF
TRHEH	Enable Inactive from $\overline{RD}$ or $\overline{INTA}$		325		150		150	ns	
TAHDV	Data Valid from Stable Address		350		200		200	ns	
TCVDV	Cascade Valid to Valid Data		300		300		200	ns	

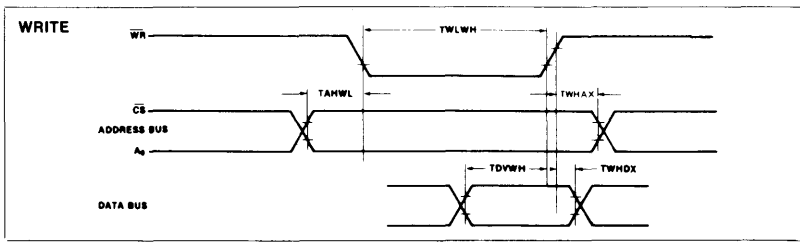
A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



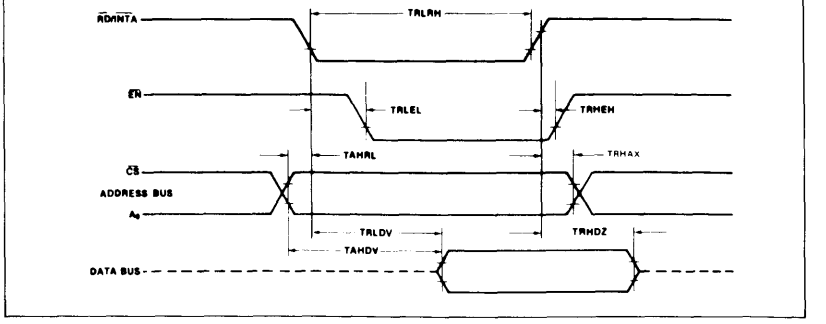
WAVEFORMS



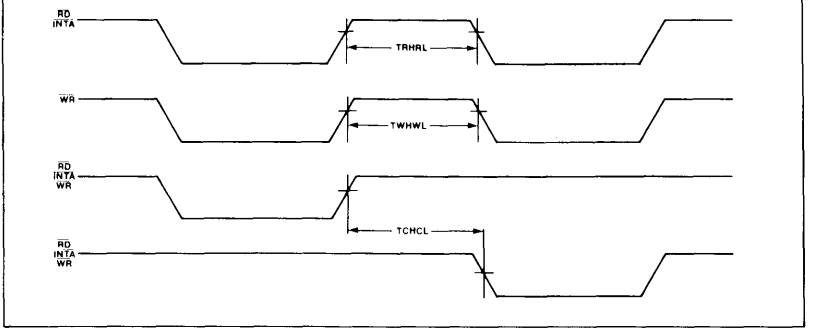
AFN 00221E

WAVEFORMS (Continued)

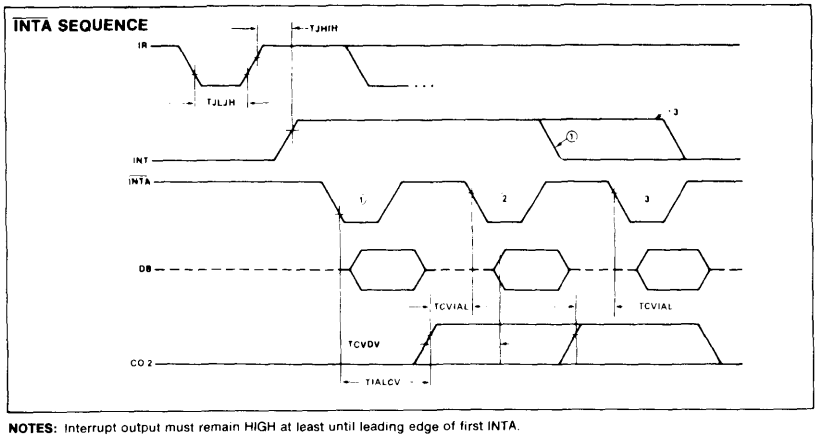
READ/INTA



OTHER TIMING



WAVEFORMS (Continued)

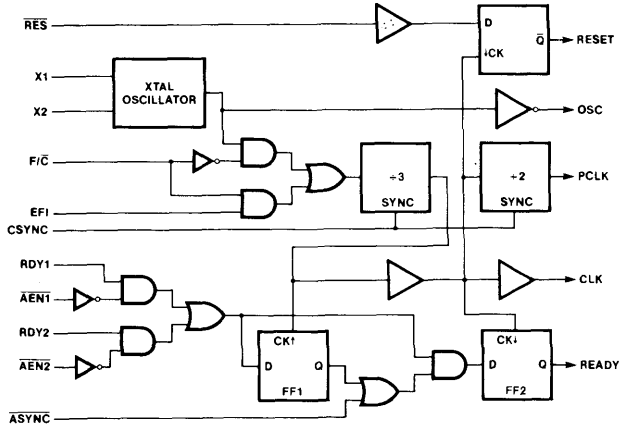


NOTES: Interrupt output must remain HIGH at least until leading edge of first INTA.
1. Cycle 1 in iAPX 86, iAPX 88 systems, the Data Bus is not active.

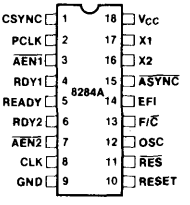
intel

8284A/8284A-1
CLOCK GENERATOR AND DRIVER FOR iAPX 86, 88 PROCESSORS

- Generates the System Clock for the iAPX 86, 88 Processors: 5 MHz, 8 MHz with 8284A 10 MHz with 8284A-1
- Uses a Crystal or a TTL Signal for Frequency Source
- Provides Local READY and Multibus™ READY Synchronization
- 18-Pin Package
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other 8284As
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range



8284A/8284A-1 Block Diagram



8284A/8284A-1 Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
$\overline{AEN1}$, $\overline{AEN2}$	I	**Address Enable:** $\overline{AEN}$ is an active LOW signal. AEN serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	**Bus Ready:** (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	I	**Ready Synchronization Select:** $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open (internal pull-up resistor is provided) or HIGH a single stage of READY synchronization is provided.
READY	O	**Ready:** READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	**Crystal In:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	I	**Frequency/Crystal Select:** F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	**External Frequency:** When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	O	**Processor Clock:** CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is ⅓ of the crystal or EFI input frequency and a ⅓ duty cycle. An output HIGH of 4.5 volts (V_{CC} = 5V) is provided on this pin to drive MOS devices.
PCLK	O	**Peripheral Clock:** PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK and has a 50% duty cycle.
OSC	O	**Oscillator Output:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	**Reset In:** $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	**Reset:** RESET is an active HIGH signal which is used to reset the 8086 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	I	**Clock Synchronization:** CSYNC is an active HIGH signal which allows multiple 8284As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		**Ground.**
V_{CC}		**Power:** +5V supply.

FUNCTIONAL DESCRIPTION

General

The 8284A is a single chip clock generator/driver for the iAPX 86, 88 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS™ "Ready" synchronization and reset logic. Refer to Figure 1 for Block Diagram and Figure 2 for Pin Configuration.

Oscillator

The oscillator circuit of the 8284A is designed primarily for use with an external series resonant, fundamental mode, crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two series resistors ($R_1 = R_2 = 510\ \Omega$) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

For systems which have a V_{CC} ramp time $\geq$ 1V/ms and/or have inherent board capacitance between X1 or X2, exceeding 10 pF (not including 8284A pin capacitance), the two 510Ω resistors should be used. This circuit provides optimum stability for the oscillator in such extreme conditions. It is advisable to limit stray capacitances to less than 10 pF on X1 and X2 to minimize deviation from operating at the fundamental frequency.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 8284A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 8284A. This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle MOS clock driver designed to drive the iAPX 86, 88 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is ½ that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 8284A.

READY Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, T_{R1VCL}, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

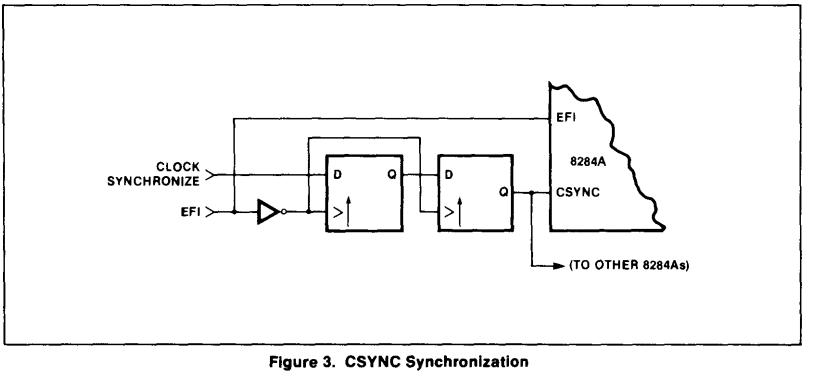


Figure 3. CSYNC Synchronization

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages ..... −1.0V to +5.5V
Power Dissipation ..... 1 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_F	Forward Input Current ($\overline{ASYNC}$) Other Inputs		−1.3 −0.5	mA mA	V_F = 0.45V V_F = 0.45V
I_R	Reverse Input Current ($\overline{ASYNC}$) Other Inputs		50 50	μA μA	$V_R = V_{CC}$ V_R = 5.25V
V_C	Input Forward Clamp Voltage		−1.0	V	I_C = −5mA
I_{CC}	Power Supply Current		162	mA	
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
V_{IHR}	Reset Input HIGH Voltage	2.6		V	
V_{OL}	Output LOW Voltage		0.45	V	5mA
V_{OH}	Output HIGH Voltage CLK Other Outputs	4 2.4		V V	−1mA −1mA
$V_{IHR} - V_{ILR}$	$\overline{RES}$ Input Hysteresis	0.25		V	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{EHEL}	External Frequency HIGH Time	13		ns	90% - 90% V_{IN}
t_{ELEH}	External Frequency LOW Time	13		ns	10% - 10% V_{IN}
t_{ELEL}	EFI Period	33		ns	(Note 1)
	XTAL Frequency	12	25	MHz	
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = HIGH
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		ns	
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK	50		ns	
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK	0		ns	
t_{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15		ns	
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		ns	
t_{EHYL}	CSYNC Hold to EFI	10		ns	
t_{YHYL}	CSYNC Width	$2 \cdot t_{ELEL}$		ns	
t_{I1HCL}	$\overline{RES}$ Setup to CLK	65		ns	(Note 1)
t_{CLI1H}	$\overline{RES}$ Hold to CLK	20		ns	(Note 1)

A.C. CHARACTERISTICS (Continued)

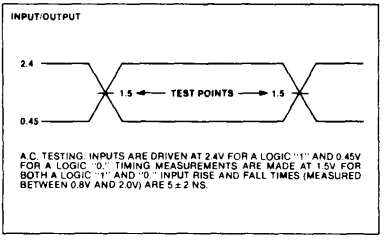
TIMING RESPONSES

Symbol	Parameter	Min. 8284A	Min. 8284A-1	Max.	Units	Test Conditions
t_{CLCL}	CLK Cycle Period	125	100		ns	
t_{CHCL}	CLK HIGH Time	$(1/3\ t_{CLCL})+2$	39		ns	
t_{CLCH}	CLK LOW Time	$(2/3\ t_{CLCL})-15$	53		ns	
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time			10	ns	1.0V to 3.5V
t_{PHPL}	PCLK HIGH Time	$t_{CLCL}-20$	$t_{CLCL}-20$		ns	
t_{PLPH}	PCLK LOW Time	$t_{CLCL}-20$	$t_{CLCL}-20$		ns	
t_{AYLCL}	Ready Inactive to CLK (See Note 3)	−8	−8		ns	
t_{RYHCH}	Ready Active to CLK (See Note 2)	$(2/3\ t_{CLCL})-15$	53		ns	
t_{CLIL}	CLK to Reset Delay			40	ns	
t_{CLPH}	CLK to PCLK HIGH DELAY			22	ns	
t_{CLPL}	CLK to PCLK LOW Delay			22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	−5	−5	22	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	2	35	ns	
t_{OLOH}	Output Rise Time (except CLK)			20	ns	From 0.8V to 2.0V
t_{OHOL}	Output Fall Time (except CLK)			12	ns	From 2.0V to 0.8V

NOTES:

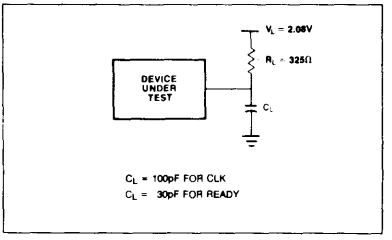
1. Setup and hold necessary only to guarantee recognition at next clock.
2. Applies only to T3 and TW states.
3. Applies only to T2 states.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0." INPUT RISE AND FALL TIMES (MEASURED BETWEEN 0.8V AND 2.0V) ARE 5 ± 2 NS.

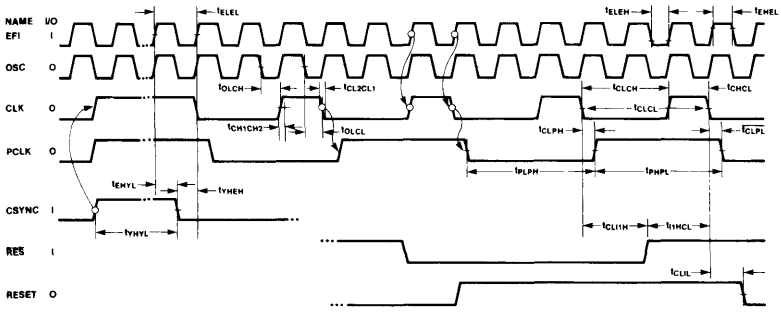
A.C. TESTING LOAD CIRCUIT



C_L = 100pF FOR CLK
C_L = 30pF FOR READY

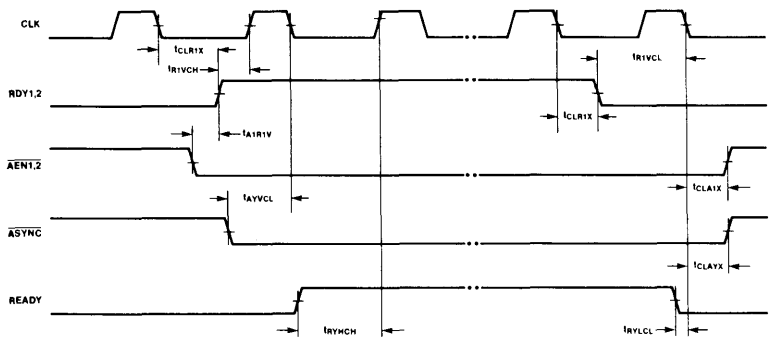
WAVEFORMS

CLOCKS AND RESET SIGNALS



NOTE: ALL TIMING MEASUREMENTS ARE MADE AT 1.5 VOLTS, UNLESS OTHERWISE NOTED.

READY SIGNALS (FOR ASYNCHRONOUS DEVICES)



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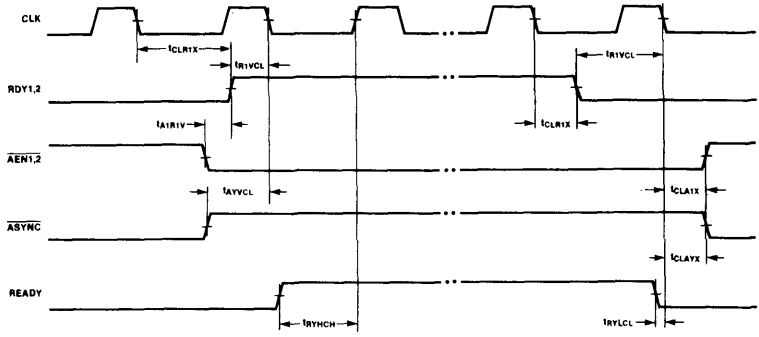
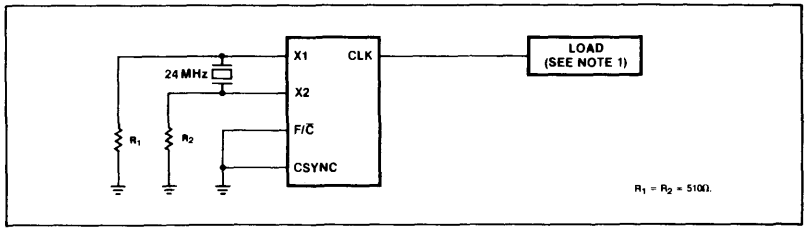
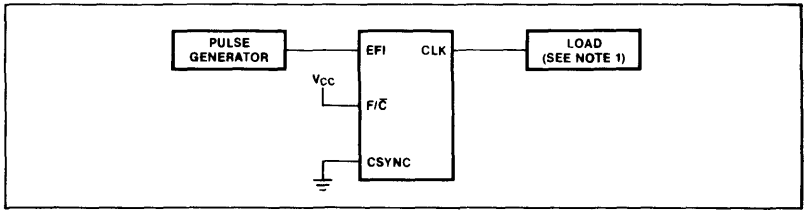
WAVEFORMS (Continued)

READY SIGNALS (FOR SYNCHRONOUS DEVICES)

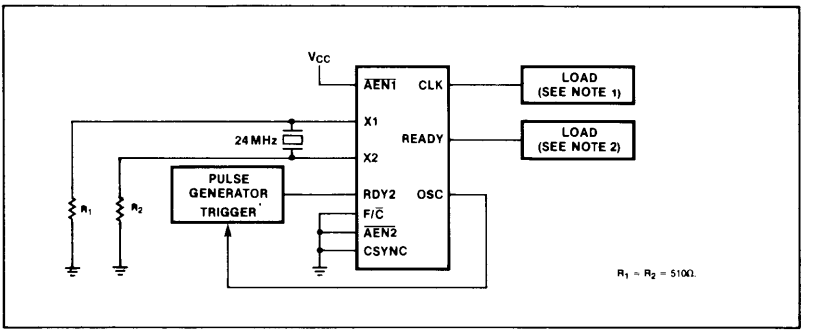




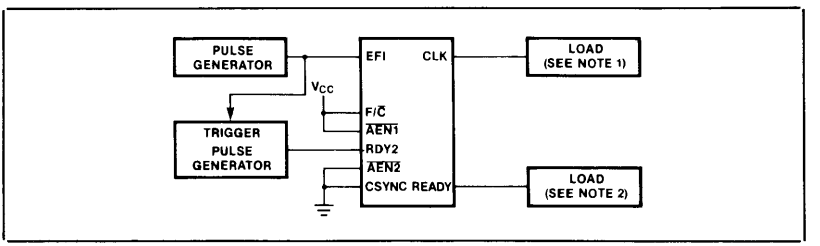
Clock High and Low Time (Using X1, X2)



Clock High and Low Time (Using EFI)



Ready to Clock (Using X1, X2)



Ready to Clock (Using EFI)

NOTES:
1. C_L = 100 pF
2. C_L = 30 pF

intel

8237A/8237A-4/8237A-5
HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER

- **Enable/Disable Control of Individual DMA Requests**
- **Four Independent DMA Channels**
- **Independent Autoinitialization of all Channels**
- **Memory-to-Memory Transfers**
- **Memory Block Initialization**
- **Address Increment or Decrement**
- **High performance: Transfers up to 1.6M Bytes/Second with 5 MHz 8237A-5**
- **Directly Expandable to any Number of Channels**
- **End of Process Input for Terminating Transfers**
- **Software DMA Requests**
- **Independent Polarity Control for DREQ and DACK Signals**
- **Available in EXPRESS**
  - **Standard Temperature Range**

The 8237A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 8237A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The 8237A is designed to be used in conjunction with an external 8-bit address register such as the 8282. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process ($\overline{EOP}$).

Each channel has a full 64K address and word count capability.

The 8237A-4 and 8237A-5 are 4 MHz and 5 MHz selected versions of the standard 3 MHz 8237A respectively.

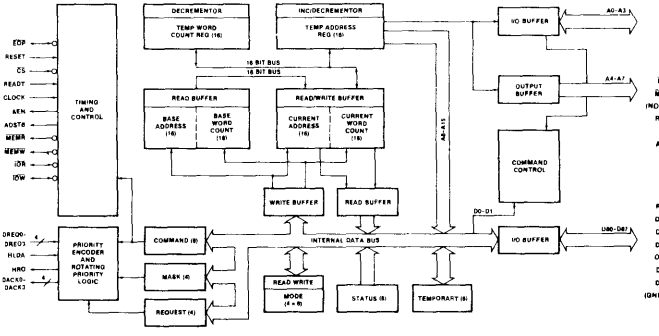


Figure 1. Block Diagram

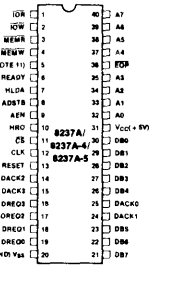


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
V_{CC}		**Power:** +5 volt supply.
V_{SS}		**Ground:** Ground.
CLK	I	**Clock Input:** Clock Input controls the internal operations of the 8237A and its rate of data transfers. The input may be driven at up to 3 MHz for the standard 8237A and up to 5 MHz for the 8237A-5.
CS	I	**Chip Select:** Chip Select is an active low input used to select the 8237A as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
RESET	I	**Reset:** Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY	I	**Ready:** Ready is an input used to extend the memory read and write pulses from the 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
HLDA	I	**Hold Acknowledge:** The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DREQ0-DREQ3	I	**DMA Request:** The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset intializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.
DB0-DB7	I/O	**Data Bus:** The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 8237A control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 8237A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.
$\overline{IOR}$	I/O	**I/O Read:** I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 8237A to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	I/O	**I/O Write:** I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 8237A. In the Active cycle, it is an output control signal used by the 8237A to load data to the peripheral during a DMA Read transfer.
$\overline{EOP}$	I/O	**End of Process:** End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 8237A allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The 8237A also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ Line. The reception of $\overline{EOP}$, either internal or external, will cause the 8237A to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.
A0-A3	I/O	**Address:** The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
A4-A7	O	**Address:** The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	**Hold Request:** This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ. After HRQ goes active at least one clock cycle (TCY) must occur before HLDA goes active.
DACK0-DACK3	O	**DMA Acknowledge:** DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	O	**Address Enable:** Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	**Address Strobe:** The active high, Address Strobe is used to strobe the upper address byte into an external latch.
$\overline{MEMR}$	O	**Memory Read:** The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{MEMW}$	O	**Memory Write:** The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

FUNCTIONAL DESCRIPTION

The 8237A block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The 8237A contains 344 bits of internal memory in the form of registers. Figure 3 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 3. 8237A Internal Registers

The 8237A contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the 8237A. The Program Command Control block decodes the various commands given to the 8237A by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In 8237A systems this input will usually be the $\phi 2$ TTL clock from an 8224 or CLK from an 8085AH or 8284A. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) does not satisfy 8237A-5 clock LOW and HIGH time requirements. In this case, an external clock should be used to drive the 8237A-5.

DMA Operation

The 8237A is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The 8237A can assume seven separate states, each composed of one full clock period. State i (SI) is the inactive state. It is entered when the 8237A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State S0 (S0) is the first state of a DMA service. The 8237A has requested a hold but the processor has not yet returned an acknowledge. The 8237A may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the 8237A. Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is not read into or driven out of the 8237A in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half

and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

IDLE CYCLE

When no channel is requesting service, the 8237A will enter the Idle cycle and perform "SI" states. In this cycle the 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the 8237A. When $\overline{CS}$ is low and HLDA is low, the 8237A enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or Reset. A separate software command can also reset this flip-flop.

Special software commands can be executed by the 8237A in the Program Condition. These commands are decoded as sets of addresses with the $\overline{CS}$ and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Clear First/Last Flip-FLop and Master Clear.

ACTIVE CYCLE

When the 8237A is in the Idle cycle and a non-masked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode — In Single Transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, in 8080A, 8085AH, 8088, or 8086 system this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 8237A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode — In Block Transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process (EOP) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode — In Demand Transfer mode the device is programmed to continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 8237A Current Address and Current Word Count registers. Only an $\overline{EOP}$ can cause an Autoinitialize at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode—This mode is used to cascade more than one 8237A together for simple system expansion. The HRQ and HLDA signals from the additional 8237A are connected to the DREQ and DACK signals of a channel of the initial 8237A. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 8237A is used only for prioritizing the additional device, it does not output any address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The 8237A will respond to DREQ and DACK but all other outputs except HRQ will be disabled. The ready input is ignored.

Figure 4 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More 8237As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

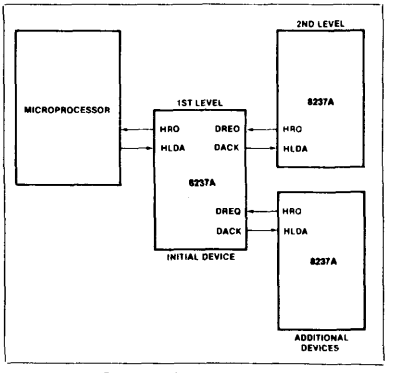


Figure 4. Cascaded 8237As

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from and I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers. The 8237A operates as in Read or Write transfers generating addresses, and responding to EOP, etc. However, the memory and I/O control lines all remain inactive. The ready input is ignored in verify mode.

Memory-to-Memory—To perform block moves of data from one memory address space to another with a minimum of program effort and time, the 8237A includes a memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 to 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The 8237A requests a DMA service in the normal manner. After HLDA is true, the device, using four state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 8237A internal Temporary register. Channel 1 then performs a four-state transfer of the data from the Temporary register to memory using the address in its Current Address register and incrementing or decrementing it in the normal manner. The channel 1 current Word Count is decremented. When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output terminating the service.

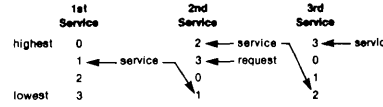
Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.

The 8237A will respond to external $\overline{EOP}$ signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 12. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Autoinitialize—By programming a bit in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialize initialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not altered when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected. In order to Autoninitialize both channels in a memory-to-memory transfer, both word counts should be programmed identically. If interrupted externally, $\overline{EOP}$ pulses should be applied in both bus cycles.

Priority—The 8237A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interferring with that service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Compressed Timing — In order to achieve even greater throughput where system characteristics permit, the 8237A can compress the transfer time to two clock cycles. From Figure 11 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 14.

Address Generation — In order to reduce pin count, the 8237A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 8237A directly. Lines A0-A7 should be connected to the address bus. Figure 11 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode services, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 8237A executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

REGISTER DESCRIPTION

Current Address Register — Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$.

Current Word Register — Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

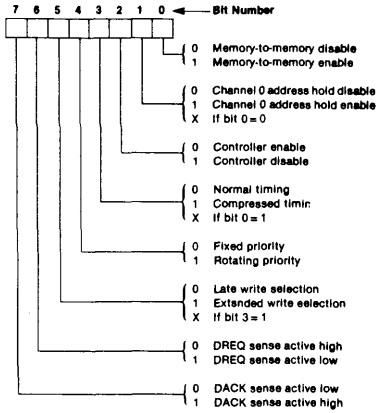
Base Address and Base Word Count Registers — Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register — This 8-bit register controls the operation of the 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction. The following table lists the function of the command bits. See Figure 6 for address coding.

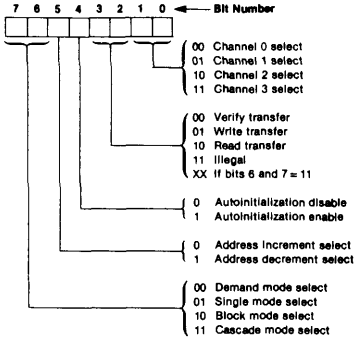
Mode Register — Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

Request Register — The 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 5 for register address coding. In order to make a software request, the channel must be in Block Mode.

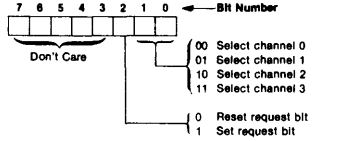
Command Register



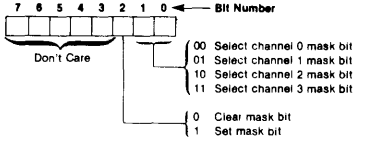
Mode Register



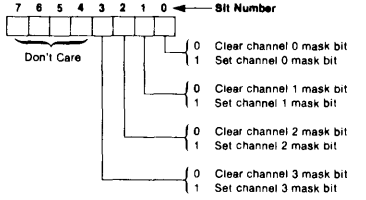
Request Register



Mask Register — Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 5 for instruction addressing.



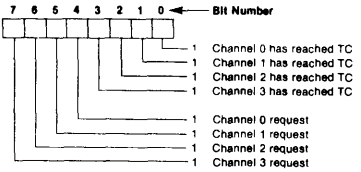
All four bits of the Mask register may also be written with a single command.



Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Figure 5. Definition of Register Codes

Status Register — The Status register is available to be read out of the 8237A by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.



Temporary Register — The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands—These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The three software commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the 8237A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The 8237A will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Figure 6 lists the address codes for the software commands:

Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 6. Software Command Codes

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0-DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W)0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W)0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W)0-W7
			0	0	1	0	1	1	1	1	W8-W15

Figure 7. Word Count and Address Register Command Codes

PROGRAMMING

The 8237A will accept programming from the host processor any time that HLDA is inactive; this is true even if HRQ is active. The responsibility of the host is to assure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs, on an unmasked channel while the 8237A is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the 8237A is enabled (bit 2 in the command register is 0) and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any other registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations, especially the Mode registers, be loaded with some valid value. This should be done even if some channels are unused.

APPLICATION INFORMATION

Figure 8 shows a convenient method for configuring a DMA system with the 8237A controller and an 8080A/8085AH microprocessor system. The multimode DMA controller issues a HRQ to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a HLDA signal, the 8237A takes control of the address bus, the data bus and the control bus. The address for the first transfer operation comes out in two bytes — the least significant 8 bits on the eight address outputs and the most significant 8 bits on the data bus. The contents of the data bus are then latched into the 8282 8-bit latch to complete the full 16 bits of the address bus. The 8282 is a high speed, 8-bit, three-state latch in a 20-pin package. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one 8237A is used.

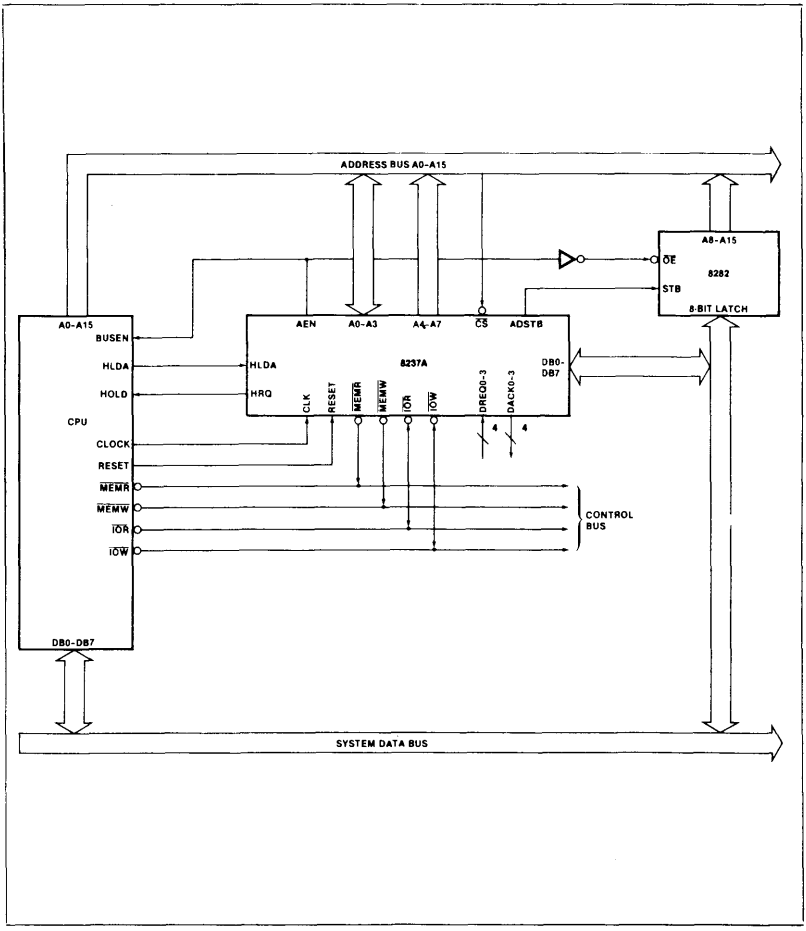


Figure 8. 8237A System Interface

AFN-00789D

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . – 65°C to + 150°C
Voltage on any Pin with
Respect to Ground . . . . . – 0.5 to 7V
Power Dissipation . . . . . 1.5 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%, GND = 0V)

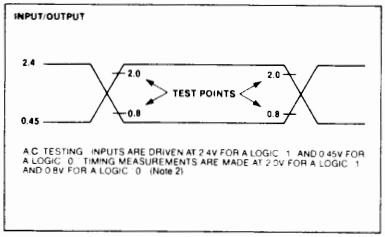
Symbol	Parameter	Min.	Typ.(1)	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -200 μA
		3.3			V	I_{OH} = -100 μA (HRQ Only)
V_{OL}	Output LOW Voltage			45	V	I_{OL} = 2.0mA (data Bus) $\overline{EDP}$ I_{OL} = 3.2mA (other outputs) (Note 8) I_{OL} = 2.5mA (ADSTB) (Note 8)
V_{IH}	Input HIGH Voltage	2.2		V_{CC} + 0.5	V	
V_{IL}	Input LOW Voltage	-0.5		0.8	V	
I_{LI}	Input Load Current			±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		110	130	mA	T_A = +25°C
			130	150	mA	T_A = 0°C
C_O	Output Capacitance		4	8	pF	fc = 1.0 MHz, Inputs = 0V
C_I	Input Capacitance		8	15	pF	
C_{IO}	I/O Capacitance		10	18	pF	

NOTES:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. Input timing parameters assume transition times of 20 ns or less. Waveform measurement points for both input and output signals are 2.0V for HIGH and 0.8V for LOW, unless otherwise noted.
3. Output loading is 1 TTL gate plus 150pF capacitance, unless otherwise noted.
4. The net $\overline{IOW}$ or $\overline{MEMW}$ Pulse width for normal write will be TCY-100 ns and for extended write will be 2TCY-100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50 ns and for compressed read will be TCY-50 ns.
5. TDQ is specified for two different output HIGH levels. TDQ1 is measured at 2.0V. TDQ2 is measured at 3.3V. The value for TDQ2 assumes an external 3.3kΩ pull-up resistor connected form HRQ to V_{CC}.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. A revision of the 8237A is planned for shipment in April 1984, which will improve the following characteristics:
   1. V_{IH} from 2.2V to 2.0V
   2. V_{OL} from 0.45V to 0.4V on all outputs. Test condition I_{OL} = 3.2 mA.

   Please contact your local sales office at that time for more information.
9. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 600 ns for the 8237A, at least 500 ns for the 8237A-4 and at least 400 ns for the 8237A-5, as recovery time between active read or write pulses.
10. $\overline{EOP}$ is an open collector output. This parameter assumes the presence of a 2.2K pullup to V_{CC}.
11. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended however, that pin 5 be tied to V_{CC}.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. CHARACTERISTICS—DMA (MASTER) MODE ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V)

Symbol	Parameter	8237A		8237A-4		8237A-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		300		225		200	ns
TAET	AEN LOW from CLK HIGH (SI) Delay Time		200		150		130	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		150		120		90	ns
TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float from CLK HIGH		150		120		120	ns
TAFDB	DB Active to Float Delay from CLK HIGH		250		190		170	ns
TAHR	ADR from $\overline{READ}$ HIGH Hold Time	TCY-100		TCY-100		TCY-100		ns
TAHS	DB from ADSTB LOW Hold Time	50		40		30		ns
TAHW	ADR from $\overline{WRITE}$ HIGH Hold Time	TCY-50		TCY-50		TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time (Note 7)		250		220		170	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time (Note 10)		250		190		170	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time		250		190		170	ns
TASM	ADR Stable from CLK HIGH		250		190		170	ns
TASS	DB to ADSTB LOW Setup Time	100		100		100		ns
TCH	Clock High Time (Transitions ≤ 10 ns)	120		100		80		ns
TCL	Clock LOW Time (Transitions ≤ 10 ns)	150		110		68		ns
TCY	CLK Cycle Time	320		250		200		ns
TDCL	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay (Note 4)		270		200		190	ns
TDCTR	$\overline{READ}$ HIGH from CLK HIGH (S4) Delay Time (Note 4)		270		210		190	ns
TDCTW	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time (Note 4)		200		150		130	ns
TDQ1	HRQ Valid from CLK HIGH Delay Time (Note 5)		160		120		120	ns
TDQ2			250		190		120	ns
TEPS	$\overline{EOP}$ LOW from CLK LOW Setup Time	60		45		40		ns
TEPW	$\overline{EOP}$ Pulse Width	300		225		220		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		250		190		170	ns
TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH		200		150		150	ns
TFADB	DB Float to Active Delay from CLK HIGH		300		225		200	ns
THS	HLDA Valid to CLK HIGH Setup Time	100		75		75		ns
TIDH	Input Data from $\overline{MEMR}$ HIGH Hold Time	0		0		0		ns
TIDS	Input Data to $\overline{MEMR}$ HIGH Setup Time	250		190		170		ns
TODH	Output Data from $\overline{MEMW}$ HIGH Hold Time	20		20		10		ns
TODV	Output Data Valid to $\overline{MEMW}$ HIGH	200		125		125		ns
TQS	DREQ to CLK LOW (SI, S4) Setup Time (Note 7)	0		0		0		ns
TRH	CLK to READY LOW Hold Time	20		20		20		ns
TRS	READY to CLK LOW Setup Time	100		60		60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		200		150		130	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		140		110		90	ns

A.C. CHARACTERISTICS—PERIPHERAL (SLAVE) MODE (T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, GND = 0V)

Symbol	Parameter	8237A		8237A-4		8237A-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50		50		50		ns
TAW	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		130		ns
TCW	CS LOW to $\overline{WRITE}$ HIGH Setup Time	200		150		130		ns
TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		130		ns
TRA	ADR or CS Hold from $\overline{READ}$ HIGH	0		0		0		ns
TRDE	Data Access from $\overline{READ}$ LOW (Note 3)		200		200		140	ns
TRDF	DB Float Delay from $\overline{READ}$ HIGH	20	100	20	100	0	70	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		500		ns
TRSTS	RESET to First $\overline{IOWR}$	2TCY		2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		300		ns
TRW	$\overline{READ}$ Width	300		250		200		ns
TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	20		20		20		ns
TWC	CS HIGH from $\overline{WRITE}$ HIGH Hold Time	20		20		20		ns
TWD	Data from $\overline{WRITE}$ HIGH Hold Time	30		30		30		ns
TWWS	Write Width	200		200		160		ns

WAVEFORMS

SLAVE MODE WRITE TIMING

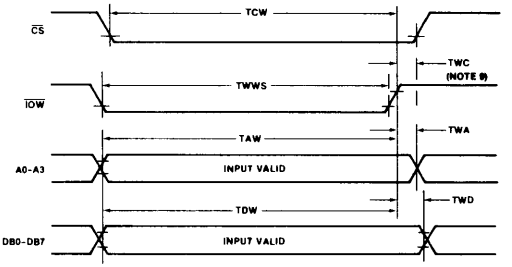


Figure 9. Slave Mode Write

SLAVE MODE READ TIMING

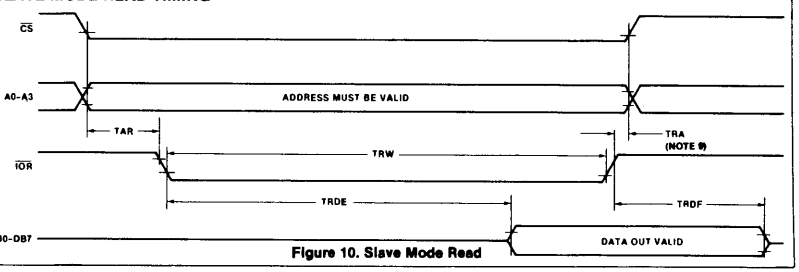


Figure 10. Slave Mode Read

WAVEFORMS (Continued)

DMA TRANSFER TIMING

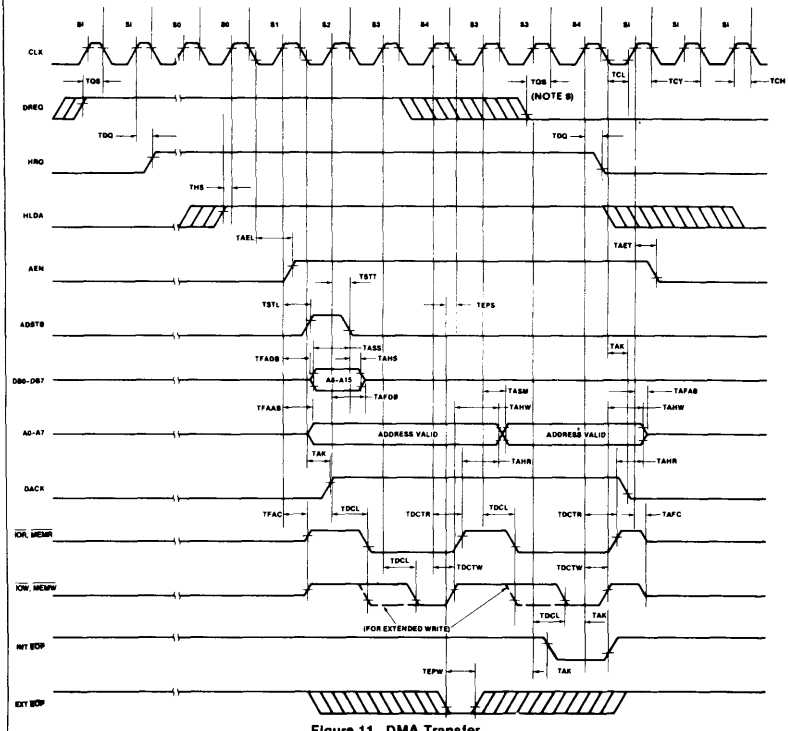


Figure 11. DMA Transfer

WAVEFORMS (Continued)

MEMORY-TO-MEMORY TRANSFER TIMING

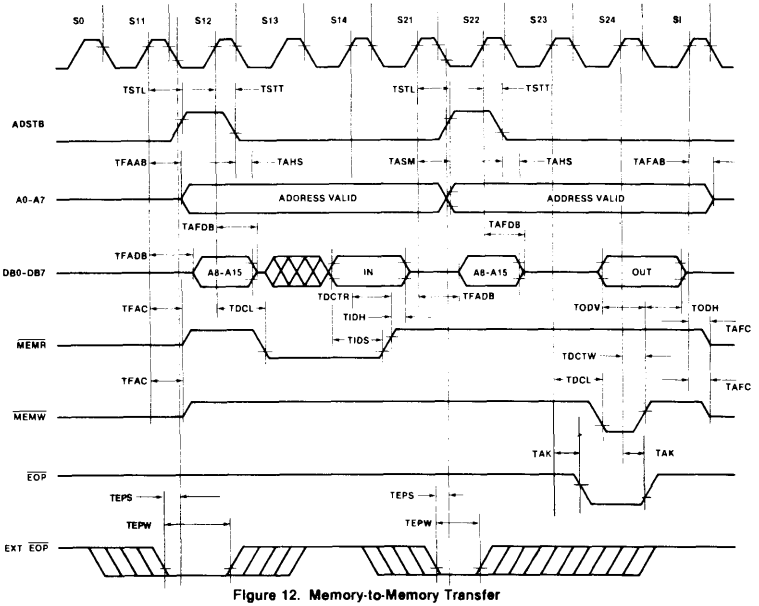


Figure 12. Memory-to-Memory Transfer

READY TIMING

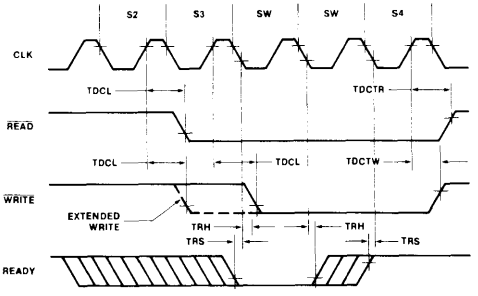


Figure 13. Ready

WAVEFORMS (Continued)

COMPRESSED TRANSFER TIMING

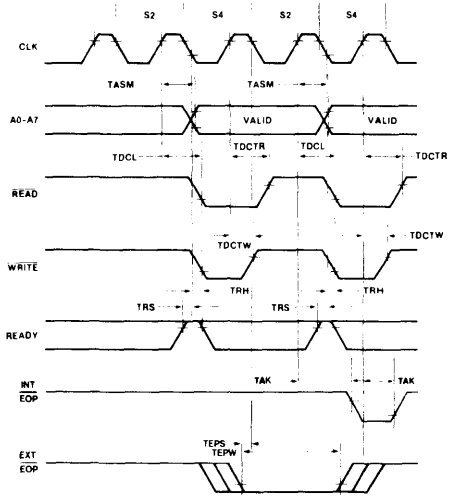


Figure 14. Compressed Transfer

RESET TIMING

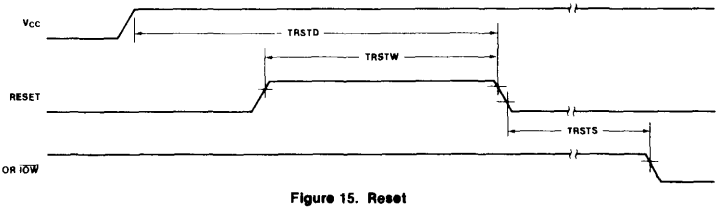


Figure 15. Reset

intel

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- **MCS-85™ Compatible 8255A-5**
- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with Intel® Microprocessor Families**
- **Improved Timing Characteristics**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **Reduces System Package Count**
- **Improved DC Driving Capability**
- **Available in EXPRESS**
  —Standard Temperature Range
  —Extended Temperature Range

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

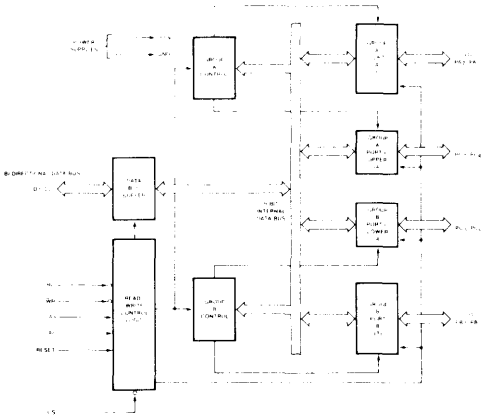


Figure 1. 8255A Block Diagram

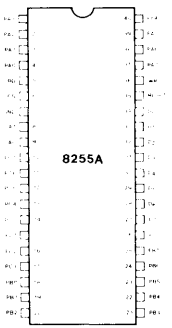


Figure 2. Pin Configuration

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communiction between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE

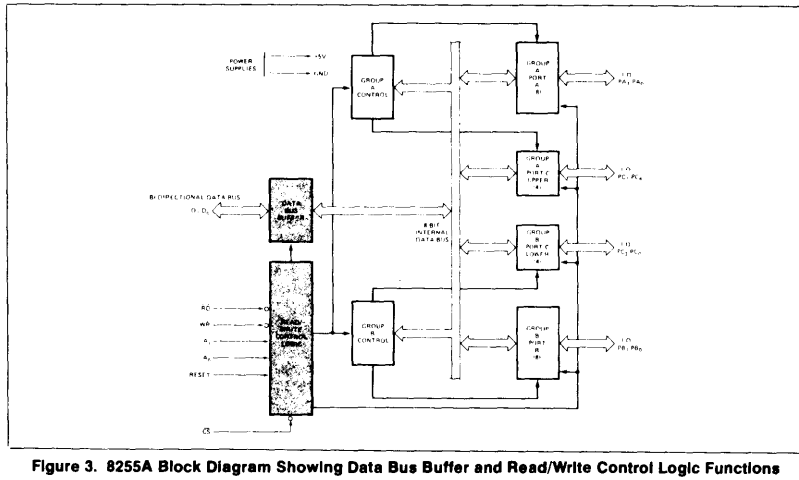


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

AFN-00744C

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

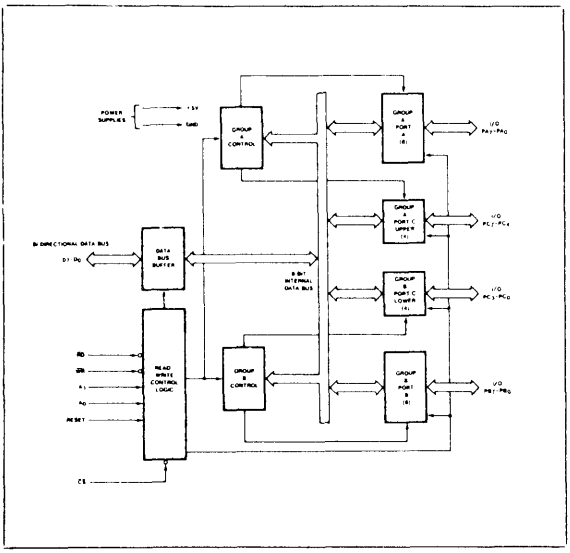
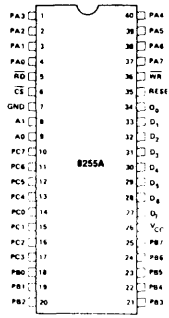


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

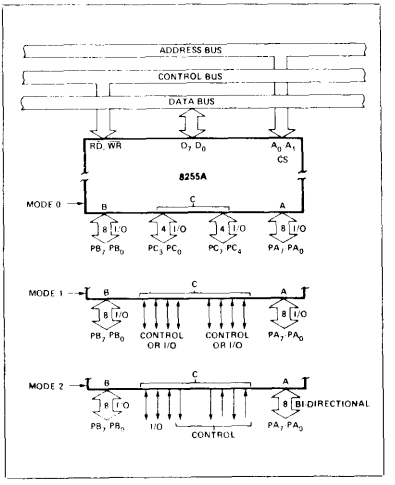


Figure 5. Basic Mode Definitions and Bus Interface

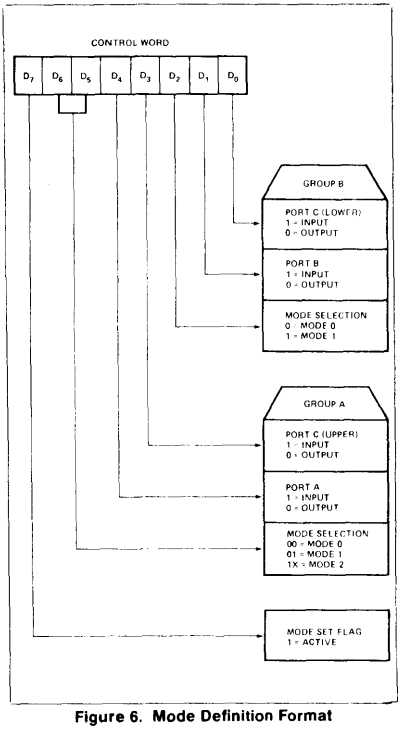


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

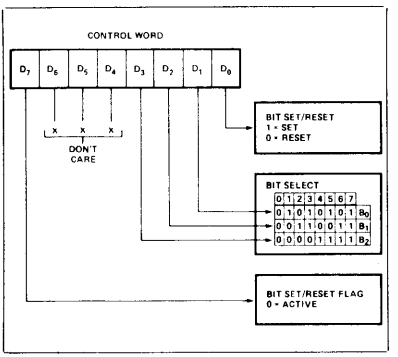


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) – INTE is SET – Interrupt enable
(BIT-RESET) – INTE is RESET – Interrupt disable

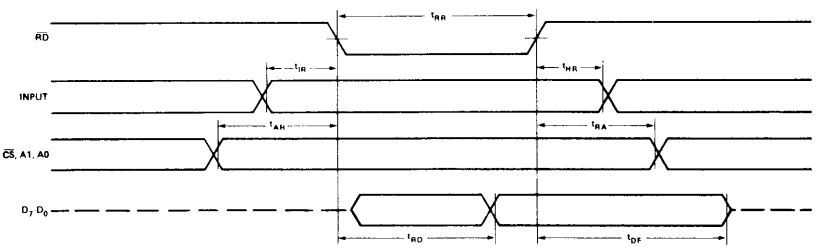
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

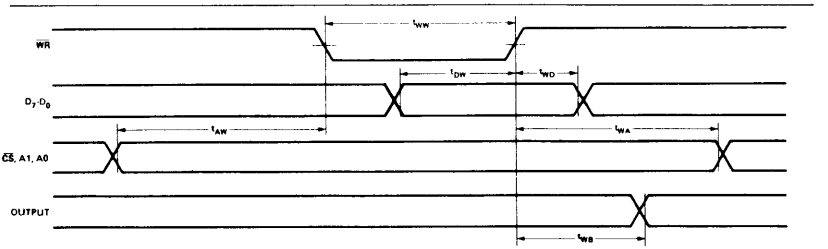
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)

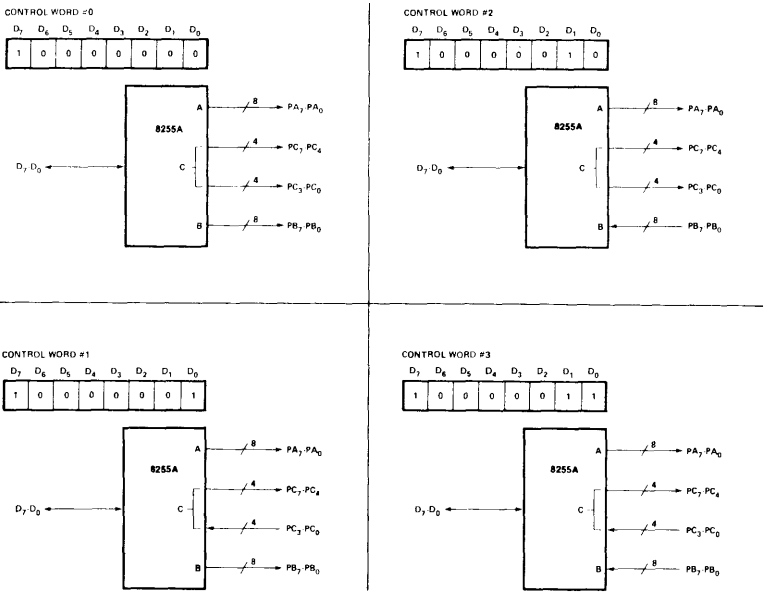


MODE 0 (Basic Output)

MODE 0 Port Definition

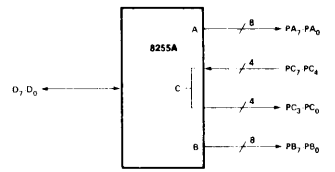
A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations



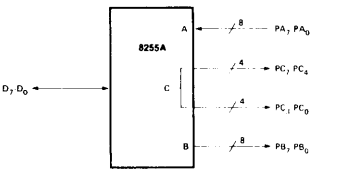
CONTROL WORD =4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



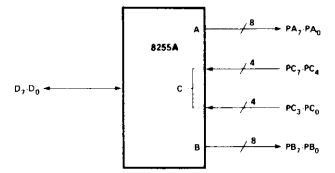
CONTROL WORD =8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



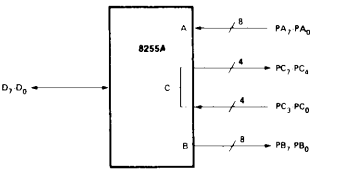
CONTROL WORD =5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



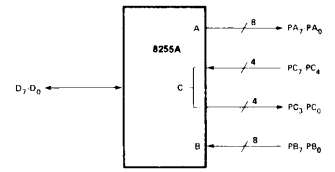
CONTROL WORD =9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



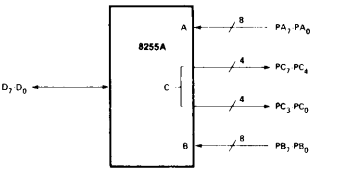
CONTROL WORD =6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



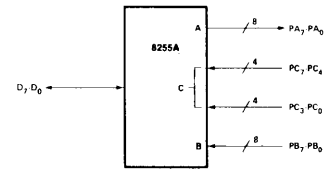
CONTROL WORD =10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



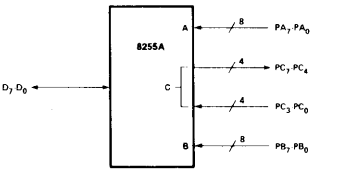
CONTROL WORD =7

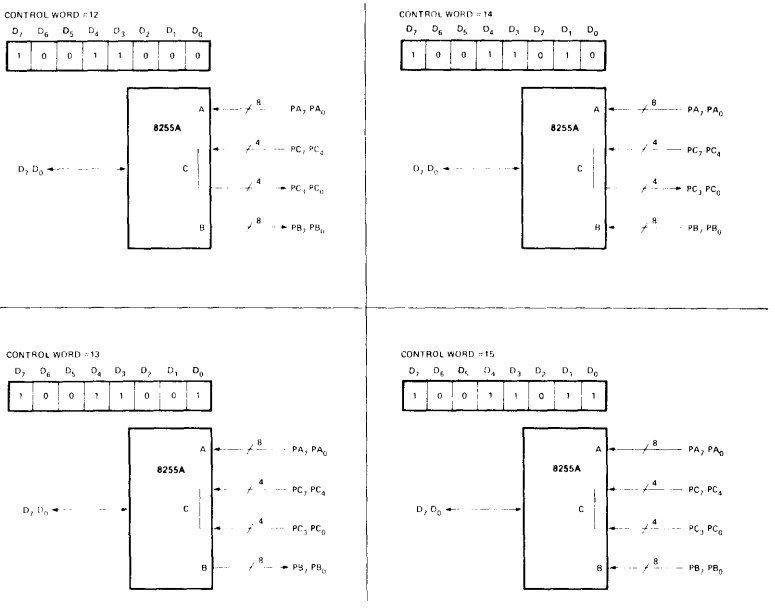
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



CONTROL WORD =11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1





Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

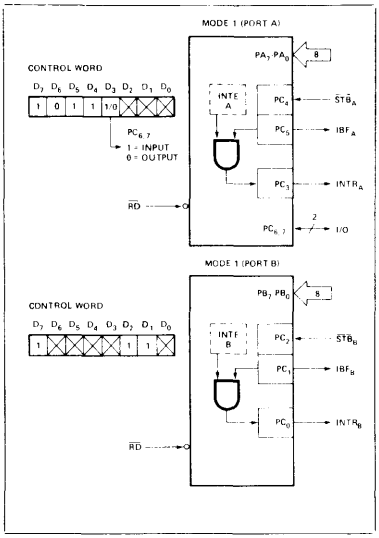


Figure 8. MODE 1 Input

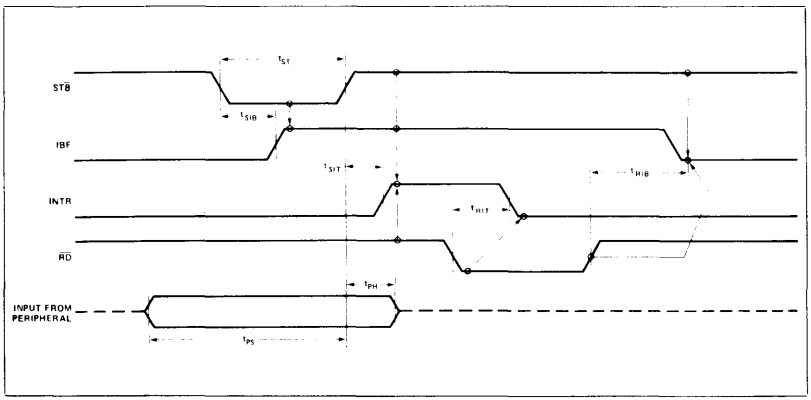


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

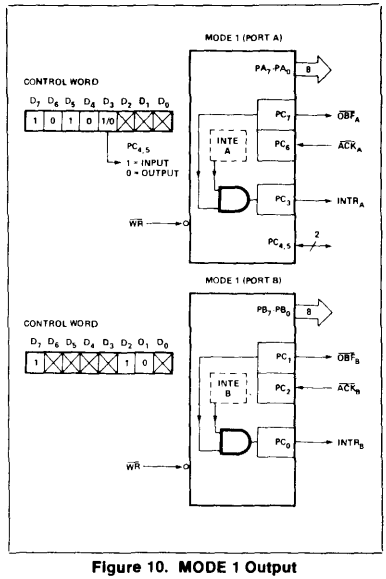


Figure 10. MODE 1 Output

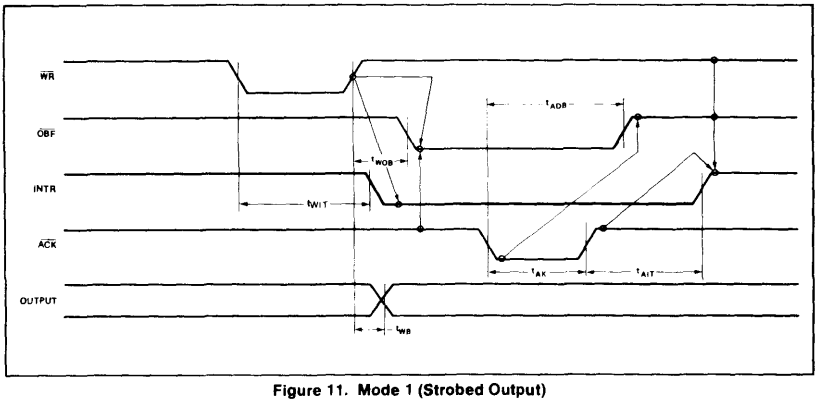


Figure 11. Mode 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

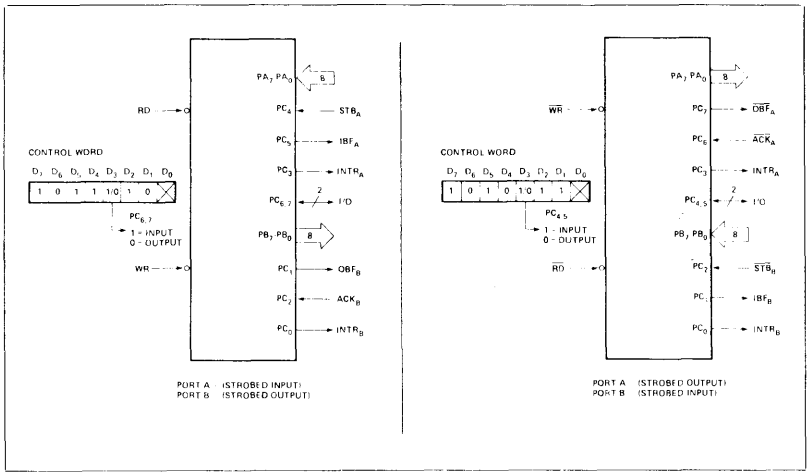


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Ful). The OBF output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input)

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

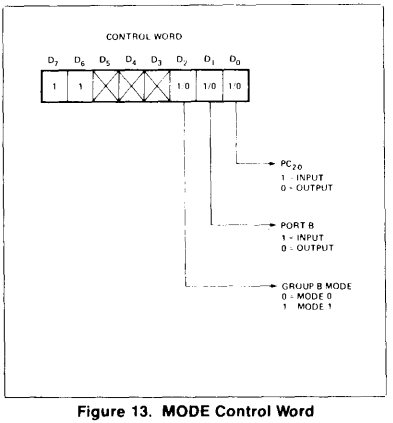


Figure 13. MODE Control Word

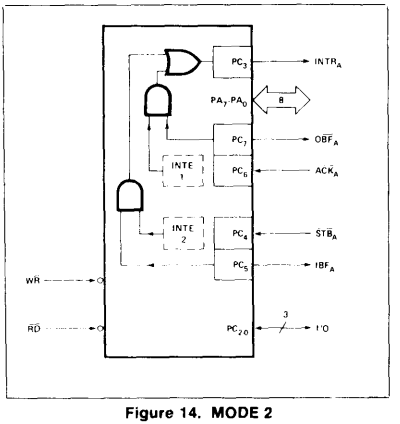


Figure 14. MODE 2

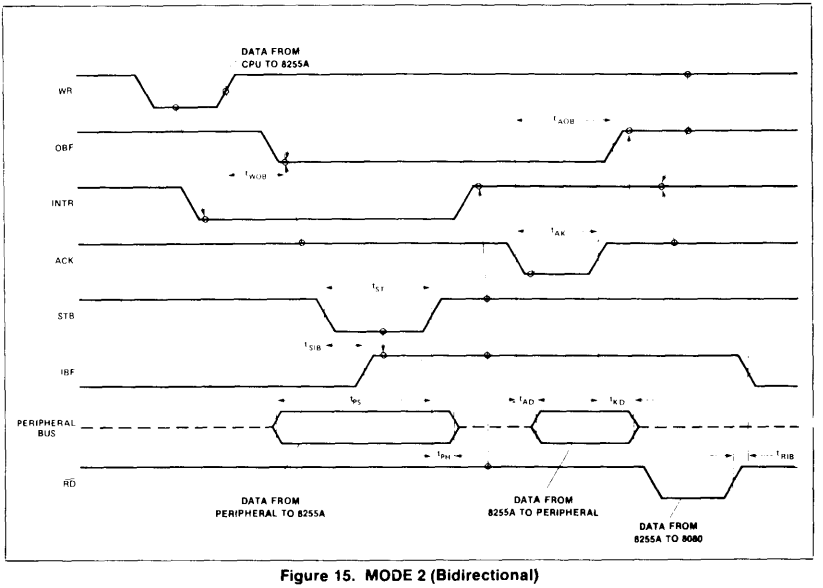


Figure 15. MODE 2 (Bidirectional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

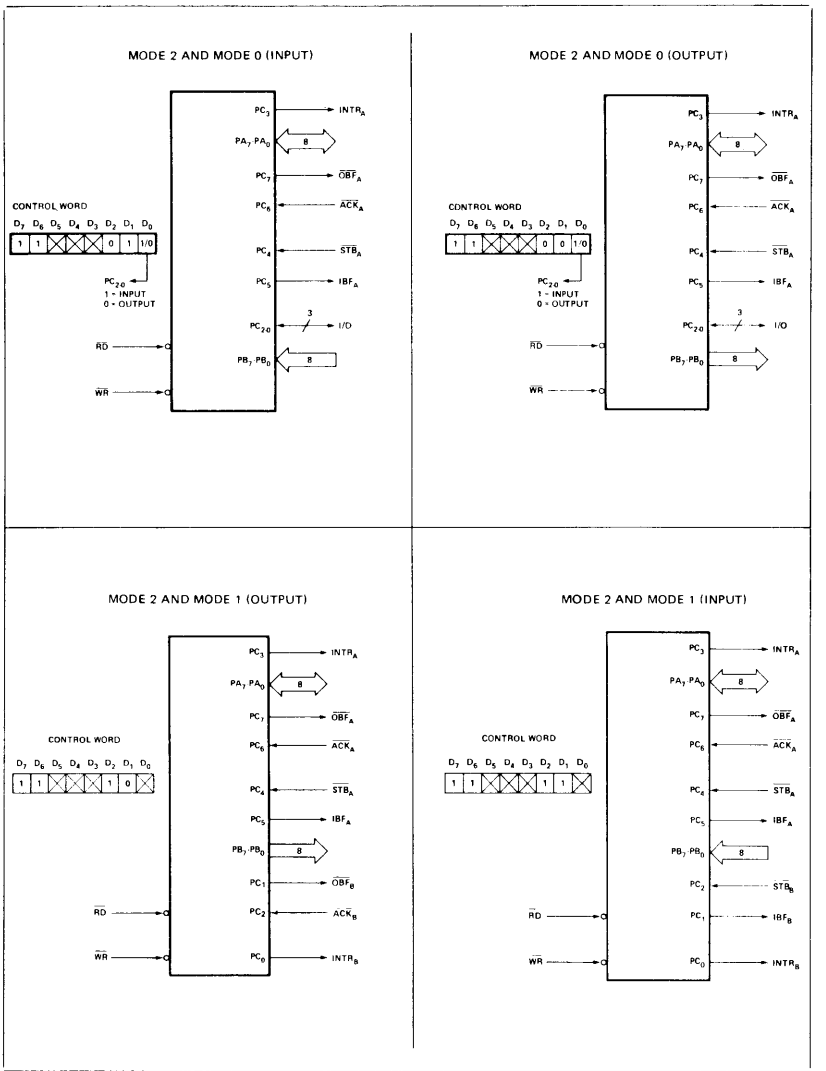


Figure 16. MODE ¼ Combinations

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Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	◄—►	
PA_1	IN	OUT	IN	OUT	◄—►	
PA_2	IN	OUT	IN	OUT	◄—►	
PA_3	IN	OUT	IN	OUT	◄—►	
PA_4	IN	OUT	IN	OUT	◄—►	
PA_5	IN	OUT	IN	OUT	◄—►	
PA_6	IN	OUT	IN	OUT	◄—►	
PA_7	IN	OUT	IN	OUT	◄—►	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs –
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs –
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

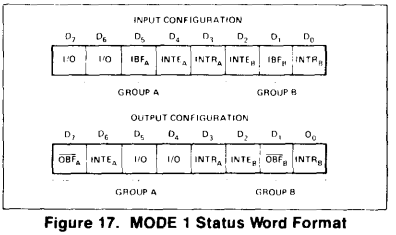


Figure 17. MODE 1 Status Word Format

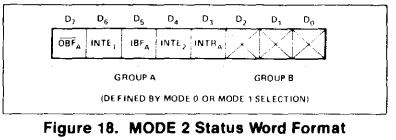


Figure 18. MODE 2 Status Word Format

AFN-00744C

APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 present a few examples of typical applications of the 8255A.

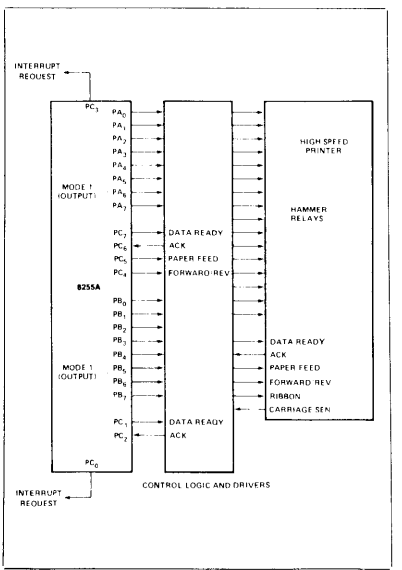


Figure 19. Printer Interface

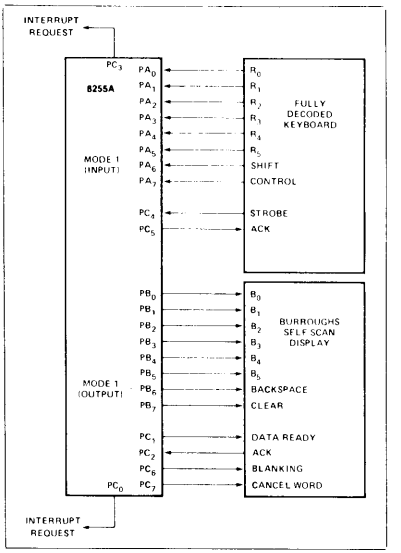


Figure 20. Keyboard and Display Interface

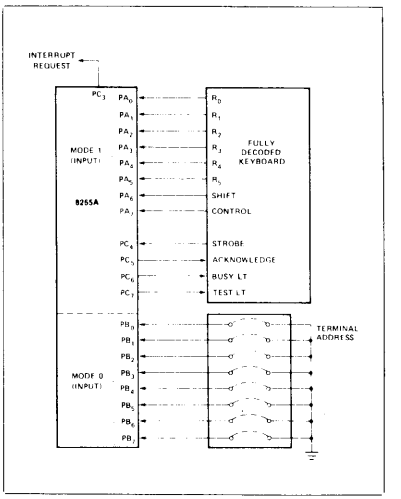


Figure 21. Keyboard and Terminal Address Interface

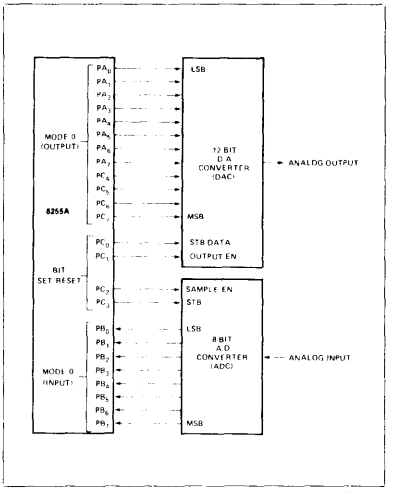


Figure 22. Digital to Analog, Analog to Digital

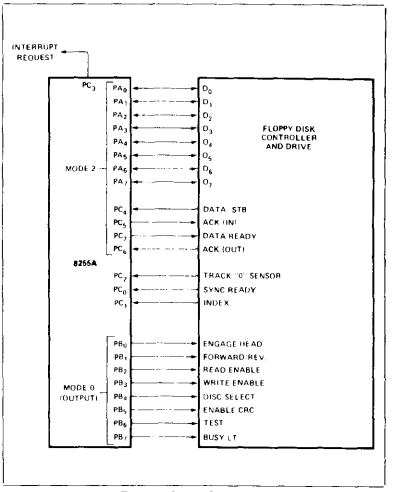


Figure 23. Basic CRT Controller Interface

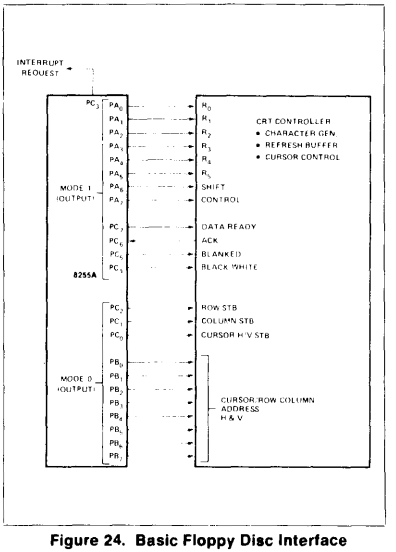


Figure 24. Basic Floppy Disc Interface

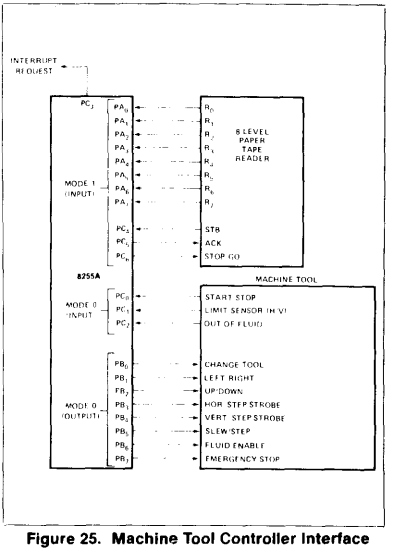


Figure 25. Machine Tool Controller Interface

intel 8255A/8255A-5

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 1 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±10%, GND = 0V)*

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45*	V	I_{OL} = 2.5mA
V_{OL}(PER)	Output Low Voltage (Peripheral Port)		0.45*	V	I_{OL} = 1.7mA
V_{OH}(DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH}(PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω, V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to .45V

NOTE:
1. Available on any 8 pins from Port B and C.

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±10%, GND = 0V)*

Bus Parameters

READ

Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before READ	0		0		ns
t_{RA}	Address Stable After READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid From READ[1]		250		200	ns
t_{DF}	Data Float After READ	10	150	10	100	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		ns

intel 8255A/8255A-5

A.C. CHARACTERISTICS (Continued)

WRITE

Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before WRITE	0		0		ns
t_{WA}	Address Stable After WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid After WRITE	30		30		ns

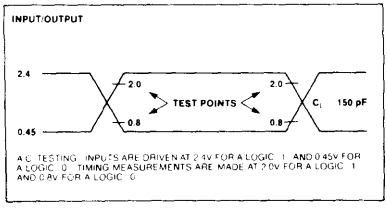
OTHER TIMINGS

Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{WB}	WR = 1 to Output[1]		350		350	ns
t_{IR}	Peripheral Data Before RD	0		0		ns
t_{HR}	Peripheral Data After RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data Before T.E. of STB	0		0		ns
t_{PH}	Per. Data After T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output[1]		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350		350	ns
t_{WIT}	WR = 0 to INTR = 0[1,3]		450		450	ns

NOTES:
1. Test Conditions: C_L = 150 pF.
2. Period of Reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500 ns min.
3. INTR↑ may occur as early as $\overline{WR}$↓.

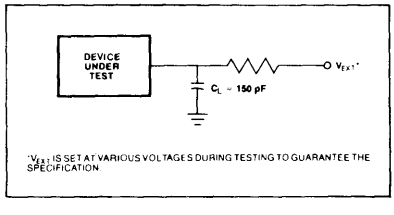
* For Extended Temperature EXPRESS, use M8255A electrical parameters.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

A.C. TESTING LOAD CIRCUIT



*V_{EX1} IS SET AT VARIOUS VOLTAGES DURING TESTING TO GUARANTEE THE SPECIFICATION.

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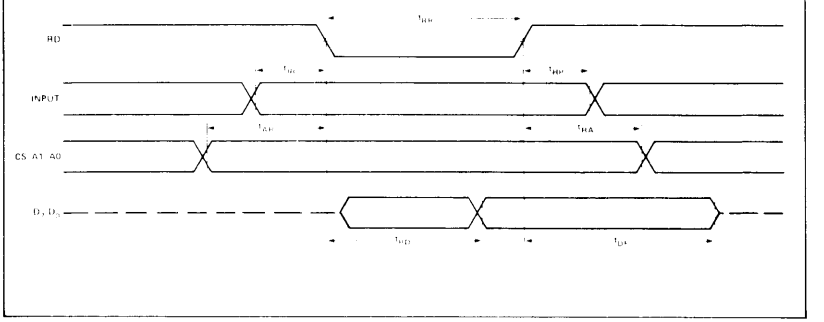
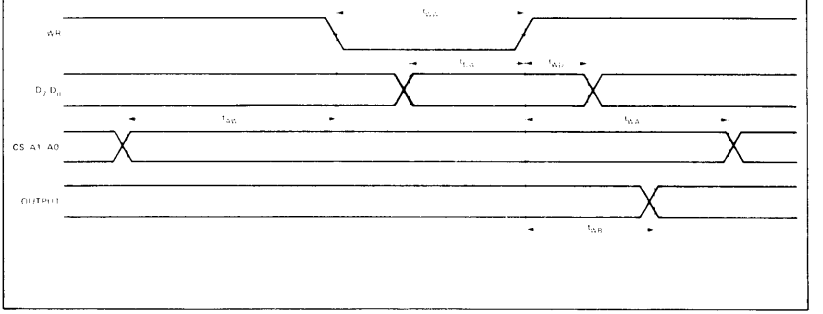
WAVEFORMS

MODE 0 (BASIC INPUT)

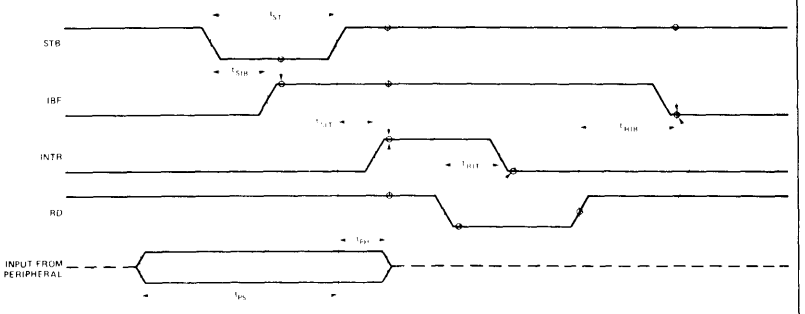


MODE 0 (BASIC OUTPUT)

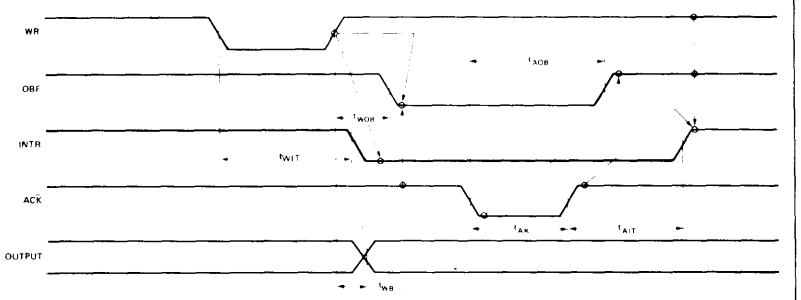


WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)

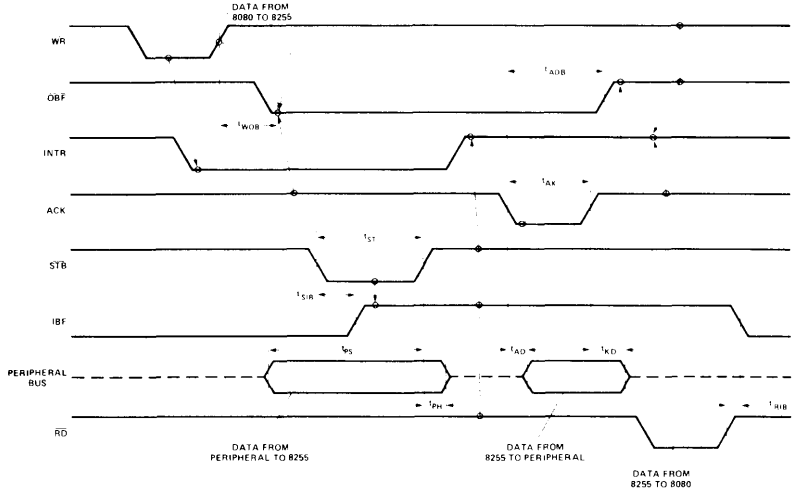


MODE 1 (STROBED OUTPUT)



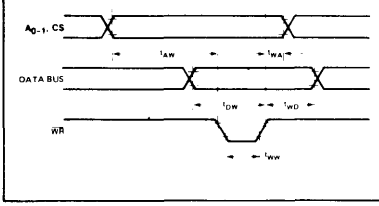
WAVEFORMS (Continued)

MODE 2 (BIDIRECTIONAL)

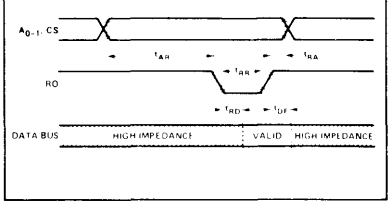


NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

WRITE TIMING



READ TIMING



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intel®

PRELIMINARY

8272A
SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

- **IBM Compatible in Both Single and Double Density Recording Formats**
- **Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector**
- **Multi-Sector and Multi-Track Transfer Capability**
- **Drives Up to 4 Floppy or Mini-Floppy Disks**
- **Data Transfers in DMA or Non-DMA Mode**
- **Parallel Seek Operations on Up to Four Drives**
- **Compatible with all Intel and Most Other Microprocessors**
- **Single-Phase 8 MHz Clock**
- **Single +5 Volt Power Supply (±10%)**

The 8272A is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The 8272A provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Drive Interface. The 8272A is a pin-compatible upgrade to the 8272.

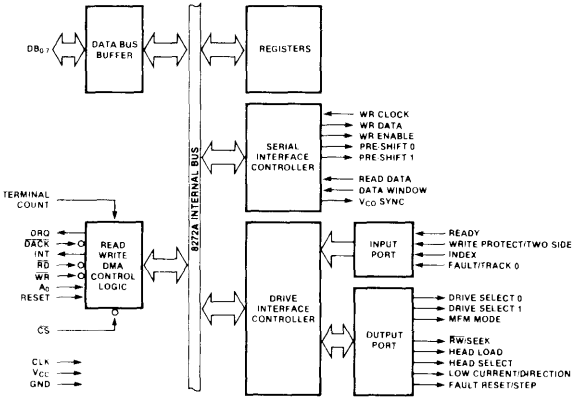

Figure 1. 8272A Internal Block Diagram

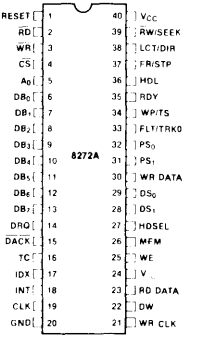

Figure 2. Pin Configuration

ORDER NUMBER 210606-001

intel 8272A PRELIMINARY

Table 1. Pin Description

Symbol	Pin No.	Type	Connection To	Name and Function
$\overline{RESET}$	1	I	μP	**Reset:** Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not clear the last specify command.
$\overline{RD}$	2	I[1]	μP	**Read:** Control signal for transfer of data from FDC to Data Bus, when "0" (low).
$\overline{WR}$	3	I[1]	μP	**Write:** Control signal for transfer of data to FDC via Data Bus, when "0" (low).
$\overline{CS}$	4	I	μP	**Chip Select:** IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
A_0	5	I[1]	μP	**Data/Status Register Select:** Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) contents to be sent to Data Bus.
DB_0-DB_7	6-13	I/O[1]	μP	**Data Bus:** Bidirectional 8-Bit Data Bus.
DRQ	14	O	DMA	**Data DMA Request:** DMA Request is being made by FDC when DRQ = 1.
$\overline{DACK}$	15	I	DMA	**DMA Acknowledge:** DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
TC	16	I	DMA	**Terminal Count:** Indicates the termination of a DMA transfer when "1" (high)[2].
IDX	17	I	FDD	**Index:** Indicates the beginning of a disk track.
INT	18	O	μP	**Interrupt:** Interrupt Request Generated by FDC.
CLK	19	I		**Clock:** Single Phase 8 MHz (4 MHz for mini floppies) Squarewave Clock.
GND	20			**Ground:** D.C. Power Return.
V_{CC}	40			**D.C. Power:** +5V
$\overline{RW}$/SEEK	39	O	FDD	**Read/Write/SEEK:** When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
LCT/DIR	38	O	FDD	**Low Current/Direction:** Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode.
FR/STP	37	O	FDD	**Fault Reset/Step:** Resets fault FF in FDD in Read/Write mode, provides step pulses to move head to another cylinder in Seek mode.
HDL	36	O	FDD	**Head Load:** Command which causes read/write head in FDD to contact diskette.
RDY	35	I	FDD	**Ready:** Indicates FDD is ready to send or receive data. Must be tied high (gated by the index pulse) for mini floppies which do not normally have a Ready line.
WP/TS	34	I	FDD	**Write Protect/Two-Side:** Senses Write Protect status in Read/Write mode, and Two Side Media in Seek mode.
FLT/TRK0	33	I	FDD	**Fault/Track 0:** Senses FDD fault condition in Read/Write mode and Track 0 condition in Seek mode.
PS_1, PS_0	31,32	O	FDD	**Precompensation (preshift):** Write precompensation status during MFM mode. Determines early, late, and normal times.
WR DATA	30	O	FDD	**Write Data:** Serial clock and data bits to FDD.
DS_1, DS_0	28,29	O	FDD	**Drive Select:** Selects FDD unit.
HDSEL	27	O	FDD	**Head Select:** Head 1 selected when "1" (high) Head 0 selected when "0" (low).

Note 1: Disabled when $\overline{CS}$ = 1.
Note 2: TC must be activated to terminate the Execution Phase of any command.

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Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Connection To	Name and Function
MFM	26	O	PLL	**MFM Mode:** MFM mode when "1," FM mode when "0."
WE	25	O	FDD	**Write Enable:** Enables write data into FDD.
VCO	24	O	PLL	**VCO Sync:** Inhibits VCO in PLL when "0" (low), enables VCO when "1."
RD DATA	23	I	FDD	**Read Data:** Read data from FDD, containing clock and data bits.
DW	22	I	PLL	**Data Window:** Generated by PLL, and used to sample data from FDD.
WR CLK	21	I		**Write Clock:** Write data rate to FDD FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM. Must be enabled for all operations, both Read and Write.

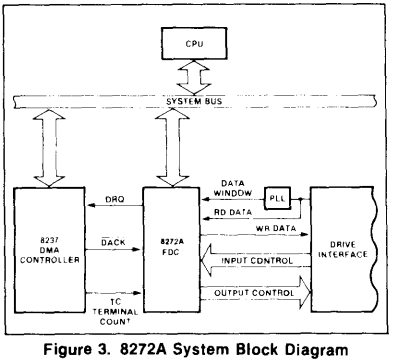

Figure 3. 8272A System Block Diagram

DESCRIPTION

Hand-shaking signals are provided in the 8272A which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the 8237A. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor for every transfer of a data byte between the CPU and the 8272A. In the DMA mode, the processor need only load a command into the FDC and all data transfers occur under control of the 8272A and DMA controller.

There are 15 separate commands which the 8272A will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available.

Read Data	Write Data
Read ID	Format a Track
Read Deleted Data	Write Deleted Data
Read a Track	Seek
Scan Equal	Recalibrate (Restore to Track 0)
Scan High or Equal	Sense Interrupt Status
Scan Low or Equal	Sense Drive Status
Specify	

For more information see the Intel Application Notes AP-116 and AP-121.

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The 8272A offers many additional features such as multiple sector transfers in both read and write modes with a single command, and full IBM compatibility in both single (FM) and double density (MFM) modes.

8272A ENHANCEMENTS

On the 8272A, after detecting the Index Pulse, the VCO Sync output stays low for a shorter period of time. See Figure 4A.

On the 8272 there can be a problem reading data when Gap 4A is 00 and there is no IAM. This occurs on some older floppy formats. The 8272A cures this problem by adjusting the VCO Sync timing so that it is not low during the data field. See Figure 4B.

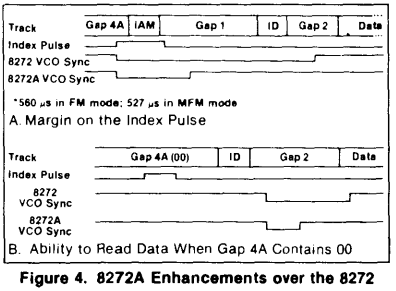

Figure 4. 8272A Enhancements over the 8272

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8272A REGISTERS — CPU INTERFACE

The 8272A contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after execution of a command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and 8272A.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in Table 2.

Table 2. A_0, $\overline{RD}$, $\overline{WR}$ decoding for the selection of Status/Data register functions.

A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal (see note)
0	0	0	Illegal (see note)
1	0	0	Illegal (see note)
1	0	1	Read from Data Register
1	1	1	Write into Data Register

Note: Design must guarantee that the 8272A is not subjected to illegal inputs.

The Main Status Register bits are defined in Table 3.

Table 3. Main Status Register bit description.

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
D_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode.
D_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode.
D_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode.
D_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode.
D_4	FDC Busy	CB	A read or write command is in process.
D_5	Non-DMA mode	NDM	The FDC is in the non-DMA mode. This bit is set only during the execution phase in non-DMA mode. Transition to "0" state indicates execution phase has ended.
D_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
D_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus.

Note: There is a 12μS or 24μS RQM flag delay when using an 8 or 4 MHz clock respectively.

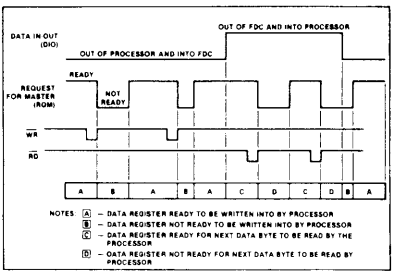

Figure 5. Status Register Timing

The 8272A is capable of executing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the 8272A and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

During Command or Result Phases the Main Status Register (described in Table 3) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the 8272A. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the 8272A. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the 8272A is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the 8272A is in the non-DMA Mode, then the receipt of each data byte (if 8272A is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal (RD = 0) will reset the Interrupt as well as output the Data onto

the Data Bus. For example, if the processor cannot handle Interrupts fast enough (every 13 μs for MFM mode) then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process, then the WR signal performs the reset to the Interrupt signal.

The 8272A always operates in a multi-sector transfer mode. It continues to transfer data until the TC input is active. In Non-DMA Mode, the system must supply the TC input.

If the 8272A is in the DMA Mode, no Interrupts are generated during the Execution Phase. The 8272A generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK} = 0$ (DMA Acknowledge) and a $\overline{RD} = 0$ (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK} = 0$) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The 8272A will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The 8272A contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the 8272A to form the Command Phase, and are read out of the 8272A in the Result Phase, must occur in the order shown in the Table 4. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the 8272A, the Execution Phase

Table 4. 8272A Command Set

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
WRITE DATA										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: 1. Symbols used in this table are described at the end of this section.
2. $A_0 = 1$ for all operations.
3. X = Don't care, usually made to equal binary 0.

Table 4. 8272A Command Set (Continued)

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MFM	SK	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system. FDC reads all of cylinders contents from index hole to EOT
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information during Execution Phase
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire cylinder
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
SCAN HIGH OR EQUAL										
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST 0								Status information at the end of each seek operation about the FDC
	R	PCN								
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT					HUT			
	W	HLT					ND			
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	ST 3								Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	NCN								
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W	Invalid Codes								Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST 0								ST 0 = 80 (16)

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Table 5. Command Mneumonics

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register ($A_0 = 0$) or Data Register ($A_0 = 1$).
C	Cylinder Number	C stands for the current selected Cylinder track number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus where D_7 is the most significant bit, and D_0 is the least significant bit.
DS0, DS1	Drive Select	DS stands for a selected drive number 0 or 1.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number of a Cylinder.
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync Field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HDS	Head Select	HDS stands for a selected head number 0 or 1 (H = HDS in all command words).
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MFM	FM or MFM Mode	If MF is low, FM mode is selected and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed (a cylinder under both HD0 and HD1 will be read or written).
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). The same Stepping Rate applies to all drives (F = 1 ms, E = 2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA), and if STP = 2, then alternate sectors are read and compared.

automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the 8272A is ready for a new command. A command may be aborted by simply sending a Terminal Count signal to pin 16 (TC = 1). This is a convenient means of ensuring that the processor may always get the 8272A's attention even if the disk system hangs up in an abnormal manner.

POLLING FEATURE OF THE 8272A

After power-up RESET, the Drive Select Lines DS0 and DS1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the 8272A polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the 8272A will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the 8272A occurs continuously between instructions, thus notifying the processor which drives are on or off line. Approximate scan timing is shown in Table 6.

Table 6. Scan Timing

DS1	DS0	APPROXIMATE SCAN TIMING
0	0	220μS
0	1	220μS
1	0	220μS
1	1	440μS

COMMAND DESCRIPTIONS

During the Command Phase, the Main Status Register must be polled by the CPU before each byte is written into the Data Register. The DIO (DB6) and RQM (DB7) bits in the Main Status Register must be in the "0" and "1" states respectively, before each byte of the command may be written into the 8272A. The beginning of the execution phase for any of these commands will cause DIO and RQM to switch to "1" and "0" states respectively.

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command must be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 7 on the next page shows the Transfer Capacity.

Table 7. Transfer Capacity

Multi-Track MT	MFM/FM MFM	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to 0FFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 5 shows the values for C, H, R, and N, when the processor terminates the Command.

Table 8. ID Information When Processor Terminates Command

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	LSB	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Notes 1. NC (No Change) The same value as the one at the beginning of command execution.

2. LSB (Least Significant Bit) The least significant bit of H is complemented.

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector

number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same; refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command.

For mini-floppies, multiple track writes are usually not permitted. This is because of the turn-off time of the erase head coils—the head switches tracks before the erase head turns off. Therefore the system should typically wait 1.3 mS before attempting to step or change sides.

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when EOT number of sectors have been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high) and the command is terminated.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the 8272A for each sector on the track. The contents of the R Register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes command termination.

Table 9 shows the relationship between N, SC, and GPL for various sector sizes:

Table 9. Sector Size Relationships.

	8" STANDARD FLOPPY						5¼" MINI FLOPPY					
FORMAT	SECTOR SIZE	N	SC	GPL[1]	GPL[2]	REMARKS	SECTOR SIZE	N	SC	GPL[1]	GPL[2]	
FM Mode	128 bytes/Sector	00	1A	07	1B	IBM Diskette 1	128 bytes/Sector	00	12	07	09	
	256	01	0F	0E	2A	IBM Diskette 2	128	00	10	10	19	
	512	02	08	1B	3A		256	01	08	18	30	
	1024	03	04	47	8A		512	02	04	46	87	
	2048	04	02	C8	FF		1024	03	02	C8	FF	
	4096	05	01	C8	FF		2048	04	01	C8	FF	
MFM Mode	256	01	1A	0E	36	IBM Diskette 2D	256	01	12	0A	0C	
	512	02	0F	1B	54		256	01	10	20	32	
	1024	03	08	35	74	IBM Diskette 2D	512	02	08	2A	50	
	2048	04	04	99	FF		1024	03	04	80	F0	
	4096	05	02	C8	FF		2048	04	02	C8	FF	
	8192	06	01	C8	FF		4096	05	01	C8	FF	

Note: 1. Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

2. Suggested values of GPL in format command.

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 10 shows the status of bits SH and SN under various conditions of SCAN.

Table 10. Scan Status Codes

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors STP = 01, or alternate sectors STP = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC terminates the command.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and performs the following operation if there is a difference:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low) and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

Note that the 8272A Read and Write Commands do not have implied Seeks. Any R/W command should be preceded by: 1) Seek Command; 2) Sense Interrupt Status; and 3) Read ID.

RECALIBRATE

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Table 11. Seek, Interrupt Codes

SEEK END BIT 5	INTERRUPT CODE BIT 6	INTERRUPT CODE BIT 7	CAUSE
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . . FE = 254 ms).

The step rate should be programmed 1 mS longer than the minimum time required by the drive.

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the 8272A during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the 8272A is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80H indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

Table 12. Status Registers

BIT NO.	NAME	SYMBOL	DESCRIPTION
			STATUS REGISTER 0
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt.
D_0	Unit Select 0	US 0	
			STATUS REGISTER 1
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
			STATUS REGISTER 2
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
			STATUS REGISTER 3
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

AFN-01259C

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −40°C to +125°C
All Output Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −0.5 to +7 Volts
Supply Voltage V_{CC} ..... −0.5 to +7 Volts
Power Dissipation ..... 1 Watt

*T_A = 25°C

NOTICE: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −400 μA
I_{CC}	V_{CC} Supply Current		120	mA	
I_{IL}	Input Load Current (All Input Pins)		10 −10	μA μA	V_{IN} = V_{CC} V_{IN} = 0V
I_{LOH}	High Level Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{OFL}	Output Float Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}

CAPACITANCE (T_A = 25°C, f_c = 1 MHz, V_{CC} = 0V)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
$C_{IN(\Phi)}$	Clock Input Capacitance		20	pF	All Pins Except Pin Under Test Tied to AC Ground
C_{IN}	Input Capacitance		10	pF	
$C_{I/O}$	Input/Output Capacitance		20	pF	

A.C. CHARACTERISTICS (T_A0°C to +70°C, V_{CC} = +5.0V ± 10%)

CLOCK TIMING

Symbol	Parameter	Min.	Max.	Unit	Notes
tCY	Clock Period	120	500	ns	Note 5
tCH	Clock High Period	40		ns	Note 4, 5
tRST	Reset Width	14		tCY	

READ CYCLE

tAR	Select Setup to $\overline{RD}$↓	0		ns	
tRA	Select Hold from $\overline{RD}$↑	0		ns	
tRR	$\overline{RD}$ Pulse Width	250		ns	
tRD	Data Delay from $\overline{RD}$↓		200	ns	
tDF	Output Float Delay	20	100	ns	

A.C. CHARACTERISTICS (Continued) (T_A 0°C to +70°C, V_{CC} = +5.0V ±10%)

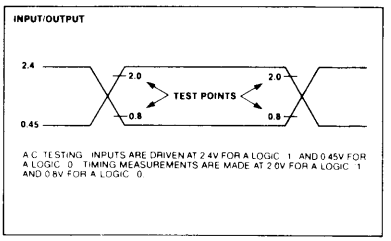
WRITE CYCLE

Symbol	Parameter	Typ.[1]	Min.	Max.	Unit	Notes
tAW	Select Setup to $\overline{WR}$↓		0		ns	
tWA	Select Hold from $\overline{WR}$↑		0		ns	
tWW	$\overline{WR}$ Pulse Width		250		ns	
tDW	Data Setup to $\overline{WR}$↑		150		ns	
tWD	Data Hold from $\overline{WR}$↑		5		ns	
INTERRUPTS						
tRI	INT Delay from $\overline{RD}$↑			500	ns	Note 6
tWI	INT Delay from $\overline{WR}$↑			500	ns	Note 6
DMA						
tRQCY	DRQ Cycle Period		13		µs	Note 6
tAKRQ	$\overline{DACK}$↓ to DRQ↓			200	ns	
tRQR	DRQ↑ to $\overline{RD}$↓		800		ns	Note 6
tRQW	DRQ↑ to $\overline{WR}$↓		250		ns	Note 6
tRQRW	DRQ↑ to $\overline{RD}$↑ or $\overline{WR}$↑			12	µs	Note 6
FDD INTERFACE						
tWCY	WCK Cycle Time	2 or 4 1 or 2			µs	MFM = 0 MFM = 1 Note 2
tWCH	WCK High Time	250	80	350	ns	
tCP	Pre-Shift Delay from WCK↑		20	100	ns	
tCD	WDA Delay from WCK↑		20	100	ns	
tWDD	Write Data Width		tWCH − 50		ns	
tWE	WE↑ to WCK↑ or WE↓ to WCK↓ Delay		20	100	ns	
tWWCY	Window Cycle Time	2 1			µs	MFM = 0 MFM = 1
tWRD	Window Setup to RDD↑		15		ns	
tRDW	Window Hold from RDD↓		15		ns	
tRDD	RDD Active Time (HIGH)		40		ns	
FDD SEEK/DIRECTION/STEP						
tUS	$US_{0,1}$ Setup to $\overline{RW}$/SEEK↑		12		µs	Note 6
tSU	$US_{0,1}$ Hold after $\overline{RW}$/SEEK↓		15		µs	Note 6
tSD	$\overline{RW}$/SEEK Setup to LCT/DIR		7		µs	Note 6
tDS	$\overline{RW}$/SEEK Hold from LCT/DIR		30		µs	Note 6
tDST	LCT/DIR Setup to FR/STEP↑		1		µs	Note 6
tSTD	LCT/DIR Hold from FR/STEP↓		24		µs	Note 6
tSTU	$DS_{2,1}$ Hold from FR/Step↓		5		µs	Note 6
tSTP	STEP Active Time (High)	5			µs	Note 6
tSC	STEP Cycle Time		33		µs	Note 3, 6
tFR	FAULT RESET Active Time (High)		8	10	µs	Note 6
tIDX	INDEX Pulse Width	10			tCY	
tTC	Terminal Count Width		1		tCY	

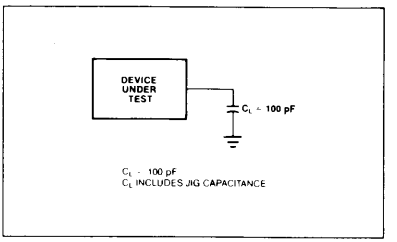
NOTES:

1. Typical values for T_A = 25°C and nominal supply voltage.
2. The former values are used for standard floppy and the latter values are used for mini-floppies.
3. tSC = 33 µs min. is for different drive units. In the case of same unit, tSC can be ranged from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.
4. From 2.0V to +2.0V.
5. At 4 MHz, the clock duty cycle may range from 16% to 76%. Using an 8 MHz clock the duty cycle can range from 32% to 52%. Duty cycle is defined as: D.C. = 100 (tCH − tCY) with typical rise and fall times of 5 ns.
6. The specified values listed are for an 8 MHz clock period. Multiply timings by 2 when using a 4 MHz clock period.

A.C. TESTING INPUT, OUTPUT WAVEFORM

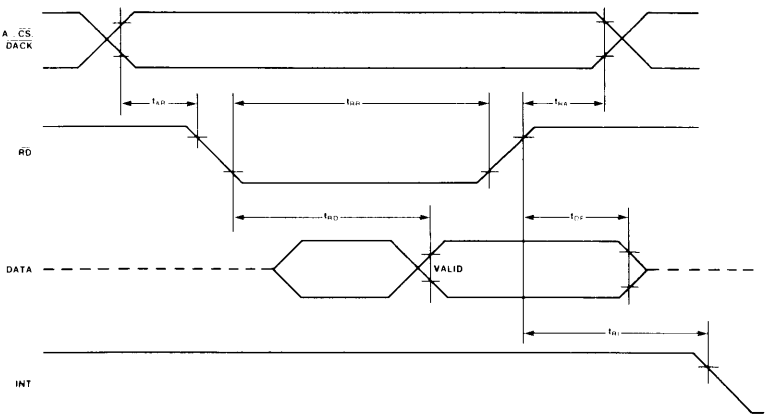


A.C. TESTING LOAD CIRCUIT



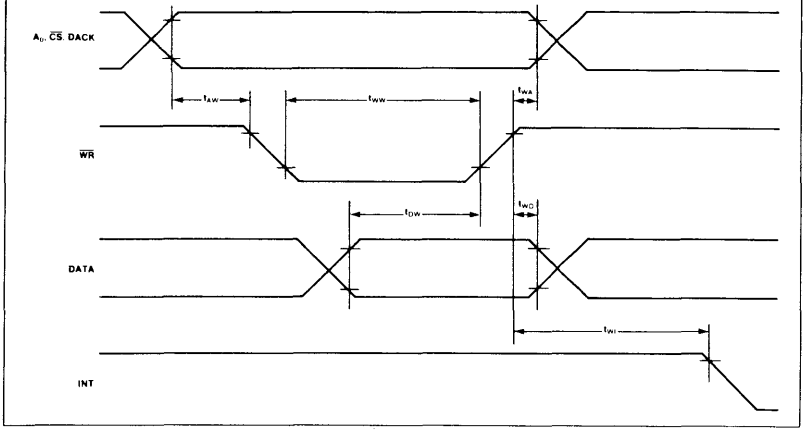
WAVEFORMS

PROCESSOR READ OPERATION

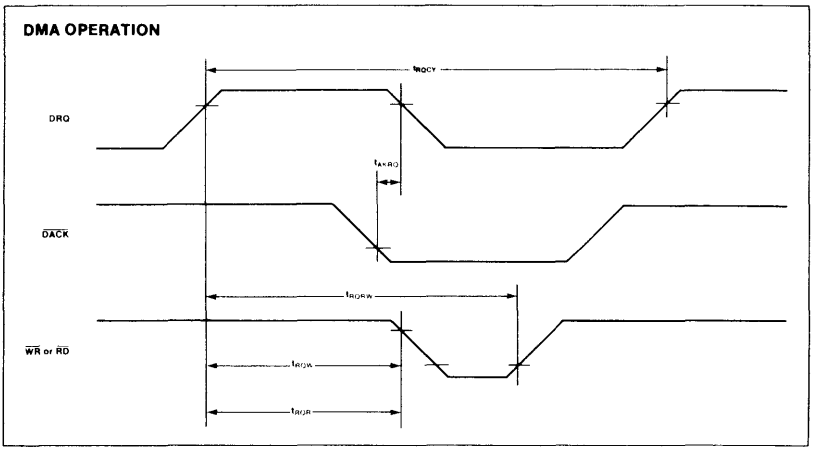


WAVEFORMS (Continued)

PROCESSOR WRITE OPERATION

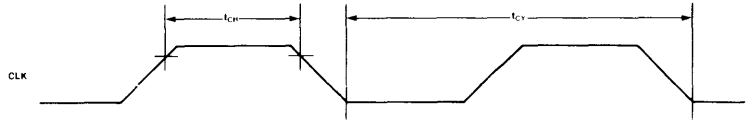


DMA OPERATION

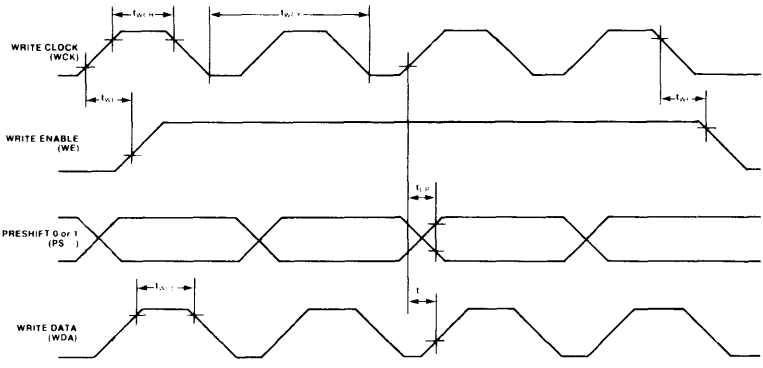


WAVEFORMS (Continued)

CLOCK TIMING



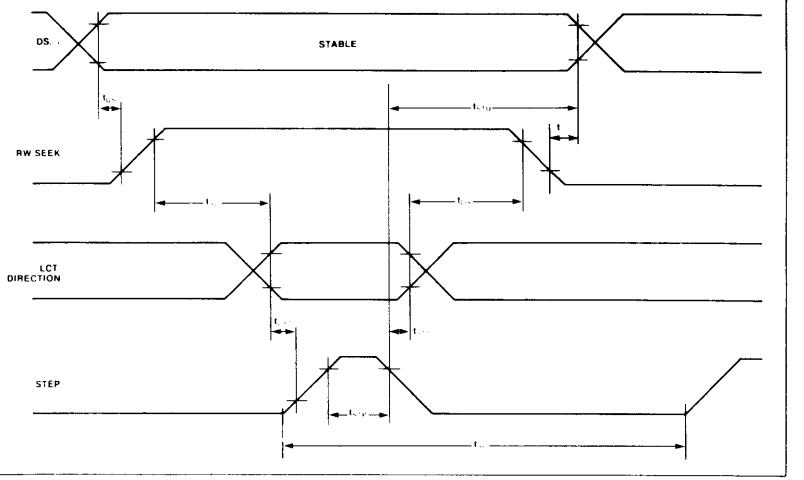
FDD WRITE OPERATION



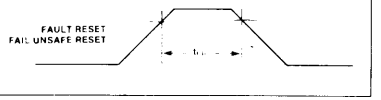
	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

WAVEFORMS (Continued)

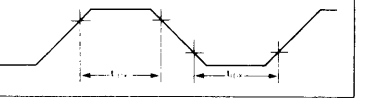
SEEK OPERATION



FLT RESET

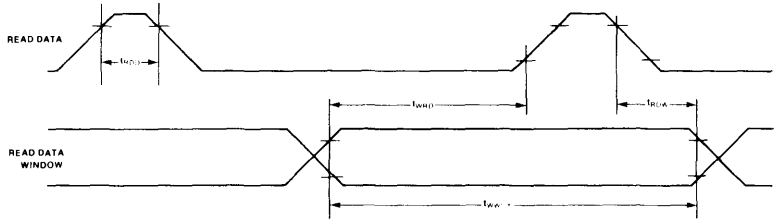


INDEX

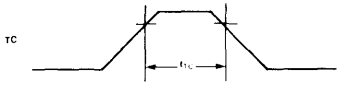


WAVEFORMS (Continued)

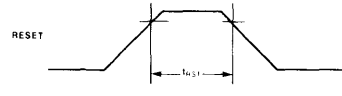
FDD READ OPERATION



TERMINAL COUNT



RESET



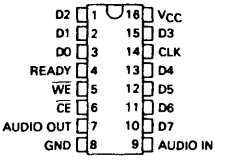
CUSTOM LOGIC CIRCUITS

TYPE SN76494, SN76496 PROGRAMMABLE TONE/NOISE GENERATOR

D2801, NOVEMBER 1983

- Each Circuit Contains 3 Programmable Tone Generators
- Programmable White-Noise Generator
- Programmable Attenuation
- Simultaneous Sounds
- TTL-Compatible
- Up to 500 kHz Clock Input for SN76494 and 4 MHz for SN76496
- External Audio Input for SN76496 May Be Summed with Internally Generated Tones

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

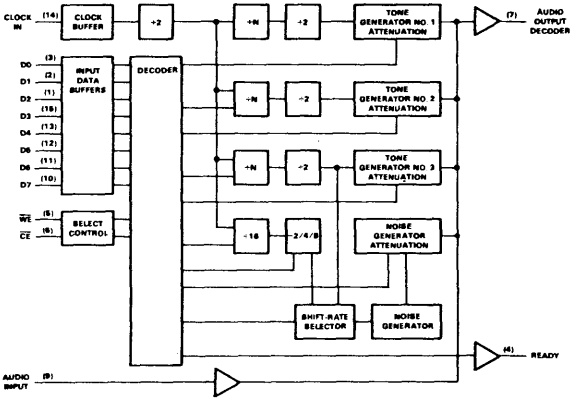
The SN76494 digital complex sound generator is an integrated injection logic (I^2L) tone generator designed to provide low-cost tone or noise generation capability in microprocessor systems. The SN76494 is a data-bus-based input-output peripheral device that interfaces the microprocessor through eight data lines and three control lines.

The SN76494 is identical to the SN76496 except that the maximum clock input frequency for SN76494 is 500 kHz and for SN76496 it is 4 MHz. A "divide-by-eight" stage is deleted from the SN76496 circuitry so that only 4 clock pulses are required to load the data into the SN76494, compared to 32 pulses for the SN76496.

Either of these devices may also be used as a replacment for the SN76489A in all applications if pin 9 is left open or grounded. The output load must be limited to 10 mA.

When audio input is not desired in the SN76494 or SN76496, the audio input pin should be grounded.

functional block diagram



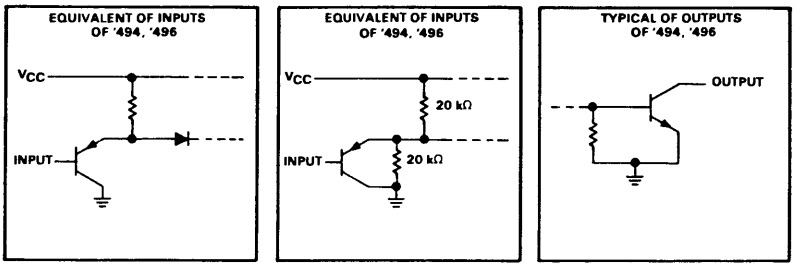
PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS

TYPE SN76494, SN76496
PROGRAMMABLE TONE/NOISE GENERATOR

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 15V
Input voltage, V_I:
Audio input 0.9V
All other inputs 7V
Output current at pin 7 ..... 10 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1150 mW
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

recommended operating conditions

		SN76494			SN76496			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
	Audio input current	0		1.8	0		1.8	mA
V_{OH}	High-level output voltage (pin 4)			5.5			5.5	V
I_{OL}	Low-level output current (pin 4)			2			2	mA
f_{clock}	Input clock frequency			0.5			4	MHz
$t_{d(WE)}$	Delay time, $\overline{CE}$ low to $\overline{WE}$ low	0			0			ns
t_{su}	Setup time, data before $\overline{WE}$↓	0			0			ns
t_h	Holdtime, data after READY 4	0			0			ns
T_A	Operating free-air temperature	0		70	0		70	°C

NOTES: 1 All voltage values are with respect to network ground terminal.
2 For operation above 25°C free-air temperature linearly at the rate of 9.2 mW/°C.

TYPE SN76494, SN76496
PROGRAMMABLE TONE/NOISE GENERATOR

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	High-level output current (pin 4)					10	μA
I_{OL}	Low-level output current (except pin 4)					2	mA
I_I	Input current	$\overline{CE}$ input	V_I = 0 to V_{CC}		-25	-175	μA
		All other inputs			-10	-70	
V_{IB}	Input bias voltage, audio		R= 4.7 kΩ pin 9 to V_{CC}	0.5	0.7	0.9	V
V_{OH}	High-level output voltage (except pin 4)					5.5	V
V_{OL}	Low-level output voltage				0.25	0.4	V
I_{CC}	Supply current				30	50	mA
	Attenuator	2 dB NOM		1	2	3	dB
		4 dB NOM		3	4	5	
		8 dB NOM		7	8	9	
		16 dB NOM		15	16	17	
C_i	Input capacitance					15	pF

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Progagation delay time, high-to-low level READY output from $\overline{CE}$	C_L = 225 pF, R_L = 2 kΩ to V_{CC}		90	150	ns

PARAMETER MEASUREMENT INFORMATION

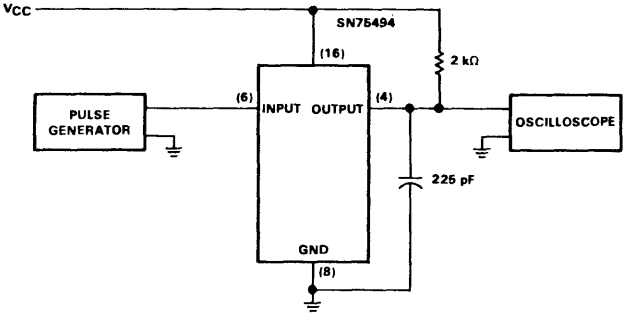


FIGURE 1 - t_{PHL} TEST CIRCUIT

TYPE SN76494, SN76496
PROGRAMMABLE TONE/NOISE GENERATOR

pin assignments and functions

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{CE}$	6	IN	Chip Enable - when active (low) data may be transferred from CPU to the SN76494 or SN76496.
D0 (MSB)	3	IN	D0 through D7 - Input data bus through which the control data is input.
D1	2	IN	
D2	1	IN	
D3	15	IN	
D4	13	IN	
D5	12	IN	
D6	11	IN	
D7 (LSB)	10	IN	
V_{CC}	16	IN	Supply Voltage (5 V nom)
GND	8	OUT	Ground Reference
CLOCK	14	IN	Input Clock
$\overline{WE}$	5	IN	Write Enable - when active (low), $\overline{WE}$ indicates that data is available from the CPU to the SN76494 or SN76496.
READY	4	OUT	When active (high), READY indicates that the data has been read. When READY is low, the microprocessor should enter a wait state until READY is high.
AUDIO IN	9	IN	Audio input from external source
AUDIO OUT	7	OUT	Audio Drive Out

PRINCIPLES OF OPERATION

tone generators

Each tone generator consists of a frequency synthesis section and an attenuation section. The frequency synthesis section requires 10 bits of information (F0-F9) to define half the period of the desired frequency (f). F0 is the most significant bit and F9 is the least significant bit. This information is loaded into a 10-stage tone counter, which counts down at an N/2 rate where N is the input clock frequency. When the tone counter counts down to zero, a borrow signal is produced. This borrow signal toggles the frequency flip-flop and also reloads the tone counter. Thus, the period of the desired frequency is twice the value of the period register.

The frequency can be calculated by the following:

$$f = \frac{N}{4n}$$

where N = clock in Hz
n = 10-bit binary number

The output of the frequency flip-flop feeds into a four stage attenuator. The attenuator values, along with their bit position in the data word, are shown in Table 1. Multiple attenuation control bits may be true simultaneously. Thus, the maximum attenuation is 28 db.

TABLE 1 - ATTENUATION CONTROL

BIT POSITION				WEIGHT
A0	A1	A2	A3	(in dB)
0	0	0	1	2
0	0	1	0	4
0	1	0	0	8
1	0	0	0	16
1	1	1	1	OFF

noise generator

The noise generator consists of a noise source and an attenuator. The noise source is a shift register with an exclusive OR-feedback network. The feedback network has provisions to protect the shift register from being locked in the zero state.

TABLE 2 - NOISE FEEDBACK CONTROL

FEEDBACK	CONFIGURATION
0	"Periodic" noise
1	"White" noise

Whenever the noise control register is changed, the shift register is cleared. The shift register will shift at one of four rates as determined by the two NF bits. The fixed shift rates are derived from the input clock.

TABLE 3 - NOISE GENERATOR FREQUENCY CONTROL

BITS		SHIFT RATE
NF0	NF1	
0	0	N/64
0	1	N/128
1	0	N/256
1	1	Tone generator #3 output

The output of the noise source is connected to a programmable attenuator as shown in Figure 4.

output buffer/amplifier

The output buffer is a conventional operational amplifier summing circuit. It sums the three tone generator outputs, the noise generator output, and any audio input through pin 9. The output buffer will generate up to 10 mA.

To prevent oscillations in the output buffer, the output (pin 7) should be decoupled. This is done by putting 10 ohms in series with 0.1 μF from pin 7 to ground (see figure 3).

data transfer

The microprocessor selects the SN76494 by taking $\overline{CE}$ low (low voltage). Unless $\overline{CE}$ is low, no data transfer can occur. When $\overline{CE}$ is low, the $\overline{WE}$ signal strobes the contents of the data bus to the appropriate control register. The data bus contents must be valid at this time.

The SN76494 requires approximately four clock cycles to load the data into the control register. The SN76496 requires approximately 32 clock cycles. The open-collector READY output is used to synchronize the microprocessor to this transfer and is pulled to the false state (low) immediately following the falling edge of CE. It is required to go to the true state (high) when the data transfer is completed. The data transfer timing is shown below.

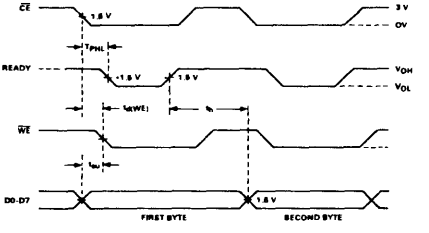


FIGURE 2 - DATA TRANSFER TIMING

TYPE SN76494, SN76496
PROGRAMMABLE TONE/NOISE GENERATOR

TYPICAL APPLICATION DATA

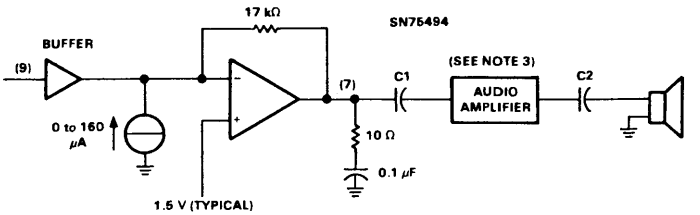


FIGURE 3 - EXTERNAL AUDIO OUTPUT INTERFACE

NOTE 3: The capacitance values of C1 and C2 are determined by the frequency response desired and the audio amplifier used.

TYPE SN76494, SN76496
PROGRAMMABLE TONE/NOISE GENERATOR

TABLE 5 - FUNCTION TABLE

INPUTS		OUTPUT
$\overline{CE}$	$\overline{WE}$	READY
L	L	L
L	H	L
H	L	H
H	H	H

This table is valid when the device is:
(1) not being clocked, and
(2) is initialized by pulling $\overline{WE}$ and $\overline{CE}$ high.

CPU interface to SN76494/SN76496

The microprocessor interfaces with the SN76494 by means of the eight data lines and three control lines ($\overline{WE}$, $\overline{CE}$ and READY). Each tone generator requires 10 bits of information to select the frequency and four bits of information to select the attenuation. A frequency update requires a double-byte transfer, while an attenuator update requires a single-byte transfer.

If no other control registers on the chip are accessed, a tone generator may be rapidly updated by initially sending both bytes of frequency and register data, followed by just the second byte of data for succeeding values. The register address is latched on the chip, so the data will continue going into the same register. This allows the six most significant bits to be quickly modified for frequency sweeps.

control registers

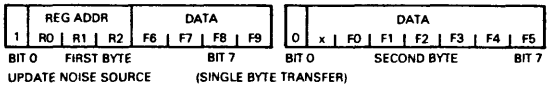
The SN76494 and SN76496 have eight internal registers that are used to control the 3 tone generators and the noise source. During all data transfers to the SN76494 or SN76496, the first byte contains a three-bit field that determines the destination control register. The register address codes are shown in Table 4.

TABLE 4 - REGISTER ADDRESS FIELD

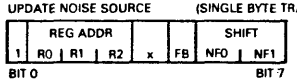
R0	R1	R2	DESTINATION CONTROL REGISTER
0	0	0	Tone 1 Frequency
0	0	1	Tone 1 Attenuation
0	1	0	Tone 2 Frequency
0	1	1	Tone 2 Attenuation
1	0	0	Tone 3 Frequency
1	0	1	Tone 3 Attenuation
1	1	0	Noise Control
1	1	1	Noise Attenuation

data formats

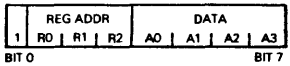
The formats required to transfer data are shown below.



UPDATE NOISE SOURCE (SINGLE BYTE TRANSFER)



UPDATE ATTENUATOR (SINGLE BYTE TRANSFER)



TYPE SN76494, SN76496
PROGRAMMABLE TONE/NOISE GENERATOR

N package

This dual-in-line package consists of a circuit mounted on a 16-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 0.300-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

MOTOROLA Semiconductors
3501 ED BLUESTEIN BLVD. AUSTIN, TEXAS 78721

MC6845

Advance Information

MOS

(N-Channel, Silicon-Gate)

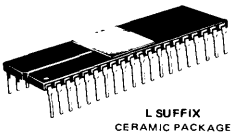
CRT CONTROLLER (CRTC)

CRT CONTROLLER (CRTC)

The MC6845 CRT Controller performs the interface to raster scan CRT displays. It is intended for use in processor-based controllers for CRT terminals in stand-alone or cluster configurations.

The CRTC is optimized for hardware/software balance in order to achieve integration of all key functions and maintain flexibility. For instance, all keyboard functions, R/W, cursor movements, and editing are under processor control; whereas the CRTC provides video timing and Refresh Memory Addressing.

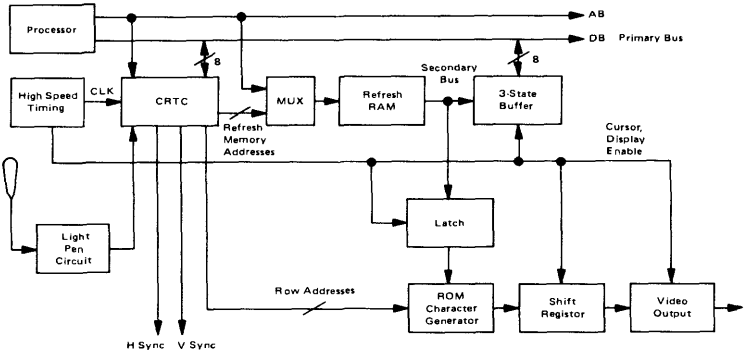
- Applications include "glass-teletype," smart, programmable, intelligent CRT terminals; video games; information display.
- Alphanumeric, semi-graphic, and full graphic capability.
- Fully programmable via processor data bus. Can generate timing for almost any alphanumeric screen density, e.g. 80 x 24, 72 x 64, 132 x 20, etc.
- Single +5 volt supply. TTL/6800 compatible I/O.
- Hardware scroll (paging or by line or by character)
- Compatible with CPU's and MPU's which provide a means for synchronizing external devices.
- Cursor register and compare circuitry.
- Cursor format and blink are programmable.
- Light pen register.
- Line buffer-less operation. No external DMA required. Refresh Memory is multiplexed between CRTC and MPU.
- Programmable interlace or non-interlace scan.
- 14-bit wide refresh address.



L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN:
P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1 – TYPICAL CRT CONTROLLER APPLICATION



AD1-465
(Replaces NP-67)

SYSTEM BLOCK DIAGRAM DESCRIPTION

As shown in Figure 1, the primary function of the CRTC is to generate refresh addresses (MA0-MA13), row selects (RA0-RA4), and video monitor timing (HSYNC, VSYNC) and Display Enable. Other functions include an internal cursor register which generates a Cursor output when its contents compare to the current Refresh Address. A light-pen strobe input signal allows capture of Refresh Address in an internal light pen register.

All timing in the CRTC is derived from the Clk input. In alphanumeric terminals, this signal is the character rate. Character rate is divided down from video rate by external High Speed Timing when the video frequency is greater than 3 MHz. Shift Register, Latch, and MUX Control signals are also provided by external High Speed Timing.

The processor communicates with the CRTC through a buffered 8-bit Data Bus by reading/writing into the 18-register file of the CRTC.

The Refresh Memory address is multiplexed between the Processor and CRTC. Data appears on a Secondary Bus which is buffered from the processor Primary Bus. A number of approaches are possible for solving contentions for the Refresh Memory.

1. Processor always gets priority.
2. Processor gets priority access anytime, but can be synchronized by an interrupt to perform accesses only during horizontal and vertical retrace times.
3. Synchronize processor by memory wait cycles.
4. Synchronize processor to character rate (See Figure 2). The 6800 MPU family lends itself to this configuration because it has constant cycle lengths. This method provides zero burden on the processor because there is never a contention for memory. All accesses are *"transparent."*

The secondary data bus concept in no way precludes using the Refresh RAM for other purposes. It looks like any other RAM to the Processor. For example, using Approach 4, a 64K byte RAM Refresh Memory could perform refresh and program storage functions transparently.

MAXIMUM RATINGS

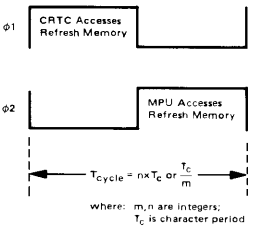
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}*	-0.3 to +7.0	Vdc
Input Voltage	V_{in}*	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

*With respect to V_{SS} (Gnd).

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc
Input High Voltage	V_{IH}	2.0	–	V_{CC}	Vdc

FIGURE 2 – TRANSPARENT REFRESH MEMORY CONFIGURATION TIMING USING 6800 MPU FAMILY



MC6845

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	2.0	–	V_{CC}	Vdc
Input Low Voltage		V_{IL}	-0.3	–	0.8	Vdc
Input Leakage Current		I_{in}	–	1.0	2.5	μAdc
Three-State (V_{CC} = 5.25 V) (V_{in} = 0.4 to 2.4 V)		I_{TSI}	-10	2.0	10	μAdc
Output High Voltage (I_{load} = -205 μA) (I_{load} = -100 μA)	D0-D7 Other Outputs	V_{OH}	2.4 2.4	– –	– –	Vdc
Output Low Voltage (I_{load} = 1.6 mA)		V_{OL}	–	–	0.4	Vdc
Power Dissipation		P_D	–	600	–	mW
Input Capacitance	D0-D7 All others	C_{in}	– –	– –	12.5 10	pF
Output Capacitance	All Outputs	C_{out}	–	–	10	pF
Minimum Clock Pulse Width, Low		P_{WCL}	160	–	–	ns
Minimum Clock Pulse Width, High		P_{WCH}	200	–	–	ns
Clock Frequency		f_c	–	–	2.5	MHz
Rise and Fall Time for Clock Input		t_{cr}, t_{cf}	–	–	20	ns
Memory Address Delay Time		t_{MAD}	–	–	160	ns
Raster Address Delay Time		t_{RAD}	–	–	160	ns
Display Timing Delay Time		t_{DTD}	–	–	300	ns
Horizontal Sync Delay Time		t_{HSD}	–	–	300	ns
Vertical Sync Delay Time		t_{VSD}	–	–	300	ns
Cursor Display Timing Delay Time		t_{CDD}	–	–	300	ns
Light Pen Strobe Minimum Pulse Width		PW_{LPH}	100	–	–	ns
Light Pen Strobe Disable Time		t_{LPD1}	–	–	120	ns
		t_{LPD2}	–	–	0	ns

Note: The light pen strobe must fall to low level before VSYNC pulse rises.

BUS TIMING CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
READ/WRITE				
Enable Cycle Time	t_{cycE}	1.0	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	μs
Setup Time, $\overline{CS}$ and RS valid to enable positive transition	t_{AS}	160	–	ns
Data Delay Time	t_{DDR}	–	320	ns
Data Hold Time (Read) (write)	t_H	10 10	– –	ns
Address Hold Time	t_{AH}	10	–	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	–	25	ns
Data Setup Time	t_{DSW}	195	–	ns
Data Access Time	t_{ACC}	–	480	ns

FIGURE 3 – CRTC TIMING CHART

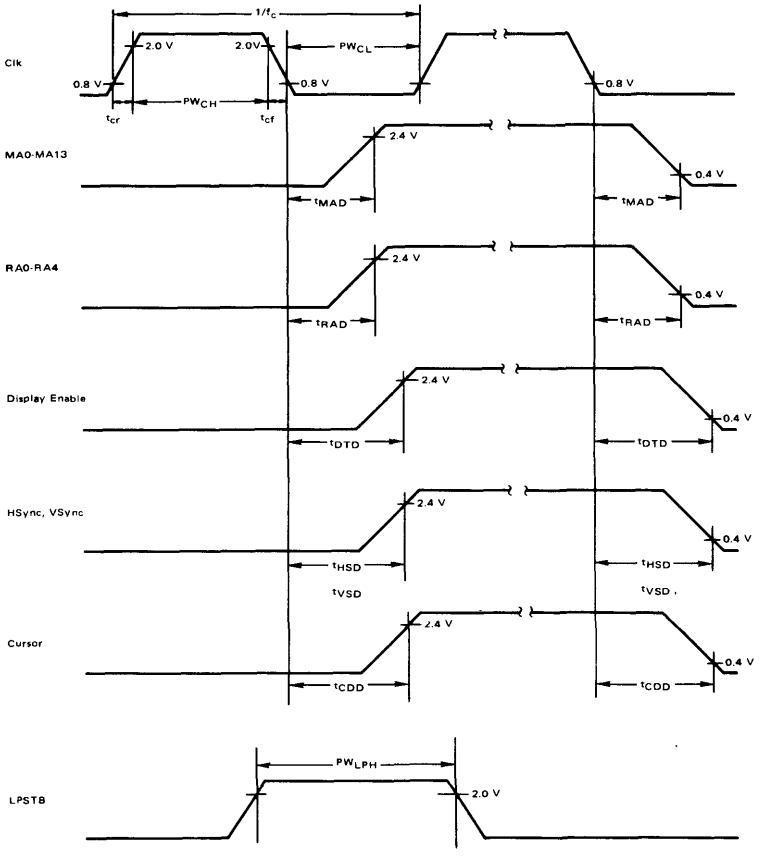


FIGURE 4 – RELATION BETWEEN LPSTB AND REFRESH MEMORY ADDRESS

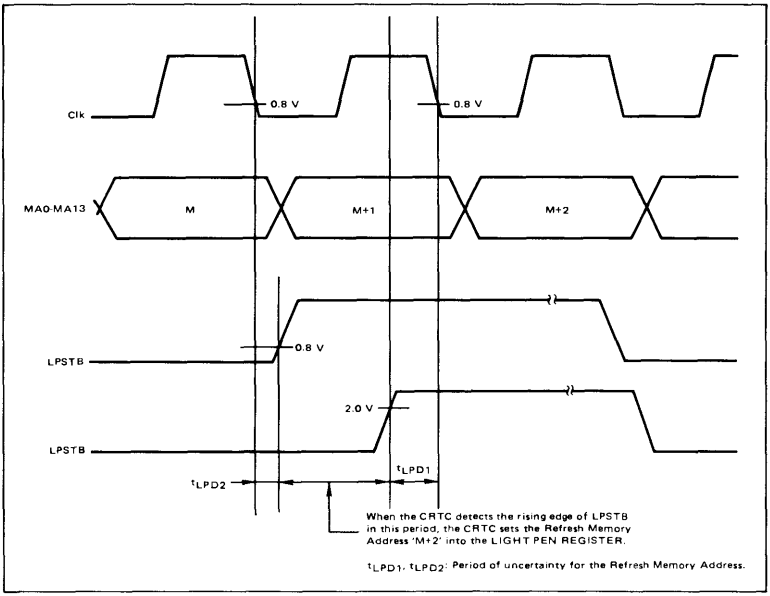
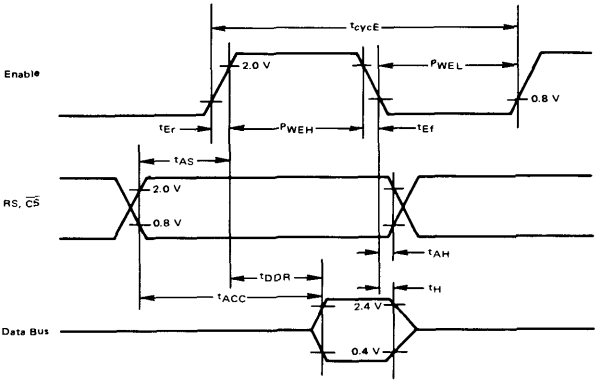


FIGURE 5 – BUS TIMING CHART

5a – Bus Read Timing (Read Information From CRTC)



5b – Bus Write Timing (Write Information Into CRTC)

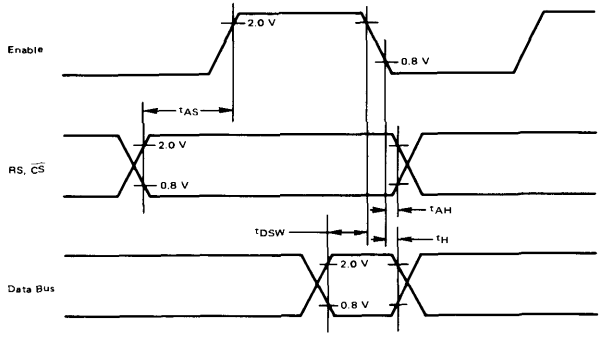


FIGURE 6 – BUS TIMING TEST LOAD

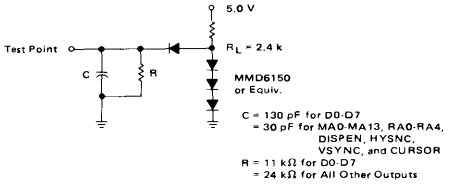
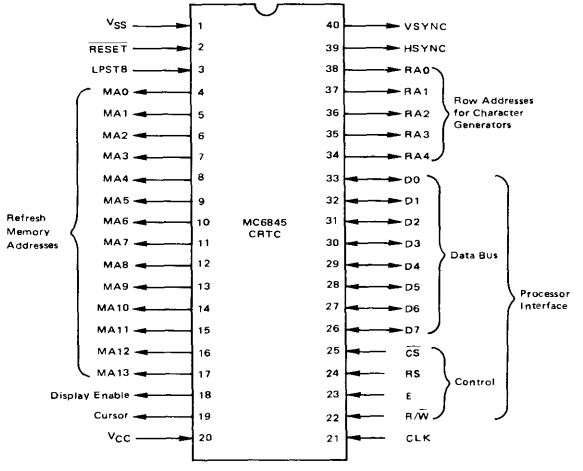


FIGURE 7 – PIN ASSIGNMENT



PIN DESCRIPTION

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the bidirectional data bus (D0-D7) using $\overline{CS}$, RS, E, and R/$\overline{W}$ for control signals.

Data Bus (D0-D7) – The bidirectional data lines (D0-D7) allow data transfers between the CRTC internal Register File and the processor. Data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a CRTC read operation. A high level on a data pin is a logical "1."

Enable (E) – The Enable signal is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock, and the high to low transition is the active edge.

Chip Select ($\overline{CS}$) – The $\overline{CS}$ line is a high impedance TTL/MOS compatible input which selects the CRTC when low to read or write the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS) – The RS line is a high impedance TTL/MOS compatible input which selects either the Address Register (RS = "0") or one of the Data Registers (RS = "1") of the internal Register File.

Read/Write (R/$\overline{W}$) – The R/$\overline{W}$ line is a high impedance TTL/MOS compatible input which determines whether the internal Register File gets written or read. A write is active low ("0").

CRT CONTROL

The CRTC provides horizontal sync (HS), vertical sync (VS), and Display Enable signals.

Vertical Sync (V SYNC) – This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the vertical position of the displayed text.

Horizontal Sync (H SYNC) – This TTL compatible output is an active high signal which drives the monitor directly or is fed to Video Processing Logic for composite generation. This signal determines the horizontal position of the displayed text.

Display Enable – This TTL compatible output is an active high signal which indicates the CRTC is providing addressing in the active Display Area.

REFRESH MEMORY/CHARACTER GENERATOR ADDRESSING

The CRTC provides Memory Addresses (MA0-MA13) to scan the Refresh RAM. Also provided are Raster Addresses (RA0-RA4) for the character ROM.

Refresh Memory Addresses (MA0-MA13) – These 14 outputs are used to refresh the CRT screen with pages of data located within a 16K block of refresh memory. These outputs drive a TTL load and 30pF. A high level on MA0-MA13 is a logical "1."

Raster Addresses (RA0-RA4) – These 5 outputs from the internal Raster Counter address the Character ROM for the row of a character. These outputs drive a TTL load and 30pF. A high level (on RA0-RA4) is a logical "1."

OTHER PINS

Cursor – This TTL compatible output indicates Cursor Display to external Video Processing Logic. Active high signal.

Clock (CLK) – The CLK TTL/MOS compatible input is used to synchronize all CRT control signals. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high to low.

Light Pen Strobe (LPSTR) – This high impedance TTL/MOS compatible input latches the current Refresh Addresses in the Register File. Latching is on the low to high edge and is synchronized internally to character clock.

V_{CC}, Gnd

$\overline{RES}$ – The $\overline{RES}$ input is used to Reset the CRTC. An input low level on $\overline{RES}$ forces CRTC into following status:

(A) All the counters in CRTC are cleared and the device stops the display operation.
(B) All the outputs go down to low level.
(C) Control registers in CRTC are not affected and remain unchanged.

This signal is different from other M6800 family in the following functions:

(A) $\overline{RES}$ signal has capability of reset function only when LPSTB is at low level.
(B) After $\overline{RES}$ has gone down to low level, output signals of MA0-MA13 and RA0-RA4, synchronizing with CLK low level, goes down to low level. (At least 1 cycle CLK signal is necessary for reset.)
(C) The CRTC starts the Display operation immediately after the release of $\overline{RES}$ signal.

TABLE 1 – CRTC Operating Mode

$\overline{RES}$	LPSTB	OPERATING MODE
0	0	Reset
0	1	Test Mode
1	0	Normal Mode
1	1	Normal Mode

REGISTER FILE DESCRIPTION
(See Table 2)

Nineteen registers in the CRTC can be accessed by means of the data bus. Register addressing and lengths are shown in Table 2.

ADDRESS REGISTER

The Address Register is a 5 bit write-only register used as an "indirect" or "pointer" register. Its contents are the address of one of the other 18 registers in the file. When RS and $\overline{CS}$ are low, the Address Register itself is addressed. When RS is high, the Register File is accessed.

HORIZONTAL TIMING REGISTERS R0, R1, R2, and R3

Figure 9 shows the visible display area of a typical CRT monitor giving the point of reference for horizontal registers as the left most displayed character position. Horizontal registers are programmed in "character time" units with respect to the reference.

Horizontal Total Register (R0) – This 8 bit write-only register determines the horizontal frequency of HS. It is the total of displayed plus non-displayed character time units minus one.

Horizontal Displayed Register (R1) – This 8 bit write-only register determines the number of displayed characters per horizontal line.

Horizontal Sync Position Register (R2) – This 8 bit write-only register determines the horizontal sync postiion on the horizontal line.

Horizontal Sync Width Register (R3) – This 4 bit write-only register determines the width of the HS pulse. It may not be apparent why this width needs to be programmed. However, consider that all timing widths must be programmed as multiples of the character clock period which varies. If HS width were fixed as an integral number of character times, it would vary with character rate and be out of tolerance for certain monitors. The rate programmable feature allows compensating HS width.

VERTICAL TIMING REGISTERS R4, R5, R6, R7, R8, and R9

The point of reference for vertical registers is the top character position displayed. Vertical registers are programmed in character row times or scan line times.

Vertical Total Register (R4) and Vertical Total Adjust Register (R5) – The vertical frequency of VS is determined by both R4 and R5. The calculated number of character line times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of character line times minus one is programmed in the 7 bit write-only Vertical Total Register; the fraction is programmed in the 5 bit write-only Vertical Scan Adjust Register as a number of scan line times.

Vertical Displayed Register (R6) – This 7 bit write-only register determines the number of displayed character rows on the CRT screen, and is programmed in character row times.

Vertical Sync Position (R7) – This 7 bit write-only register determines the vertical sync position with respect

TABLE 2 – CRTC INTERNAL REGISTER ASSIGNMENT

	$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
	1	X	X	X	X	X	X	X	–	–	–	–								
	0	0	X	X	X	X	X	X	Address Register	–	No	Yes								
	0	1	0	0	0	0	0	R0	Horizontal Total	Char.	No	Yes								
	0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
	0	1	0	0	0	1	0	R2	H. Sync Position	Char.	No	Yes								
	0	1	0	0	0	1	1	R3	H. Sync Width	Char.	No	Yes								
	0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes								
	0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
	0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes								
	0	1	0	0	1	1	1	R7	V. Sync Position	Char. Row	No	Yes								
W	0	1	0	1	0	0	0	R8	Interlace Mode	–	No	Yes								
	0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
	0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes		B	P				(Note 1)	
	0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes								
	0	1	0	1	1	0	0	R12	Start Address (H)	–	No	Yes								
	0	1	0	1	1	0	1	R13	Start Address (L)	–	No	Yes								
	0	1	0	1	1	1	0	R14	Cursor (H)	–	Yes	Yes								
	0	1	0	1	1	1	1	R15	Cursor (L)	–	Yes	Yes								
	0	1	1	0	0	0	0	R16	Light Pen (H)	–	Yes	No								
	0	1	1	0	0	0	1	R17	Light Pen (L)	–	Yes	No								

Note (1): Bit 5 of the Cursor Start Raster Register is used for blink period control, and Bit 6 is used to select blink or non-blink.

to the reference. It is programmed in character row times.

Interlace Mode Register (R8) – This 2 bit write-only register controls the raster scan mode (see Figure 11). When bit 0 and bit 1 are reset, or bit 0 is reset and bit 1 set, the non-interlace raster scan mode is selected. Two interlace modes are available. Both are interlaced 2 fields per frame. When bit 0 is set and bit 1 is reset, the interlace sync raster scan mode is selected. Also when bit 0 and bit 1 are set, the interlace sync and video raster scan mode is selected.

Maximum Scan Line Address Register (R9) – This 5 bit write-only register determines the number of scan lines per character row including spacing. The programmed value is a max address and is one less than the number of scan lines.

OTHER REGISTERS

Cursor Start Register (R10) – This 7 bit write-only register controls the cursor format (see Figure 10). Bit 5 is the blink timing control. When bit 5 is low, the blink frequency is 1/16 of the vertical field rate, and when bit 5 is high, the blink frequency is 1/32 of the vertical field rate. Bit 6 is used to enable a blink. The cursor start scan line is set by the lower 5 bits.

Cursor End Register (R11) – This 5 bit write-only register sets the cursor end scan line.

Start Address Register (H & L) (R12, R13) – Start Address Register is a 14 bit write-only register which determines the first address put out as a refresh address after vertical blanking. It consists of an 8 bit lower register, and a 6 bit higher register.

Light Pen Register (H & L) (R16, R17) – This 14 bit read-only register is used to store the contents of the Address Register (H & L) when the LPSTB input pulses high. This register consists of an 8 bit lower and 6 bit higher register.

Cursor Register (H & L) (R14, R15) – This 14 bit read/write register stores the cursor location. This register consists of an 8 bit lower and 6 bit higher register.

CURSOR

The Cursor Start and End Registers allow a cursor of up to 32 scan lines in height to be placed on any scan lines of the character block as shown in Figure 10. Using Bits 5 & 6 of the Cursor Start Register, the cursor is programmed with blink periods of 16 or 32 times the field period. Optional non-blink and non-display modes can also be selected. When an external 2X blink on characters is required, it may be necessary to perform cursor blink externally as well so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRTC for blinking cursor and externally inverting the video signal with an exclusive-OR.

The cursor is positioned by changing the contents of registers R14 and R15. The cursor can be placed at any of 16K character positions, thus facilitating hardware paging and scrolling through memory without loss of the cursor's original position.

INTERLACE/NON-INTERLACE DISPLAY MODES

An illustration of the 3 raster scan modes of operation is shown in Figure 11. Normal sync mode is non-interlace. In this mode, each scan line is refreshed at the vertical field rate (e.g., 50 or 60 Hz). Frame time is divided into even and odd alternating fields. The horizontal and vertical timing relationship results in the displacement of scan lines in the odd field with respect to the even field. When the same information is painted in both fields, the mode is called "Interlace Sync;" this is a useful mode for enhancing readability by filling in a character. When the even lines of a character are displayed in the even field and the odd lines in the odd field, the mode is called "Interlace Sync and Video." This last mode effectively doubles the character density on a monitor of a given bandwidth. The disadvantage of both interlace modes is an apparent flicker effect, which can be reduced by careful monitor design.

There are restrictions on the programming of CRTC registers for interlace operation:

1) Horizontal total character count, N_{ht} must be odd (i.e., an even number of character times)
2) For Interlace Sync and Video mode only, the max scan line address, N_{sl}, must be odd (i.e., an even number of scan lines)
3) For Interlace Sync and Video mode only, the Vertical Displayed Total characters must be even. The programmed number, N_{vd}, must be *one-half* the actual number required.
4) For Interlace Sync & Video mode only, the Cursor START and Cursor End Registers must both be even or both odd.

LIGHT PEN

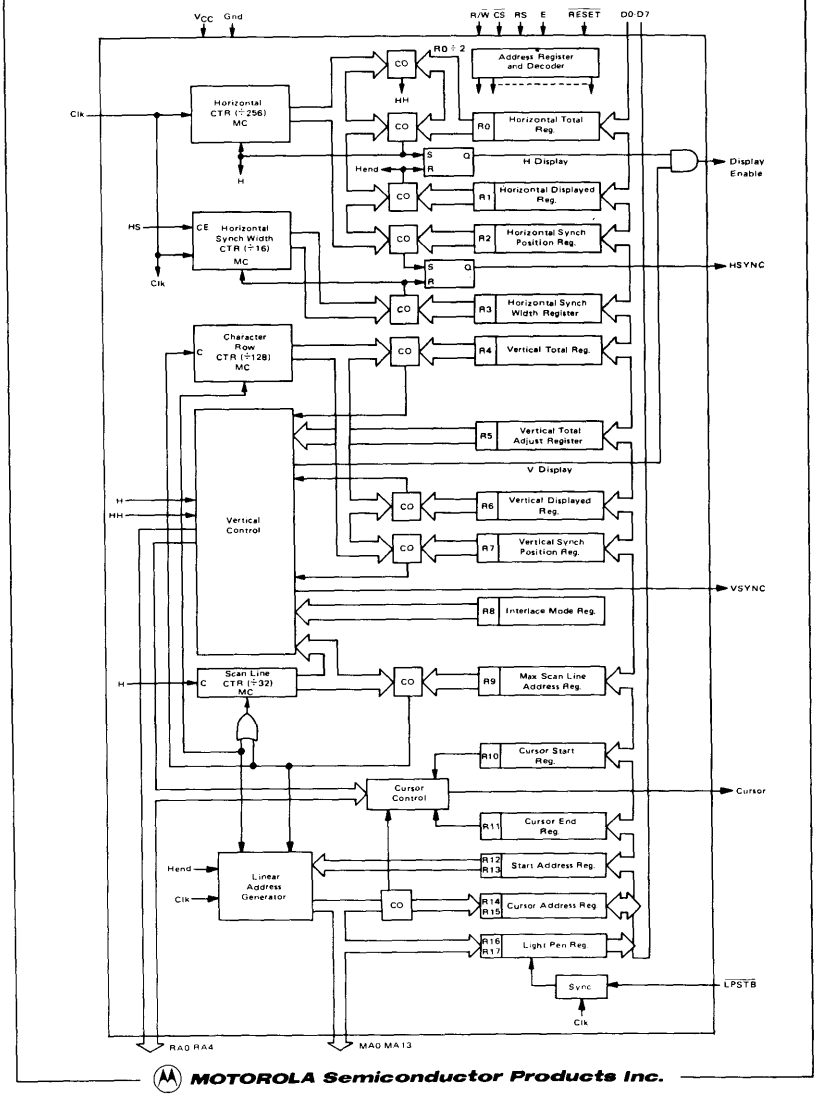
The contents of the CRTC Address Counter are strobed into R16/R17 Light Pen Registers on the next high to low CLK transition after LPSTB goes high. In most systems, the light pen signal would also cause a processor interrupt routine to read R16/R17. Slow light pen response requires the processor software to modify the captured address read from R16/R17 by a calibration factor.

PROGRAMMING CONSIDERATIONS

Initialization – Registers R0-R15 must be initialized after power is turned on. The processor normally loads the CRTC registers sequentially from a firmware table. Henceforth, R0-R11 are not changed in most systems. The 6800 program in Table 3 and Figure 12 shows a typical CRTC initialization.

Hardware Scrolling – Registers R12/R13 contents determine which memory location is the first displayed character on the screen. Since the CRTC Linear Address Generator counts from this beginning count, the displayed portion of the screen may be a window on any continuous string of characters within a 16K block or refresh memory. By centering the R12/R13 pointer in the middle of the available memory space, scrolling up or down is possible . . . by line, page, or character.

FIGURE 8 – CRTC FUNCTIONAL BLOCK DIAGRAM



MOTOROLA Semiconductor Products Inc.

CRTC DESCRIPTION
(Figure 8: CRTC Block Diagram)

The CRTC consists of programmable horizontal and vertical timing generators, programmable linear address register, programmable cursor logic, light pen capture register, and control circuitry for interface to a processor bus.

All CRTC timing is derived from CLK, usually the output of an external dot rate counter. Coincidence (CO) circuits continuously compare counter contents to the contents of the programmable register file, R0-R17. For horizontal timing generation, comparisons result in: 1) Horizontal sync pulse (HS) of a frequency, position, and width determined by the registers, 2) Horizontal Display Signal of a frequency, position, and duration determined by the registers.

The Horizontal counter produces H clock which drives the Scan Line Counter and Vertical Control. The contents of the Raster Counter are continuously compared to the Max Scan Line Address Register. A coincidence resets the Raster Counter and clocks the Vertical Counter.

Comparisons of Vertical Counter contents and Vertical Registers result in: 1) Vertical sync pulse (VS) of a frequency and positon determined by the registers—the width is fixed at 16 raster lines in the vertical control section and is not programmable, 2) Vertical Display of a frequency and position determined by the registers.

The Vertical Control Logic has other functions.

1. Generate row selects, RA0-RA4, from the Raster Count for the corresponding interlace or non-interlace modes.
2. Extend the number of scan lines in the vertical total by the amount programmed in the Vertical Total Adjust Register.

The Linear Address Generator is driven by CLK and locates the relative positions of characters in memory with their positions on the screen. Fourteen lines, MA0-MA13, are available for addressing up to four pages of 4K characters, 8 pages of 2K characters, etc. Using the Start Address Register, hardware scrolling through 16K characters is possible. The Linear Address Generator repeats the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and blinking rate on the screen. All are programmable.

The light pen strobe going high causes the current contents of the Address Counter to be latched in the Light Pen Register. The contents of the Light Pen Register are subsequently read by the Processor.

Internal CRTC registers are programmed by the processor through the data bus, D0-D7, and the control signals—R/$\overline{W}$, $\overline{CS}$, RS and E.

FIGURE 9 – ILLUSTRATION OF THE CRT SCREEN FORMAT

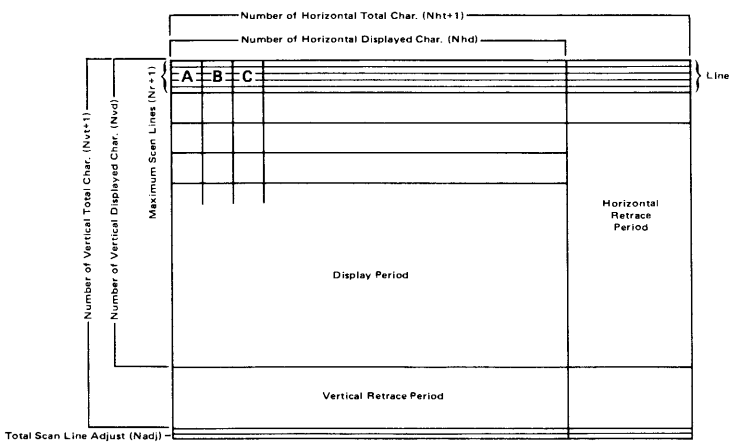
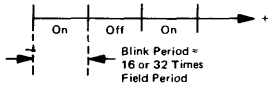


FIGURE 10 – CURSOR CONTROL

Cursor Start Register

B Bit 6	P Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate



Example of Cursor Display Mode

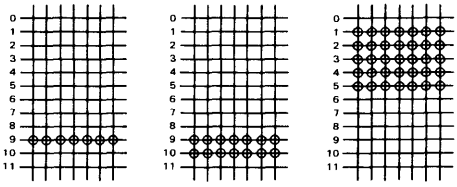
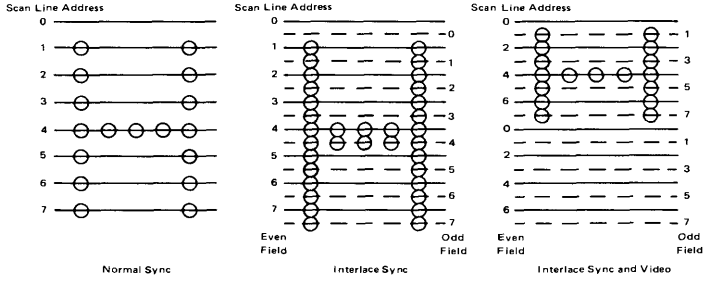


FIGURE 11 – INTERFACE CONTROL

Interlace Mode Register

Bit 1	Bit 0	Mode
0	0	Normal Sync Mode (Non-Interlace)
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode



MC6845

TABLE 3 – Typical 80 x 24 Screen Format Initialization of CRTC

Reg. #	Register File	Program Unit	Calculation*	Programmed Value	
				Decimal	Hex
R0	H Total	T_c	102 x .527 = 53.76 µs	102 - 1 = 101	N_{ht} = $65
R1	H Displayed	T_c	80 x .527 = 42.16 µs	80	N_{hd} = $50
R2	H Sync Position	T_c	86 x .527 = 45.32 µs	86	N_{hsp} = $56
R3	H Sync Width	T_c	9 x .527 = 4.74 µs	9	N_{hsw} = $09
R4	V Total	T_{cr}	25 x 645.12 = 16.13 ms	25 - 1 = 24	N_{vt} = $18
R5	V Total Adjust	T_{sl}	10 x 53.76 = 54 ms	10	N_{adj} = $0A
R6	V Displayed	T_{cr}	24 x 645.12 = 15.48 ms	24	N_{vd} = $18
R7	V Sync Position	T_{cr}	24 x 645.12 = 15.48 ms	24	N_{vsp} = $18
R8	Interlace Mode	–		–	$00
R9	Max Scan Line Address	T_{sl}		11	N_{sl} = $0B
R10	Cursor Start	T_{sl}		0	$00
R11	Cursor End	T_{sl}		11	$0B
R12	Start Address (H)	–		128	$00
R13	Start Address (L)	–			$80
R14	Cursor (H)	–		128	$00
R15	Cursor (L)	–			$80

Clock Period = T_c = .527 µs

Scan Line Period = T_{sl} = $(N_{ht} + 1) \times T_c$ = 102 x .527 µs = 53.76 µs

Character Row Period = $T_{cr} = N_{sl} \times T_{sl}$ = 12 x 53.76 µs = 645.12 µs

*These are typical values for the Motorola M3000 Monitor; values may vary for other monitors.

FIGURE 12 – INITIALIZATION OF CRTC FOR 80x24 SCREEN FORMAT IN TABLE 3

```
PAGE  001   CRTINT

00001                          NAM     CRTINT
00002 0000                     ORG     $0
00003 0000 5F                  CLR B                 CLEAR COUNTER
00004 0001 CE 0020             LDX     #$20
00005 0004 F7 9000 CRTII       STA B   $9000         CRTC ADDR REG
00006 0007 A6 00               LDA A   0,X
00007 0009 B7 9001             STA A   $9001         ACC TO CRTC REG
00008 000C 08                  INX
00009 000D 5C                  INC B                 INC COUNTER
00010 000E C1 10               CMP B   #$10          LAST CRTC REG?
00011 0010 26 F2               BNE     CRTII
00012 0012 3F                  SWI
00013 0020                     ORG     $20
00014 0020 65          CRTTAB  FCB     $65,$50,$56,$9
00015 0024 18                  FCB     $18,$0A,$18,$18
00016 0028 00                  FCB     0,$0B,0,$0B
00017 002C 0080                FDB     $80,$80
00018      0000                END
CRTII   0004 CRTTAB 0020

TOTAL ERRORS 00000
```

OPERATION OF THE CRTC

Timing Chart of the CRT Interface Signals – Timing charts of CRT interface signals are illustrated in this section with the aid of programmed example of the CRTC. When values listed in Table 4 are programmed into CRTC control registers, the device provides the outputs as shown in the Timing Diagrams (Figures 13 through 15). The screen format of this example is shown in Figure 9. Figure 16 is an illustration of the relation between Refresh Memory Address (MA0-MA13), Raster Address (RA0-RA4) and the position on the screen. In this example, the start address is assumed to be "0".

TABLE 4 – Values Programmed Into CRTC Registers

Reg. #	Register Name	Value	Programmed Value
R0	H. Total	$N_{ht}+1$	N_{ht}
R1	H. Displayed	N_{hd}	N_{hd}
R2	H. Sync Position	N_{hsp}	N_{hsp}
R3	H. Sync Width	N_{hsw}	N_{hsw}
R4	V. Total	$N_{vt}+1$	N_{vt}
R5	V. Scan Line Adjust	N_{adj}	N_{adj}
R6	V. Displayed	N_{vd}	N_{vd}
R7	V. Sync Position	N_{vsp}	N_{vsp}
R8	Interlace Mode		
R9	Max. Scan Line Address	N_{sl}	N_{sl}
R10	Cursor Start		
R11	Cursor End		
R12	Start Address (H)	0	
R13	Start Address (L)	0	
R14	Cursor (H)		
R15	Cursor (L)		
R16	Light Pen (H)		
R17	Light Pen (L)		

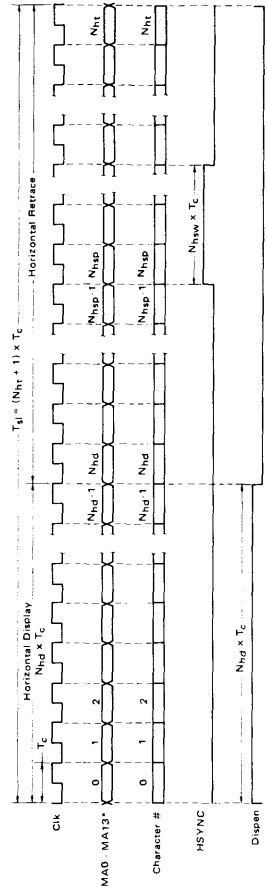


FIGURE 13 – CRTC HORIZONTAL TIMING

*Timing is shown for first displayed scan row only. See Chart in Figure 16 for other rows. The initial MA is determined by the contents of Start Address Register. R12/R13. Timing is shown for R12/R13 = 0.

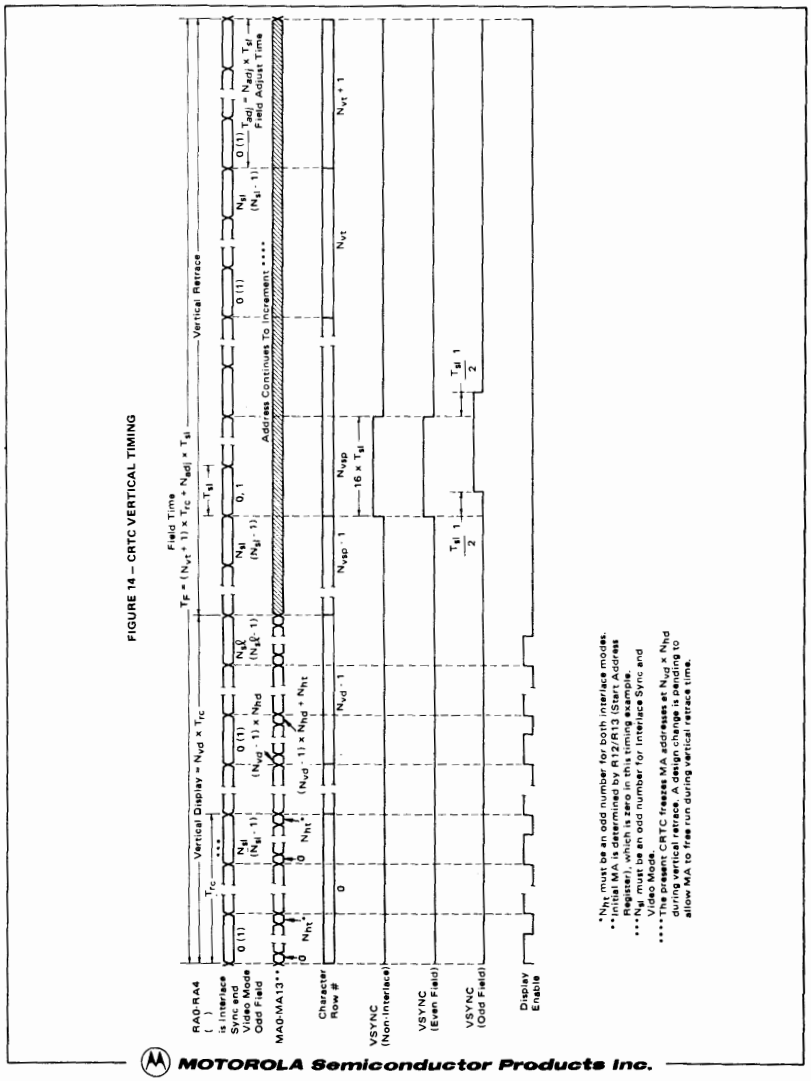


FIGURE 14 — CRTC VERTICAL TIMING

*N_{ht} must be an odd number for both interlace modes.
**Interlace MA is determined by R8 bits 0 and 1 of Address Register A, which is zero in this example.
***N_{si} must be an odd number for interlace Sync and Video Mode.
****The present CRTC freezes MA addresses at $N_{vd} \times N_{hd}$ during vertical retrace. A design change is pending to allow MA to free run during vertical retrace time.

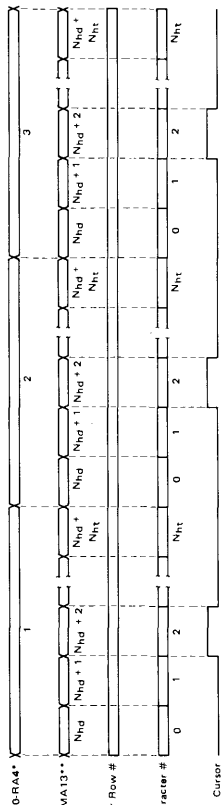


FIGURE 15 — CURSOR TIMING

*Timing is shown for non-interlace and interlace sync modes.
Example shown has cursor programmed as:
Cursor Register = $N_{hd}+2$
Cursor Start = 1
Cursor End = 3

**The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

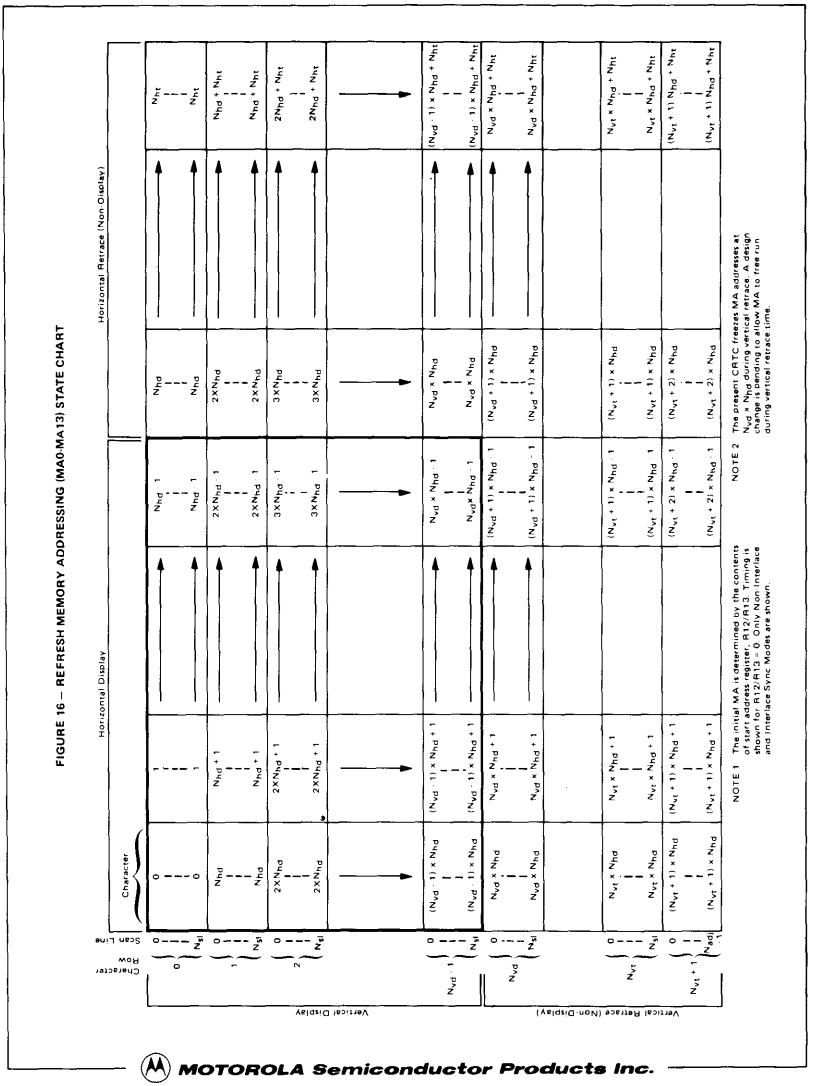


FIGURE 16 – REFRESH MEMORY ADDRESSING (MA0-MA13) STATE CHART

NOTE 1 The initial MA is determined by the contents of start address register: R12/R13. Timing is shown for R12/R13 = 0. Only Non Interlace and Interlace Sync Modes are shown.

NOTE 2 The present CRTC freezes MA addresses at $N_{vd} \times N_{hd}$ during vertical retrace. A design change is pending to allow MA to free run during vertical retrace time.

TEAC FD-54

MINI FLEXIBLE DISK DRIVE

MAINTENANCE MANUAL

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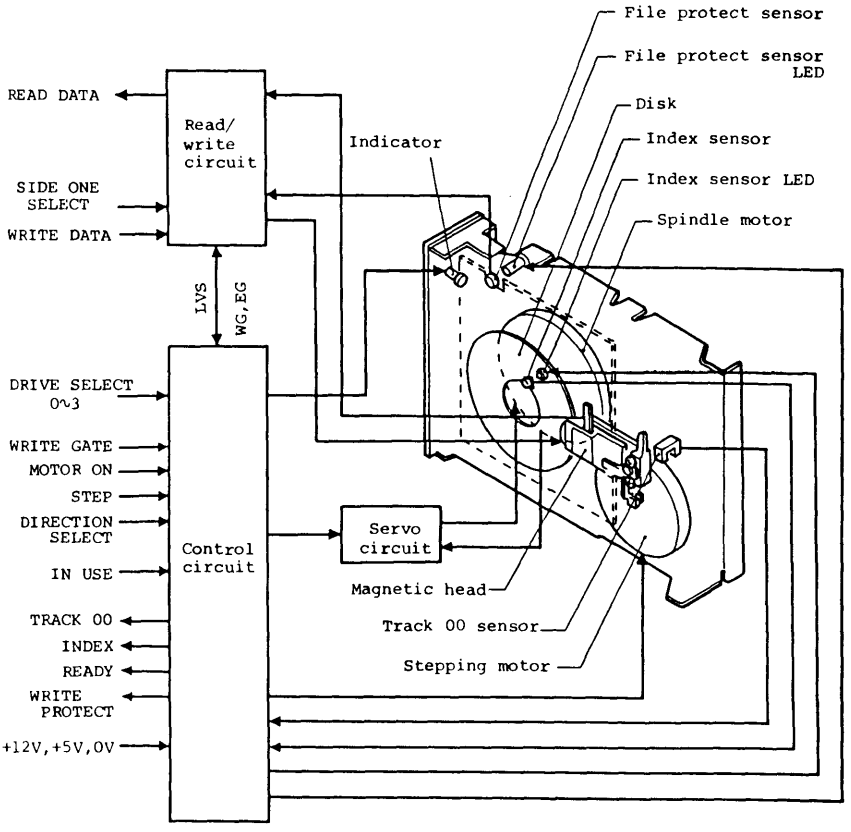
SECTION 3

THEORY OF OPERATION

3-1. CONSTRUCTION AND FUNCTION

3-1-1. General Block Diagram



(Fig.301) General block diagram

3-1-2. Mechanical Section

Since the disk is a flexible recording media made of mylar film base and data interchangeability between disks and FDDs is required, the mechanical section of the FDD uses precision parts and it is also assembled with high precision. For this reason, only trained technicians can handle the internal mechanism. Never apply excessive impact nor drop the FDD down on the desk.
The mechanical section is constructed with frame (chassis), door mechanism, disk clamp mechanism, disk rotation mechanism, magnetic head and carriage, head seek mechanism, various detection mechanisms, etc.

(1) Frame (chassis)

The main structure for mounting the various mechanisms and printed circuit boards. The frame is made of sheet metal to maintain the stability of the FDD in strength, precision,durability, and expansion coefficient.

(2) Door mechanism and disk clamp mechanism

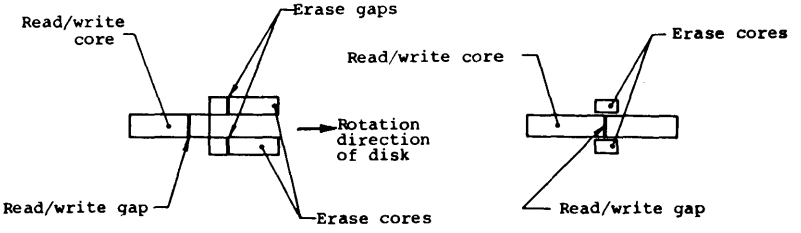
The door mechanism is constructed with clamp spring (plate spring), front lever, set arm, etc. The end of the clamp spring makes the disk clamp mechanism (collet Ass'y) move up and down.
When a disk is inserted and the front lever is closed, the tip of the collet is inserted in the central window of the disk and the window area is depressed to the spindle so that the center of the disk is clamped in the correct position along the outer circumference of the collet.

(3) Disk rotation mechanism

The disk rotation mechanism comprises DD motor Ass'y which includes spindle.

The DD motor is an outor-rotor type DC brushless motor which has the long life of 20,000 hours or more in continuous rotation.
The rotational speed is 300rpm and maintains stable rotational speed against load variations and environmental changes. This is achieved by a feedback signal from the internal AC tachometer.
The precisely combined collet and spindle are attached at the correct angle to maintain the center position correctly without damaging the center hole of the disk and so as to make the head be in contact with disk at the correct angle.

(4) Magnetic head and carriage



Tunnel erase type head Straddle erase type head

(Fig.302) External view of magnetic head core

For single sided FDDs, the external view of the magnetic head is button shaped and it is mounted on the carriage so that it is in contact with the SIDE 0 (the buttom side when the FDD is placed horizontally) head window area of the disk.
For double sided FDDs, both the SIDE 1 head and the SIDE 0 head are special flat type supported with the gimballed mechanisms. The two magnetic heads are mounted accross the disk on one carriage.
In both types of head, the surface is designed for minimum disk wear and maximum read output. The head itself is a long life type for

improved head wear.
For the FD-54 drives, either of tunnel erase type head or straddle erase type head is used. The core of the tunnel erase type head is constructed with a read/write gap which is used for data write and data read operations and two erase gaps which are used to erase the edges of the recorded track immediately after the recording (tunnel erase). For the straddle erase type head, the core is constructed with a read/write gap and two erase cores for erasing the edges of the recorded track at the same time with the recording.
Even though the core construction of these two types of head are different, their functions in the FD-54 drives are the same and have complete interchangeability between the data recorded on the disks.
The magnetic head and the carriage on which the head is mounted form the most important part of the FDD and is specially assembled with high precision.

(5) Head seek mechanism

The head seek mechanism consists mainly of stepper motor with a capstan (pooly), steel belt (band), guide shafts, and carriage.
The carriage is connected to the capstan of the stepping motor through the steel belt and is slided along the guide shafts.
The flat type 4-phase stepping motor is adopted and it rotates 2 steps (3.6°) per one track space. The stepper motor is driven in a unique 1-2 phase driving method which brought a success in reducing the heat radiation and to obtain a high speed driving and positioning accuracy.
The parrallelism and the distance between the shafts and the center line of the disk, and shaft and disk themselves are precisely machined.
Also the thermal expansion of the chassis, steel belt, carriage, etc. are taken into consideration in the process of design so that they are mutually offset with the expansion of the disk.

(6) Detection mechanisms

(a) File protect detection mechanism

This mechanism is constructed with an LED and a photo-transistor to detect the existence of the write enable notch of the disk jacket. When a disk with the notch covered is installed and the light pass for detection is disturbed, no write or erase current will be supplied to the read/write and erase heads and the recorded information on the disk is protected from an erroneous input of a write command.
The LED is mounted on the PCBA DD motor servo and the photo-transistor on the front OPT Ass'y.

(b) Track 00 detection mechanism

This mechanism is constructed with a photo-interrupter for detecting the outermost track position (track 00) of the head and the track 00 stopper which is ataached to the rear side of the head carriage. Inside tracks from the track 00 on the disk are used. Even if an erroneous step out command is input from the track 00 position, the command will be ignored by the internal circuit of the FDD.
If the head moves out from the track 00 by some reason (such as impact during transportation), the head carriage strikes the track 00 stopper to protect the head from moving out of the returnable range at a next power on.

When step-in commands are input from the innermost track, the head seeks toward inward and stops with an appropriate space left against the head window edge of the disk. In order to recalibrate the track from this position (returning operation to the track 00), it is required to input the step-out commands with several additional steps to the maximum track number.

(c) Index detection mechanism

LED and photo-transistor for the detection of the index hole are

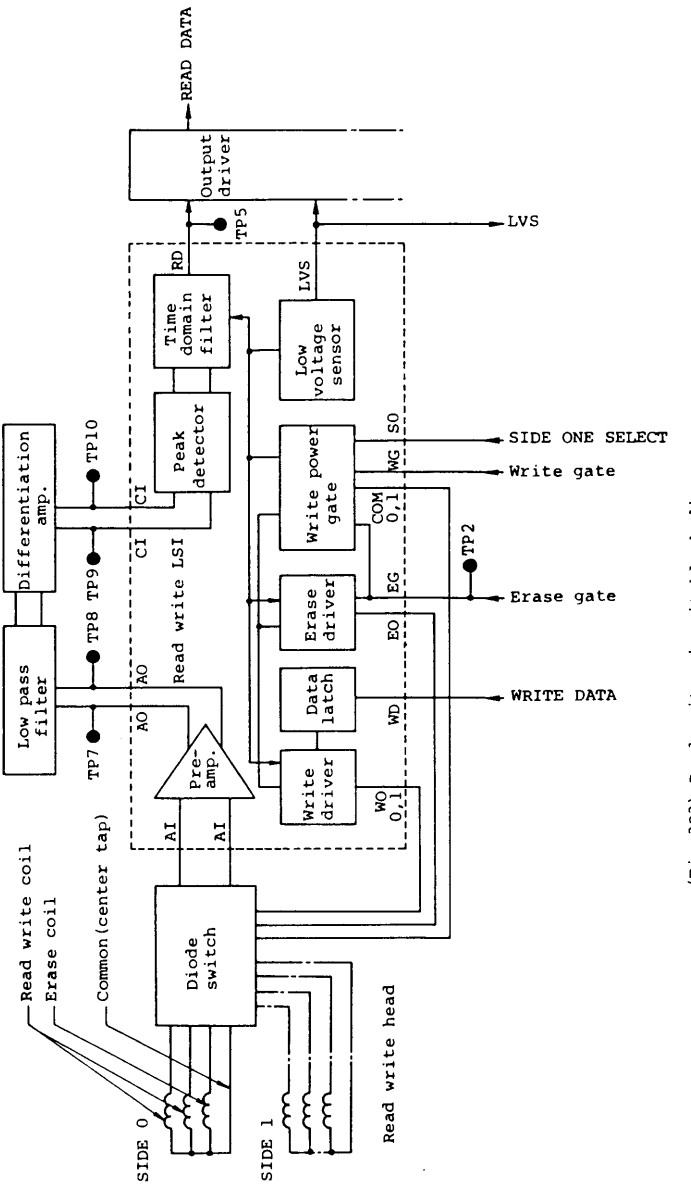
located at the index window area of the disk jacket.
The LED is mounted on the PCBA DD motor servo and the photo-transistor on the front OPT Ass'y. The index hole will be detected along the rotation of the disk.

3-2. CIRCUIT DESCRIPTIONS

The electronics of the FDD is constructed with three sections which are read write circuit, control circuit, and servo circuit. Read write circuit and control circuit are mounted on the PCBA MFD control, and servo circuit is on the PCBA DD motor servo.

3-2-1. Read Write Circuit

The read write circuit is constructed with read circuit, write circuit, and low voltage sensor. They are mostly packed in a read write LSI (bipolar).
Fig.303 shows the block diagram.



(Fig.303) Read write circuit block diagram

(1) Read circuit

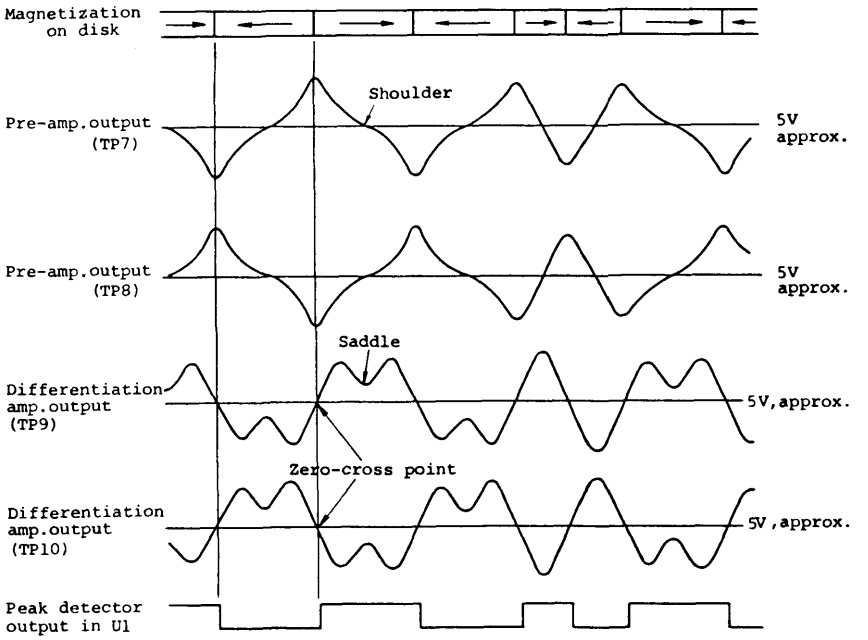
The read circuit consists of pre-amplifier, low pass filter, differentiation amplifier, peak detector, time domain filter and read gate (output driver).

In read operation, the minute voltage induced by the read/write head is amplified about 30dB by the pre-amplifier which is constructed with a video band differential amplifier. Undesirable high frequency noise is eliminated by the low pass filter (L1, L2, C30, etc.) and the read signal is supplied to the differentiation amplifier (Q3, Q4, L3, C35, etc.).

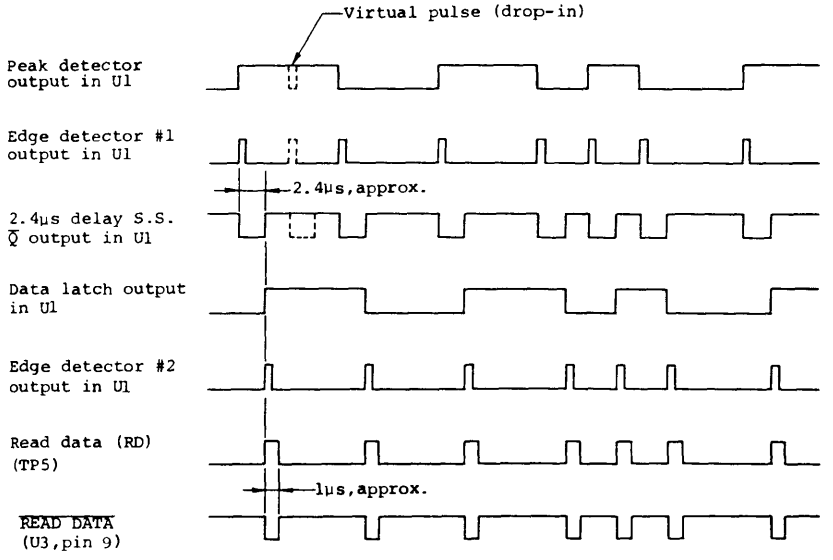
The differentiation amplifier phase-shifts the peak position of the reproduced waveform to the zero cross point, and at the same time, further amplifies the signal about 20dB with the most appropriate equalization. The peak detector which is constructed with a comparator converts the differentiated output into a square wave.

The time domain filter eliminates a virtual pulse caused by the saddle in the low frequency area (1F area, 62.5KHz, approx.) at outer tracks. The time domain filter is constructed with two edge detectors, 2.4µsec, delay single shot (LSI pin 7, RA5, C21), data latch, and 1µsec data single shot (LSI pins 8 and 9, RA5, C22).

Then the signal is output from the FDD through the read gate, U3 (pins 9, 10, 3-state output driver).



(Fig.304) Read amp. and peak detector waveforms



(Fig.305) Time domain filter and read gate waveforms

(2) Write circuit

The write circuit consists of write power gate (with side selector), select gate, data latch, write driver, and erase driver. The write power gate output (COM0 or COM1) becomes high voltage when the write gate signal or the erase gate signal is TRUE (HIGH level). These signals are generated by the write/erase gate in the control circuit when all of the following three conditions are satisfied.

(a) The file protect sensor detects the notch of the disk jacket (write enable condition).
(b) The WRITE GATE input signal is TRUE.
(c) MX strap is on or the DRIVE SELECT signal is TRUE (LOW).

The write power gate output is supplied to the common terminal of the head through the diode switch. Table 301 shows the output voltage of the write power gate in various operations.

Conditions	Write power gate output voltage	
	COM 0 (for Side 0)	COM 1 (for Side 1)
Side 0 write operation	High	Low
Side 1 write operation	Low	High
Side 0 read operation	Middle	Low
Side 1 read operation	Low	Middle

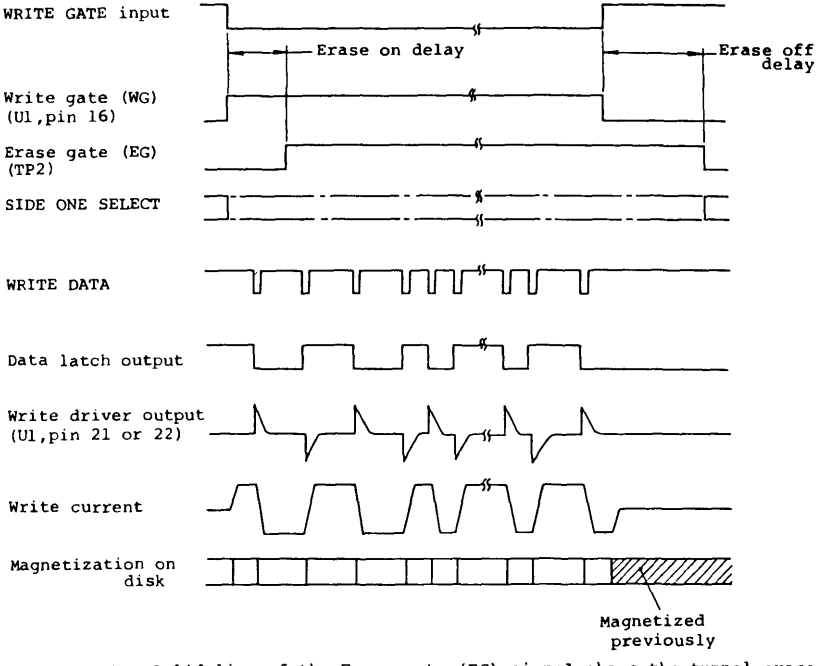
High: 10.5V, approx. Middle: 4V, approx. Low: 0V, approx.

(Table 301) Write power gate output voltage

For the tunnel erase head, the erase gate signal is delayed appropriately against the write gate signal. Since the erase gap is about 0.85mm behind the read/write gap, it is necessary for the erase driver to delay the write gate signal so that the written data is completely trimmed by the erase head (tunnel erase).

For the straddle erase head, the write gate and the erase gate signals have the same timing. The tunnel erase or the straddle erase produces a guard band between the tracks preventing deterioration of the S/N ratio resulting from a off-track (positioning error). It also ensures disk interchangeability.

The WRITE DATA input pulse is latched by the data latch. And appropriate write current is supplied to the read/write head by turning on and off the two write drivers alternately. When the write driver is active, no read data pulse is generated by the read circuit.

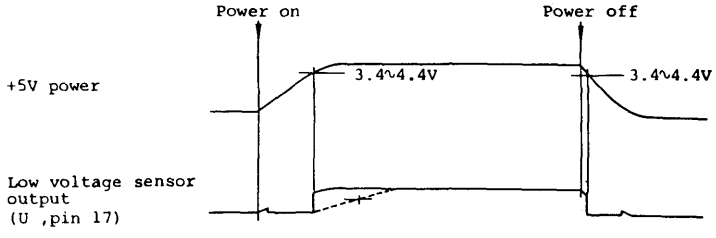


Note: Solid line of the Erase gate (EG) signal shows the tunnel erase type and dotted line shows the straddle erase type. Erase on delay and Erase off delay are applied only for the tunnel erase type.

(Fig.306) Write circuit waveforms

(3) Low voltage sensor

The low voltage sensor is equipped to protect the FDD from erroneous operation due to the internal circuit construction of the FDD during unstable condition of the supplied voltage such as at power on or off. The output of this sensor is supplied to almost all the functional blocks of the read write circuit, and control circuit to protect the write driver and erase driver from erroneous operation under the unstable condition of the DC power voltage.



Note: Dotted line shows the LVS input pin 34 of U2, control LSI.

(Fig.307) Low voltage sensor waveforms

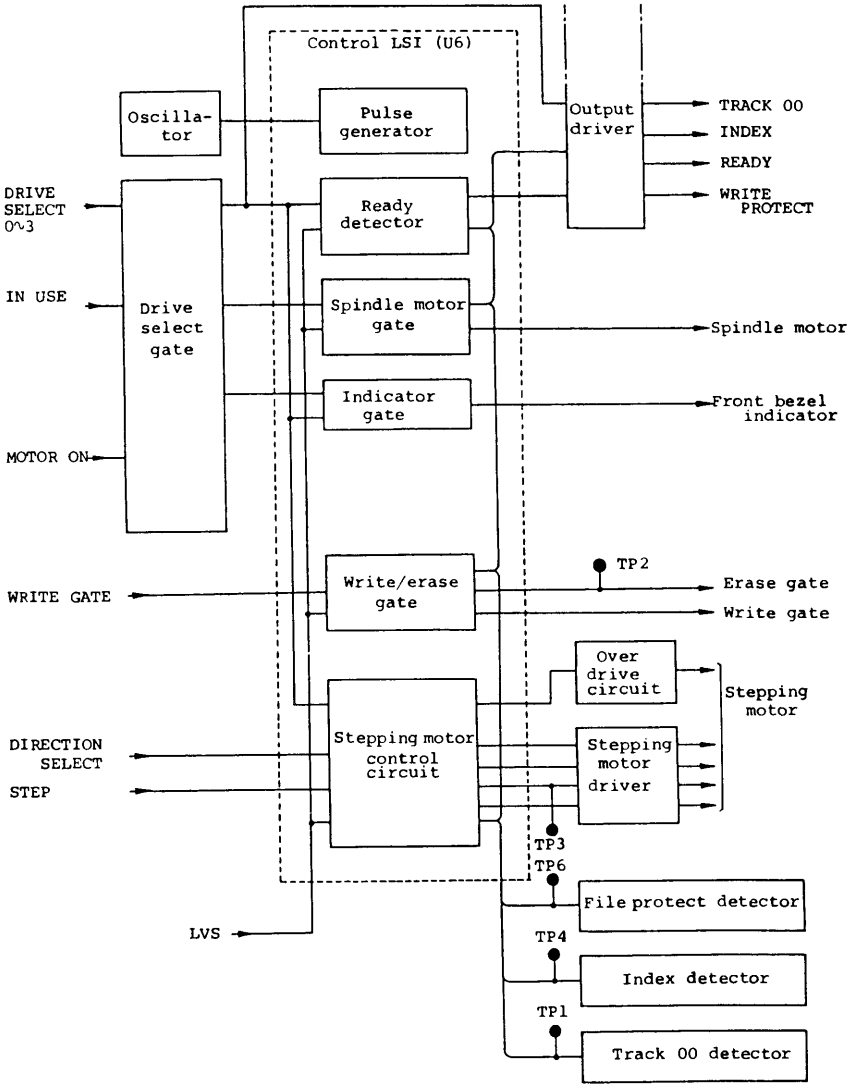
3-2-2. Control Circuit

The control circuit consists of gates, detectors, and the stepping motor control circuit. The gates are drive select gate to determine the drive select condition, spindle motor gate to determine the rotational condition of the spindle motor, write/erase gate to control the actual write operation, etc. The detectors are index/sector detector, track 00 detector, file protect detector, and ready detector. The former three detectors (photo-transistors) are mounted on the front OPT Ass'y and the transport frame. And the other circuits are mounted on the PCBA MFD control (mostly packed in a control LSI (CMOS)). Fig.308 shows the block diagram.

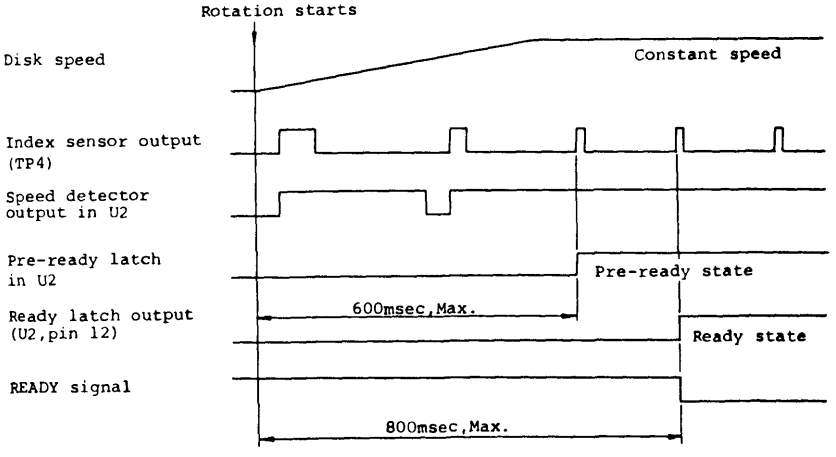
Drive select gate classifies the external input signals into several functions and transmits them into the control LSI.
The selection of straps (short bars) determines the select condition of the drive, spindle motor operating conditions, and turn-on condition of the front bezel indicator. Refer to items 1-11 of the Specification as to the detailed function of each strap.

The write/erase gate judges the FDD whether it can execute write operation or not and issues write gate and erase gate signals for the write circuit. For the FDD with tunnel erase head, a specified delay time is established in the erase gate signal by an internal counter (refer to Fig.306).

The ready detector consists of speed detector and ready latch. The output of the speed detector which is constructed with a re-triggerable counter becomes always TRUE (HIGH) when the rotational speed of an installed disk (soft sectored) is more than 50%, approx. of the rated speed. The ready latch detects the second index pulse after the speed detector detects the 50% of the rated speed, then the READY condition is informed to the host system through the output driver, U7 (pin 13 ∿ 14).



(Fig.308) Control circuit block diagram



(Fig.309) Ready detector waveforms

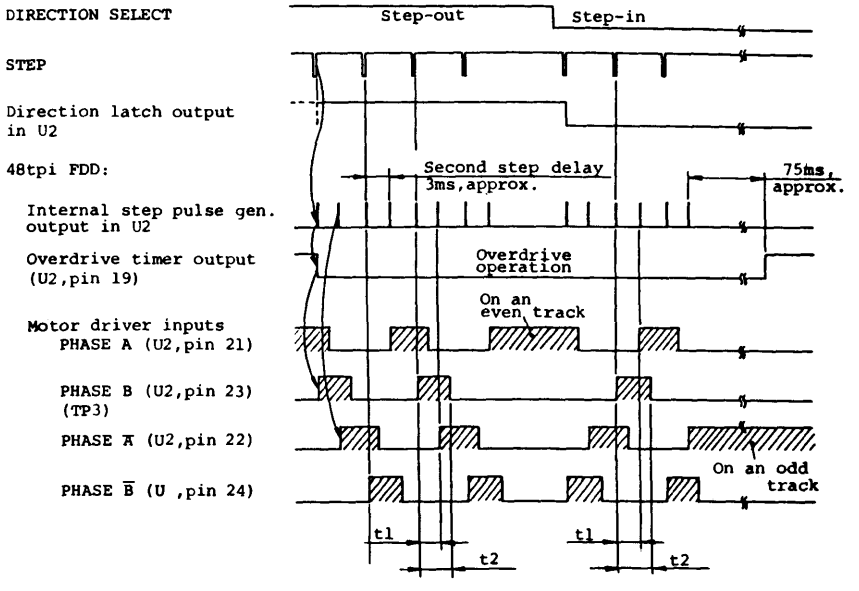
Stepping motor control circuit is constructed with direction latch, internal step pulse generator, shift register, phase drive selector, overdrive timer, etc.

Direction latch is a circuit to sample and hold the head seek direction designated by the DIRECTION SELECT signal at every input of the STEP pulses.

The internal step pulse generator is constructed with a counter and a pulse generator. The counter is triggered at the trailing edge of the STEP input pulse, and the second internal step pulse is generated with a delay of 3msec, approx. from each STEP input pulse by the pulse generator. It makes the stepping motor rotate for 2 steps (3.6°) in response to one STEP input pulse.

Outputs of the direction latch and the internal step pulse generator are input to the shift register and phase drive selector, and they are converted to the appropriate timing signals for uni-polar 1-2 phase drive of the 4-phase stepping motor. These phase drive signals are supplied to the stepping motor driver, U5 (output pins 12 ∿ 15). In order to improve the torque margin in the seek operation, partially 2-phase drive period is provided by the phase drive selector only in the initial stage when the drive phase is changed.
When the head stops on an even track, phase A is magnetized, while phase $\overline{A}$ is magnetized when the head stops on an odd track. The phase B and $\overline{B}$ are magnetized only during the seek operation.

The output from the internal step pulse generator is also supplied to the over-drive timer constructed with a re-triggerable counter. During the active period of this timer (75msec, approx.), +12V power is supplied to the stepping motor coils through the over-drive circuit (Q1) to produce enough torque required for the head seek and the settling operations. After the completion of the settling, only +5V power is supplied to the stepping motor through the diode, CR1, which minimize the power loss by supplying only the required torque for the holding of the stop position. By the above consideration, heat radiation from the motor is depressed to the minimum level and the stepping motor power consumption of 0.33W, approx. at the stop condition is achieved.



t1: Second step delay (3ms,approx.)
t2: Phase B or $\overline{B}$ magnetization (3.6ms,approx.)

(Fig.310) Stepping motor control circuit waveforms

3-2-3. Servo Circuit

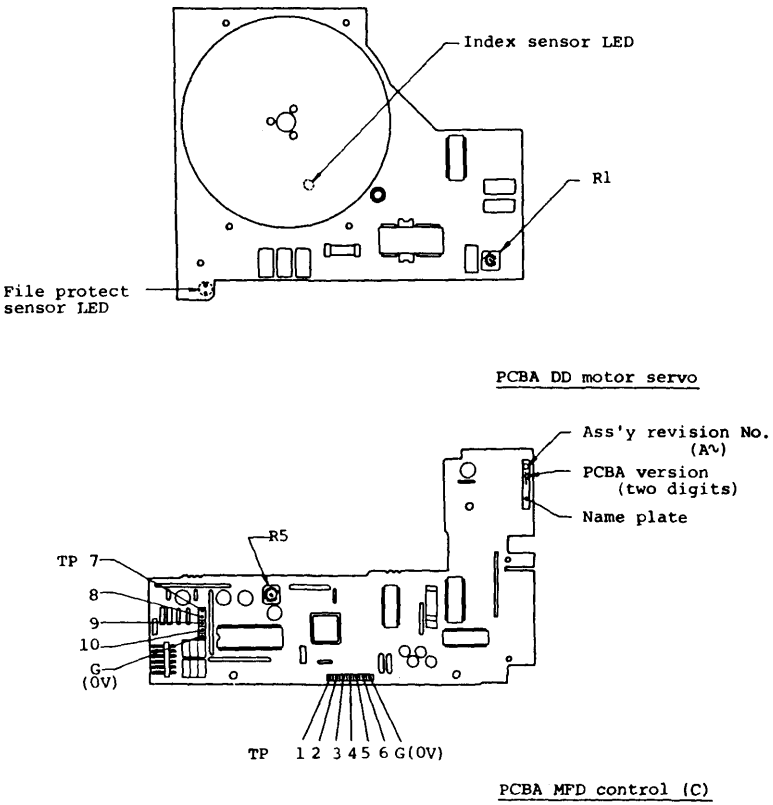
The servo circuit aims to maintain the rotational speed of the spindle motor at 300rpm, and the circuit is mounted on the PCBA assembled with the spindle motor.

Start and stop of the spindle motor (DD motor Ass'y) is controlled by the MOTOR ON signal supplied through the spindle motor gate in the control circuit.

The spindle motor is a long life DC brushless motor having 3-phase coils. The coils are driven by the exclusive drive IC. Energization and magnetized direction of the coils are controlled by the signal from the hall elements mounted on the PCBA around the rotor so that they are changed corresponding to the designated rotational direction. The rotational speed is maintained stably and precisely. The feedback signal from the AC tacho-meter in the rotor is converted into the drive voltage (F-V conversion) by servo IC, and supplied to the driver IC through the phase compensation circuit.

3-3. FUNCTION OF TEST POINTS AND VARIABLE RESISTORS

Fig.311 shows the mounting positions of the test points and variable resistors.



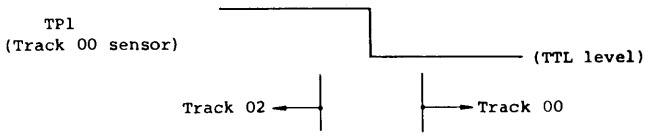
(Fig.311) Location of test points and variable resistors

3-3-1. Function of Test Points

Twelve test points (two for ground) are equipped on the PCBA MFD control for the check and adjustment of the FDD.

(1) TP1 (Track 00 sensor)

Test point to observe the output of the track 00 detection photo-transistor (shumitt inverter included). As well as TRACK 00 output signal, TP1 becomes LOW level when the head is on track 00 or around track 00 position.

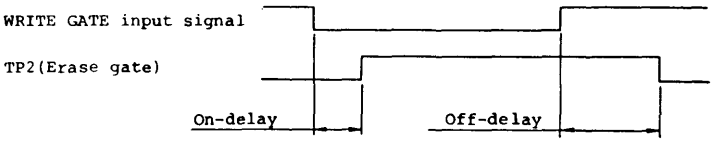


(Fig.312) Typical waveform of TP1

Note: The TRACK 00 output signal goes TRUE (LOW level) only when the phase A coil of the stepper motor is energized and the direction latch is set to the step-out direction (refer to Fig.310). Therefore, the level change timing of the TRACK 00 signal is not consistent with that of the TP1 signal.

(2) TP2 (Erase gate)

Test point to observe the output of the erase gate.
When TP2 is HIGH level, erase current flows through the erase head.
This TP is used for the check and adjustment of the required delay time of the erase gate signal against the WRITE GATE input signal when the tunnel erase head is used.



(Fig.313) Typical waveform of TP2(for tunnel erase head)

Delay	Straddle erase head	Tunnel erase head
On-delay	0μs	200 ∿ 320μs
Off-delay	0μs	860 ∿ 950μs

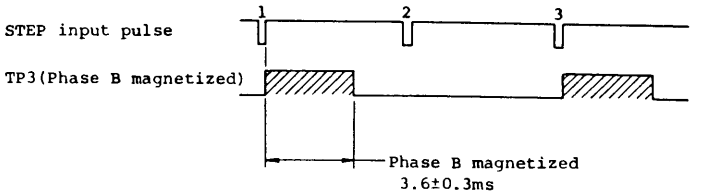
(Table 302) Erase gate delay

(3) TP3 (Phase B)

Test point to observe the phase B magnetized period of the stepping motor.
The stepping motor rotates for 2-steps in response to one STEP input pulse. Therefore, TP3 becomes HIGH level for a specified period when a step-out command from an even track or when a step-in command from an odd track is executed. Refer to Fig.310.

(4) TP4 (Index)

Test point to observe the output of the index detection photo-transistor (shumitt inverter included).
The signal level at this TP is opposite to that of INDEX output signal. When the index hole or sector hole (hard sectored disk) is detected, HIGH going pulse is observed at TP4. The photo-transistor is mounted on the front OPT Ass'y and the LED is mounted on the back side of the



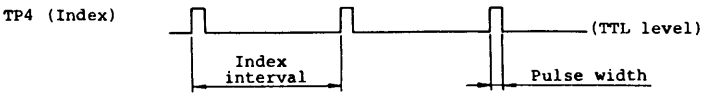
(Fig.314) Typical waveform of TP3

PCBA DD motor servo.

The test point is used for the following purposes.

(a) Confirmation and adjustment of the disk rotational speed. Speed is adjusted by the variable resistor R1 on the PCBA DD motor servo.

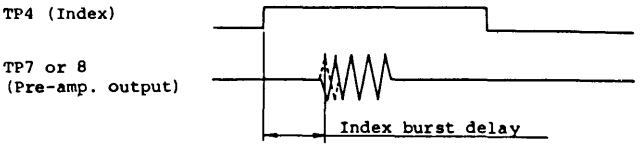
(b) Confirmation and adjustment of the index burst timing. Burst timing is adjusted by the index sensor installation screw in the front OPT Ass'y



(Fig.315) Typical waveform of TP4 (Speed observation)

Items	Timing
Index interval	200±4ms
Pulse width	2 ∿ 5.5ms
Burst delay	200±200μs

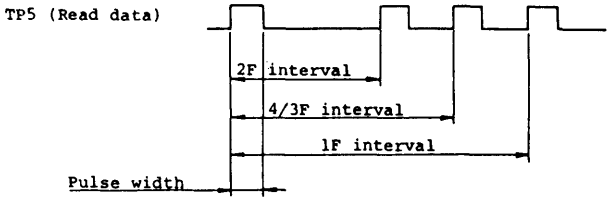
(Table 303) Index timing



(Fig.316) Typical waveform of TP4 (Burst timing observation)

(5) TP5 (Read data)

Test point to observe the read data pulse.
The signal level at this TP is opposite to that of the READ DATA output signal.



(Fig.317) Typical waveform of TP5

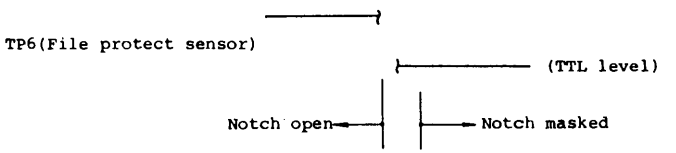
Fig.317 shows the waveform at TP5 in normal data read operation.
In the FM method, 2F and 1F intervals are observed, while 2F, 4/3F, and 1F intervals are observed in the MFM method.

Items	Timing
2F interval	4µs, Nom.
4/3F interval	6µs, Nom.
1F interval	8µs, Nom.
Pulse width	1±0.5µs

(Table 304) Read data pulse timing

(6) TP6 (File protect sensor)

Test point to observe the output of the file protect detection photo-transistor (shumitt inverter included).
As well as the WRITE PROTECT output signal, TP6 becomes LOW level when a disk with the masked write protect notch (write operation cannot be done) is installed.

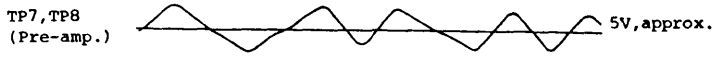


(Fig.318) Typical waveform of TP6

(7) TP7, TP8 (Pre-amplifier)

Test point to observe the read pre-amplifier output signals.
The pre-amplifier has two outputs of the order of several dozen to several hundred mVp-p, and they differ in phase by 180° (opposite phase).
Both outputs are observed at TP7 and TP8 respectively.
For an accurate observation of the read waveforms, use two channels of an oscilloscope with one channel set to Invert mode and Add mode of both channels. Use G (0V) test point for the oscilloscope ground.

TP7 and TP8 are used for checking various characteristics of the read/write head and also for the check and adjustment of the head seek mechanism such as track alignment.



(Fig.319) Typical waveform of TP7 and TP8

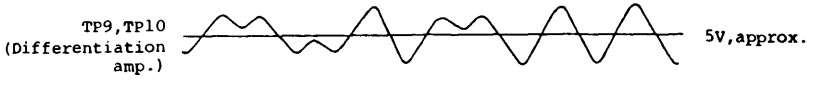
(8) TP9, TP10 (Differentiation amplifier)

Test points to observe the differentiation amplifier output signals. Like the pre-amplifier, the differentiation amplifier also has two outputs of the order of several hundred mVp-p to several Vp-p which differ in phase by 180°. Both outputs are observed at TP9 and TP10 respectively.

For an accurate observation of the waveforms, use two channels of the oscilloscope with one channel set to Invert mode and Add mode of both channels.

Use G (0V) test point for the oscilloscope ground.

TP9 and TP10 are used for checking the total operation of the read/write head and the read amplifier and for the check and adjustment of the head seek mechanism such as track alignment.



(Fig.320) Typical waveform of TP9 and TP10

(9) TP G (0V) -- PCBA MFD control, PCBA read write amp.

TP G is equipped respectively for two test point blocks (TP1 ∿ 6 and TP7 ∿ 10). They are used as the ground terminals for measurement equipment. Be sure to use a small size clip to obtain a probe ground of the equipment.

3-3-2. Function of Variable Resistors

On the PCBA MFD control and the PCBA DD motor servo, maximum two variable resistors are mounted.
The PCBA MFD control of some PCBA versions and some revision numbers has not the variable resistor R5. Also some types of DD motor Ass'y have not the variable resistor R1 on the PCBA DD motor servo.
However, there is interchangeability in function and performance between these PCBAs with the variable resistor and without the variable resistor as far as they have the same parts number (8 digits) and the same version number (2 digits).
The variable resistors are correctly adjusted before the shipment of the FDD and fundamentally they shall not be readjusted except for by a trained technicians.

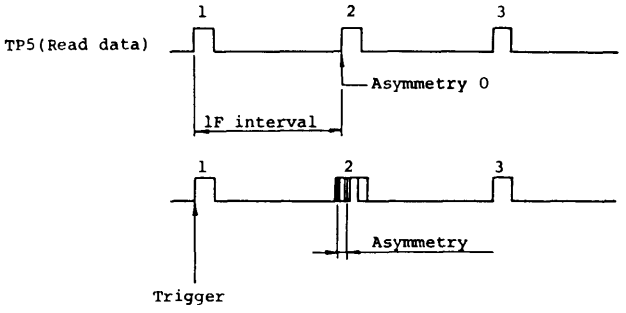
(1) R1 on PCBA DD motor servo (Disk rotational speed adjustment)

Variable resistor for adjusting the rotational speed of the disk.
It is adjusted so that the index pulse interval at TP4 or at the INDEX output signal is 200msec±4msec (see Fig.315).
For the DD motor Ass'y without the variable resistor R1, the rotation speed of the motor is fixed by the ceramic oscillator in the servo circuit and no adjustment is required.

(2) R5 on PCBA MFD control (Read data asymmetry adjustment)

Variable resistor for adjusting the asymmetry of the read data pulse.
Some PCBAs have this variable resistor and others have fixed resistor instead of it.
For a PCBA with the variable resistor, R5, write 1F data and observe the pulse intervals at TP5 or at the READ DATA output signal during read operation. Then adjust the variable resistor so that the read data asymmetry in Fig.321 takes the minimum value. For a double sided FDD, repeat this operation alternately for side 0 and side 1 heads to

obtain the minimum asymmetry for both sides.



(Fig.321) Read data asymmetry

SECTION 4

MAINTENANCE

4-1. GENERAL

4-1-1. Periodic Maintenance

The FDD is designed to be free from periodic maintenance such as replacement of parts, grease-up, etc. when it is operated at a normal operation duty.
However, cleaning of the magnetic head using a cleaning disk is recommended since it is effective to improve the reliability of the data.
If some of the parts in the FDD are operated at a specially heavy duty condition, or if the FDD is operated over 5 years, it is recommended to replace the wear parts according to Table 403.

Periodic maintenance items	Recommended cycle	Required time	Referred items
Cleaning of magnetic head	Refer to 4-3-1 and 4-3-2	5 min.	4-3-1
Replacement of wear parts	Refer to 4-1-3 and 4-5.		

(Table 401) Periodic maintenance items

4-1-2. Check and Adjustment

Table 402 shows all of the check and adjustment items. Following items do not require periodic maintenance. Check and adjustment should be done when required during replacement of the maintenance parts or during trouble shooting referring to items 4-2 and 4-3.

The numbered procedure in Table 402 shows a typical procedure of the general check and adjustment all over the FDD.

Steps	Check and adjustment items	Required time	Referred items
1	Adjustment of collet shaft plate	5 minutes	4-4-1
2	Adjustment of front lever position	5 minutes	4-4-2
3	Check and adjustment of disk pad lever (bail) (double sided only)	5 minutes	4-4-3
4	Check of file protect sensor	5 minutes	4-4-4
5	Check and adjustment of disk rotation speed	5 minutes	4-4-5
6	Check and adjustment of head touch	5 minutes	4-4-6
7	Check and adjustment of asymmetry	5 minutes	4-4-7
8	Check of read level	5 minutes	4-4-8
9	Check of resolution	5 minutes	4-4-9
10	Check and adjustment of track alignment	10 minutes	4-4-10
11	Check and adjustment of track 00 sensor	5 minutes	4-4-11
12	Check and adjustment of track 00 stopper	5 minutes	4-4-12
13	Check and adjustment of index burst timing	5 minutes	4-4-13

(Table 402) Check and adjustment items

4-1-3. Maintenance Parts Replacement

It is recommended to replace the wear parts periodically if the FDD is operated at a specially heavy duty condition or if it is operated over five years. Periodic replacement is not required for the parts if the FDD is operated at a normal operation duty.
Table 403 shows all of the maintenance parts. Replace the wear parts according to the recommended replacement cycle. Periodic replacement is not required for parts without a recommended replacement cycle.
The replacement of the parts should be done according to each referred item in Table 403.

Notes for Table 403:

(1) Since the parts number versions of PCBA MFD control (C) vary depending on some factors such as signal interface condition, be sure to confirm the version by checking the name plate on the actual printed circuit board.

(2) The head carriage Ass'y are used always in pair with two guide shafts. The head carriage Ass'y represented by listed parts number in Table 403 includes these guide shafts which parts number is different from that of a head carriage Ass'y itself without these guide shafts.

(3) The listed parts numbers of the front bezel Ass'y and front lever Ass'y are those of standard color (black). For designating other color, use the corresponding parts number.

(4) Periodic replacement is not required for parts without a recommended replacement cycle. Replace the parts when required such as during repair.

(5) If two recommended cycles are listed, the cycle which the parts reach first should have priority.

(6) The required time for replacement includes the time for basic check and adjustment after the replacement.

(7) Order the maintenance parts using the parts number.

(Table 403-1) FD-54A (Single sided, 48tpi) Maintenance parts list

Maintenance parts			Replacement		
Parts name	Description	Parts No.	Replacement cycle	Required time	Referred items
Head carriage Ass'y (C) (For spare parts)	Note (2)	17966930-00	7,000 head load & motor on hrs. or $5x10^6$ seeks	45 min.	4-5-1
Stepping motor Ass'y (C)		14733730-00	$5x10^6$ seeks	30 min.	4-5-2
Steel belt (C)		16792300-00	Replace with stepping motor Ass'y	-	4-5-2
DD motor Ass'y (C) (Spindle motor)		14733780-00	20,000 motor on hrs.	20 min.	4-5-3
Collet Ass'y (C)		17966923-00	$3x10^5$ clamsp	15 min.	4-5-4
PCBA T00 sensor		15532004-00	-	10 min.	4-5-5
PCBA MFD control (C)	Note (1)	15532006-XX	-	30 min.	4-5-6
Front OPT Ass'y (C)		15090730-00	-	15 min.	4-5-7
Front bezel Ass'y	Note (3)	17966807-00	-	10 min.	4-5-9
Front lever Ass'y (C)	Note (3)	17966924-00	-	5 min.	4-5-10
Pad (Head pad)		16786634-01	2,500 head load & motor on hrs.	10 min.	4-5-8
Clamp cam Ass'y (C)		17966929-00	$1.5x10^5$ clamps	10 min.	
Eject Ass'y (C)	Option	17966926-00	$1.5x10^5$ clamsp	10 min.	

(Table 403-2) FD-54B (Double sided, 48tpi) Maintenance parts list

Maintenance parts			Replacement		
Parts name	Description	Parts No.	Replacement cycle	Required time	Referred items
Head carriage Ass'y (C) (For spare parts)	Note (2)	17966928-00	7,000 head load & motor on hrs. or $5x10^6$ seeks	45 min.	4-5-1
Stepping motor Ass'y (C)		14733730-00	$5x10^6$ seeks	30 min.	4-5-2
Steel belt		16792300-00	Replace with stepping motor Ass'y	-	4-5-2
DD motor Ass'y (C) (Spindle motor)		14733780-00	20,000 motor on hrs.	20 min.	4-5-3
Collet Ass'y (C)		17966923-00	$3x10^5$ clamps	15 min.	4-5-4
PCBA T00 sensor		15532004-00	-	10 min.	4-5-5
PCBA MFD control (C)	Note (1)	15532006-XX	-	30 min.	4-5-6
Front OPT Ass'y		15090730-00	-	15 min.	4-5-7
Front bezel Ass'y	Note (3)	17966807-00	-	10 min.	4-5-9
Front lever Ass'y (C)	Note (3)	17966924-00	-	5 min.	4-5-10
CSS Ass'y		17966927-00	3x10 clamsp	10 min.	4-5-11
Clamp cam Ass'y (C)		17966929-00	$1.5x10^5$ clamps	10 min.	
Eject Ass'y (C)	Option	17966926-00	$1.5x10^5$ clamps	10 min.	

4-1-4. Maintenance Jigs and Tools

The following are the jigs and tools required for adequate maintenance of the FDD.

(1) Equipment

(A) When Simulator KA (off-line exerciser for FD-54, abbreviated to SKA) is used:

(a) SKA

The following accessories are necessary for operating the SKA (the accessories are supplied with the SKA).

i) SKA/FDD interface cable (-00 type)
ii) Check cable #1 (for observation of control signals)
iii) Check cable #2 (for observation of read amp. output signals)
iv) SKA/FDD power cable

(b) Oscilloscope (two channels)

(c) DC power supply (+12V, 1.2A and +5V, 2A) or SKA power supply. The following accessory is required for the power supply (The accessory is supplied with the SKA power supply).

i) Power cable (4P)

(d) Thermometer and hygrometer

(B) When SKA is not used:

(a) FDD controller and DC power supply (user's system)
(b) Oscilloscope (two channels)
(c) Frequency counter

(d) Digital volt meter
(e) DC clip-on ammeter
(f) Thermometer and hygrometer

(2) Tools

(a) Cross-point screwdrivers, M2.6 and M3
(b) Common screwdrivers, small size and medium size
(c) Hexagon wrench key, 1.5mm
(d) A pair of tweezers
(e) Round nose pliers
(f) Cutting pliers
(g) Solder and soldering iron
(h) Hexagon screwdriver, M3

(3) Special jigs

(a) MAX media jig (Jig D, P/N 17890746-01)

(4) Disks

(a) Work disk (commercially available disk)

(b) Cleaning disk (commercially available cleaning disk)

i) Single sided type
ii) Double sided type

(c) Level disk (P/N 14900015-00)

(d) Alignment disk

i) Single sided, 48tpi type (P/N 14900016-20)
ii) Double sided, 48tpi type (P/N 14900016-21)

(5) Other articles used during maintenance

(a) Absolute alcohol (Ethanol)
(b) Cotton swab or gauze
(c) Locking paint (3 Bond, 1401B)
(d) Binding agent (Sumitomo Chemical, Cyano-bond SF, Red)
(e) Screws and washers (Refer to item 5-2-2)
(f) Lubricant (Kantoh Kasei, 946P)

Note: Be sure to use well calibrated equipment and disks.

4-2. PRECAUTIONS

4-2-1. Torque Applied to Screws and Locking Paint

The following torque should be applied to screws, unless otherwise specified.

Size of screws	Torque
M2	2kg.cm
M2.6	4.5kg.cm
M3	6kg.cm
M3 set screw	4.5kg.cm

(Table 404) Torque applied to screws

For tightening or loosening M3 set screws for adjustment and parts replacement, the following procedure should be followed.

(1) For adjustment, remove out the set screw and also remove the locking paint which had applied to the screw itself and around it.

(2) Apply fresh locking paint to the first three threads of the set screw with some narrow object such as a pair of tweezers.

(3) Adjust or tighten the set screw with the specified torque.

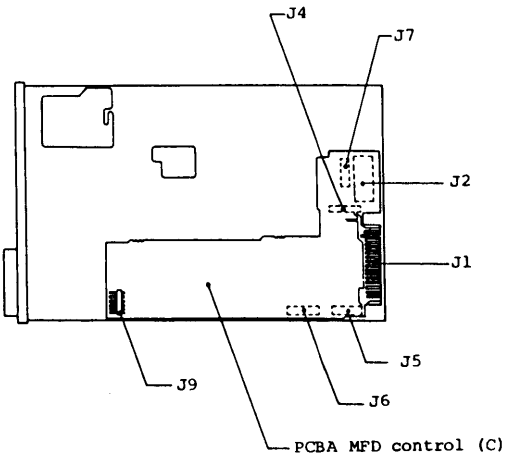
For other screws than set screws, apply a drop of locking paint to the designated points after tightening them.

4-2-2. Handling of Connectors

(1) Types of connectors

The following connectors are used for the FDD.

(a) J1: Interface connector
(b) J2: Power connector
(c) J4: Track 00 connector
(d) J5: Front OPT connector
(e) J6: Stepping motor connector
(f) J7: Spindle motor (DD motor Ass'y) connector
(g) J9: Head connector



(Fig.401) Types of connectors

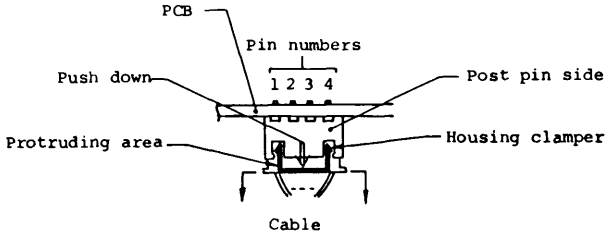
(2) Connection and disconnection of the connectors

Be sure to turn the power off before connecting and disconnecting the connectors. Connection or disconnection should be done straightly and correctly without applying excessive force to the cables and the post pins.

(3) Precautions for handling the white connectors (J4, J5, J6, J7)

(a) Disconnection of the connector

As shown in Fig.402, carefully push down the edges of the protruding area of the connector little by little with the finger nails or with a screwdriver.



(Fig.402) Disconnection of white connector

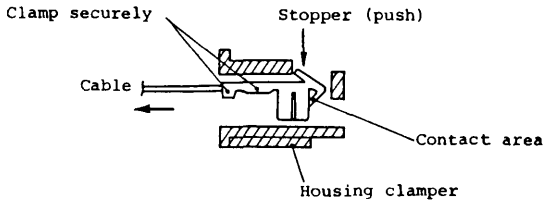
(b) Connection of the connector

Push the connector into the post pin under the PCBA matching the housing clamper to the groove.

(c) Removal of the pin (for reference)

Refer to Fig.403.
Depressing the stopper of the pin lightly with a narrow object such

as a pair of tweezers, pull the cable in the direction indicated by the arrow.



(Fig.403) Sectional view of white connectors

(d) Insertion of the pin (for reference)

Before insertion, check the following three points.

i) Confirm that the sheath and the core of the cable are securely clamped.

ii) Confirm that the stopper is lifted as in Fig.403 and it inhibits accidental removal.

iii) No tarnish or contamination should be on the contact area of the pin or the PCB side post pin. If there is, remove it.

Contact failure may happen if any of these three points is not satisfied.

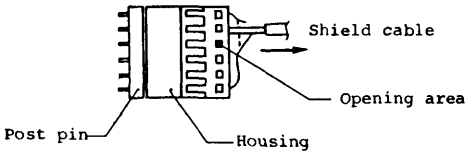
When you insert the pin, it should be so inserted that the stopper faces the opening side of the housing.

After the insertion, check the connection by pulling the cable lightly.

(4) Precautions for handling the black connector (J9)

(a) Disconnection of the connector

Pull out J9 connector straightly by inserting the narrow points of



(Fig.404) Disconnection of J9

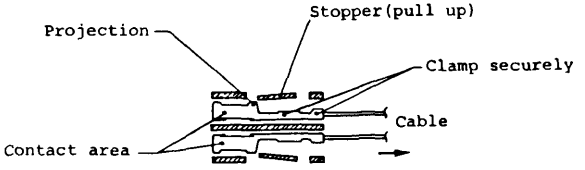
the tweezers into the opening area at the back side of the housing as shown in Fig.404. Be careful not to pull the fine wires.

(b) Connection of the connector

Make the polarizing key position of the housing correspond with the lack of the post pin, and push the housing carefully with the fingers.

(c) Removal of the pin

Lifting up the stopper of the housing with a narrow object such as cutter knife, pull the cable with a pair of tweezers in the direction indicated by the arrow. Refer to Fig.405.



(Fig.405) Sectional view of black connector

(d) Insertion of the pin

Before insertion, check the pins according to item (3)-(d), i) through iii).

When you insert the pin, it should be so inserted that the projection side faces the stopper of the housing. After the insertion, pull the cable with a pair of tweezers softly in order to confirm whether it is securely connected.

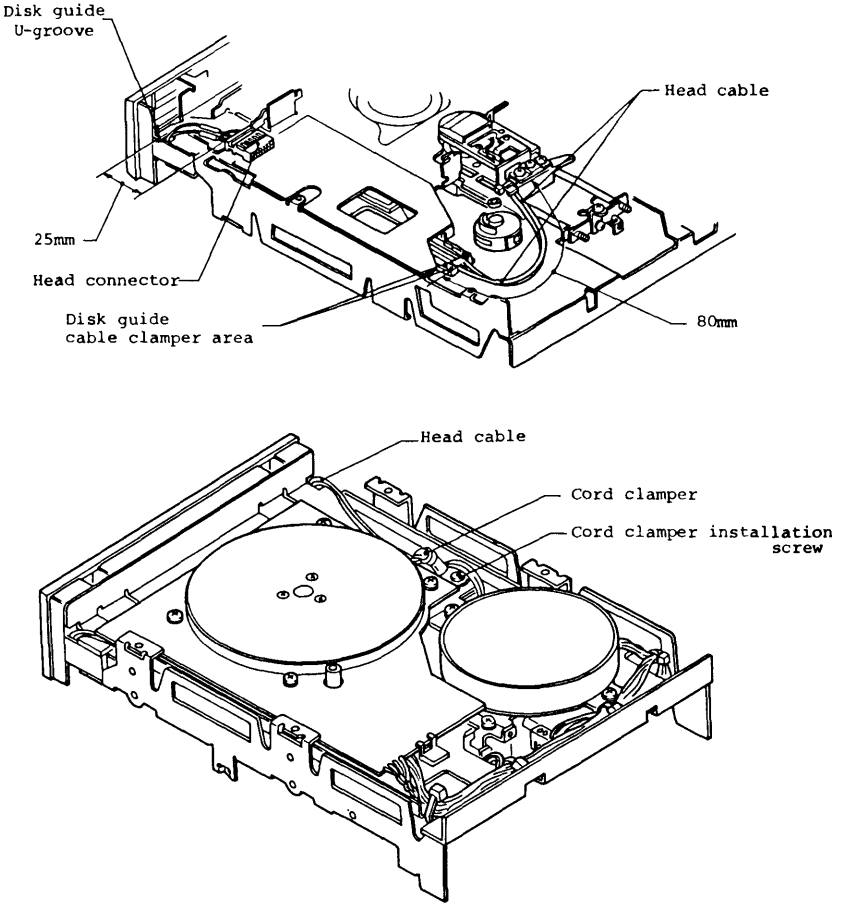
4-2-3. Head Cable Treatment

Head cable should be arranged correctly by the clampers with appropriate margin in length so that the head carriage can move on the guide shafts smoothly.

(1) Clamp the head cable with cable clamper area of the disk guide so that the cable has appropriate looseness when the head carriage is set to track 00 (rear end of the moving area). The appropriate length of the head cable from the head carriage output to the cable clamper is approximately 80mm (see Fig.406).
Also confirm that the head cable do not touch the tail end of the steel belt.

(2) Thread the head cable through the hole of the disk guide and arrange it under the chassis to hold with a cord clamper. There should be no excessive looseness of the cable between the cable clamper and the cord clamper which may cause undesirable contact of the cable to the disk when inserted. The cable length between the cable clamper and the cord clamper is 65mm, approx.

(3) Remove the front bezel according to item 4-5-9. Thread the head cable along the U-groove of the disk guide and pull it up on the chassis to connect it to the head connector, J9. The cable length between the U-groove of the disk guide and the head connector is 25mm, approx. (see Fig.406).
If the head cable is too long, turn the cable around the cord clamper under the chassis.



Note: The figure uses the double sided FDD. The same cable arrangement is applied to the single sided FDD.

(Fig.406) Head cable arrangement

4-2-4. Initial Setting of SKA

Following initial setting is required for operating the SKA.

Note: Use matched SKA for the FD-54 series. The SKA for the FD-54 has 430Ω terminator at the interface receiver which is different from that conventionally used 150Ω terminator for the FD-55 series. As to the other performance, SKA for the FD-54 and for the FD-55 are the same.
The SKA for the FD-54 series can also be used in the FD-55 series.

4-2-4-1. Cable connection and setting of power supply voltage

(1) Set the output voltage of DC power supply to +12V and +5V, approx.

(2) Turn the DC power off and connect the power cable to the PSA (SKA PWR) connector of the SKA.

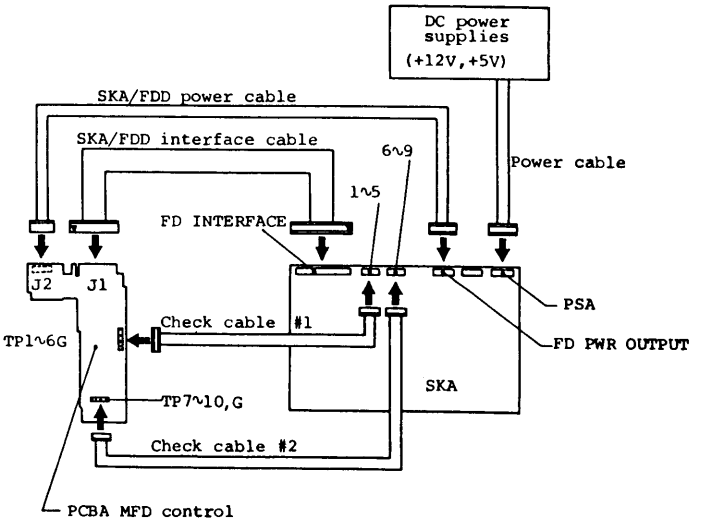
(3) Set the FD PWR switch of the SKA to the OFF position.

(4) Connect the FD PWR OUTPUT of the SKA and the FDD with the SKA/FDD power cable.

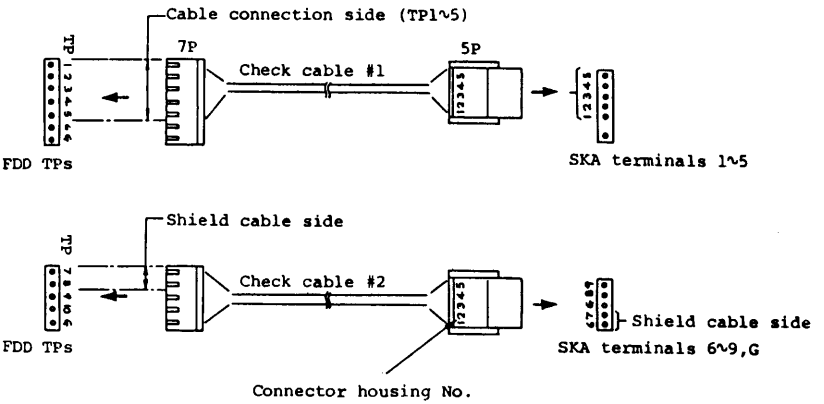
(5) Connect the SKA/FDD interface cable. Pay attention to the identification mark of the connector (▽) so that it locates at the pin 1 and 2 side.

(6) Connect the check cable #1 (Flat cable, 7P connector at the FDD side and 5P connector at the SKA side) between the terminals 1 ∿ 5 of the SKA and TP1 ∿ TP6, G of the FDD. For the SKA side, be sure to match the pin numbers of the connector housing and the terminal numbers of the connector. For the FDD, cable connection side pins should be connected to the TP1 ∿ 5 side.

(7) Connect the check cable #2 (shield cable is used partially, 5P connectors



(Fig.407) Connection of SKA cable



(Fig.408) Connection of check cable

at both ends) between the terminals 6 ∿ 9, G of the SKA and TP7 ∿ TP10, G of the FDD. Be sure to match the pin numbers of the connector housing and the terminal numbers of the SKA as in Fig.408.
The shield cable side is TP7, 8, and terminals 6, 7 of the SKA.

(8) Turn the DC power on. Set the FD PWR switch of the SKA to the PSA side.

(9) Key in "CB". (+5V VOLTAGE)

(10) Adjust the DC power voltage so that the DATA indicator of the SKA □□.□□ (V) indicates the value within the range of 5.00±0.1V.

(11) Key in "F". (STOP)

(12) Key in "CC". (+12V VOLTAGE)

(13) Adjust the DC power voltage so that the DATA indicator of the SKA □□.□□ (V) indicates the value within the range of 12.00±0.24V.

(14) Key in "F". (STOP)

Note: The above items (1), (2), (9) ∿ (14) may be omitted for replacement of the FDD or a temporary FDD power off. Remain DC power on and control the FDD power by the SKA PWR switch.

4-2-4-2. Setting of the maximum track number

Before the check and the adjustment of the FDD, set the maximum track number according to the following instructions.
Usually the maximum track number is set to 79 at the initial setting, change it to 39.
The setting will be maintained until the main DC power (for SKA) is turned off, or until the RESET switch of the SKA is depressed. Since the FD PWR switch is independent of this setting, it is convenient to maintain the main DC power on for the successive operations.

(1) Key in "CF" (SET TMAX)

(2) The maximum track number set at that time is indecated with the latter two digits of the DATA indicator □□□□ (track).

Note: If there is no change in the maximum track number in item (2), depress "F" key.

(3) Key in the maximum track number (39) of the FDD in two digits of decimal notation.

e.g. MAXIMUM TRACK NUMBER 39 (40 cylinders): CF 39

4-2-4-3. Setting of step rate and settling time

Generally, the step rate and the settling time of the FDD is the same as the initial value of the SKA (step rate: 6msec, settling time: 15msec) and no initial setting is required.
For the confirmation or the change of the initial setting, execute according to the following procedure. Once the setting is done, it will be maintained until the main DC power (for SKA) is turned off, or until the RESET switch of the SKA is depressed.

(1) Key in "DB". (SET STEP RATE)

(2) Step rate set at that time is indicated by 0.1msec scale on the DATA indicator □□□□ (ms).

e.g. DATA indicator □□60 indicates 6.0msec.

(3) Key in a new step rate down to one decimal place (unit: msec).

Note: If there is no change in step rate in item (2), omit item (3) and forward to item (4).

(4) Key in "F". (STOP -- Setting of the step rate completes.)

(5) Settling time at that itme is indicated by 0.1msec scale on the DATA indicator □□□□ (ms).

e.g. DATA indicator □150 indicates 15.0msec.

(6) Key in new settling time down to one decimal place (unit: msec).

Note: If there is no change in settling time in item (5), omit item (6) and depress "F" key to complete the operation.

(7) Depress "F" key. (STOP -- Setting of the settling time completes.)

e.g. STEP RATE 6msec, SETTLING TIME 15msec : DB 30 F 150 F

4-2-4-4. Level disk calibration

Setting of the following calibration value is required for accurate measurement before the check of the read level or the resolution. Use a level disk with a calibration value (100% center) written on the label. The setting will be maintained until the main DC power (for SKA) is turned off or unitl the RESET switch of the SKA is depressed. If the calibration value is the same as the initial value (100%) of the SKA, the initial setting of the following is not required.

(1) Innermost track read level

(a) Key in "D0". (CALIBRATION READ LEVEL)

(b) Calibration value set at that time is indicated in the latter three digits of the DATA indicator □□□□ (%).

(c) Key in a new calibration value written on the level disk label (three digits, Max.)

(d) Key in "F". (STOP)

Note: If there is no calibration change in item (b), omit item (c) and depress "F" key.

(2) Innermost track resolution

(a) Key in "D1". (CALIBRATION RESOLUTION)

(b) Calibration value set at that time is indicated in the latter three digits of the DATA indicator □□□□ (%).

(c) Key in a new calibration value written on the level disk label (three digits, Max.)

(d) Key in "F". (STOP)

Note: If there is no calibration change in item (b), omit item (c) and depress "F" key.

e.g. READ LEVEL 103%, RESOLUTION 96%: D0 103 F, D1 96 F

4-2-4-5. Alignment disk calibration

Setting of the following calibration value is required for accurate measurement before the check and adjustment of the track alignment. Use a correctly calibrated (0% center) alignment disk with a calibration value written on the label. The setting will be maintained until the main DC power (for SKA) is turned off or until the RESET switch of the SKA is depressed.
If the calibration value is the same as the initial value (0%) of the SKA, the initial setting of the following is not required.

(1) SIDE 0 alignment

(a) Key in "E0". (CALIBRATION SIDE 0 ALIGNMENT)

(b) The calibration value set at the time is indicated in the latter two digits of the DATA indicator □□□□ (%), and the polarity is indicated in the initial digit. If a "0" is indicated, the polarity is positive.
Polarity indication: plus /, minus -

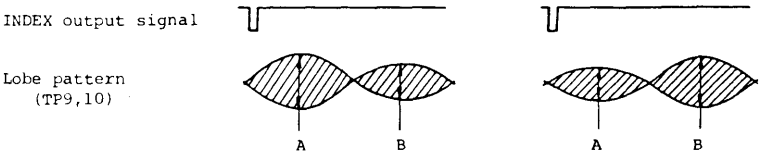
(c) Key in a polarity and a new calibration value (two digits, Max.) written on the alignment disk label.
Designation of polarity: Depress "B" key only for minus designation. (No designation is required for plus).

(d) Key in "F". (STOP)

(2) Side 1 alignment (Double sided only)

(a) Key in "E1". (CALIBRATION SIDE 1 ALIGNMENT)

(b) The same as in item (1)-(b) ∿ (d).



Notes: 1. The lobe pattern ratio is calibrated in the SKA according to the following expression.

$$\text{Lobe pattern ratio after calibration} = \frac{\text{A-B}}{\text{Larger one of A \& B}} \times 100 - \text{Calibration valu}$$

2. If the calculated value with the above expression is positi the polarity is plus, while the polarity is minus when the value is negative.

(Fig.409) Calibration of alignment lobe pattern

(3) Index burst timing

(a) Key in "E5". (CALIBRATION INDEX TIMING)

(b) The calibration value set at that time is indicated in the latter three digits of the DATA indicator □□□□ (μs), and the polarity is indicated in the initial digit. (Refer to item (1)-(b)). If a "0" is indicated, the polarity is positive.

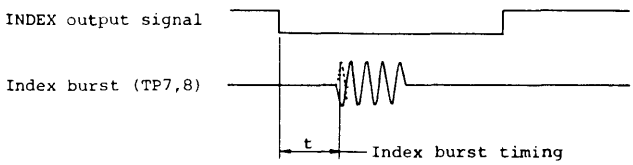
(c) Key in a polarity and a new calibration value (three digits, Max.) written on the alignment disk label. Refer to item (1)-(c) for the polarity designation.

(d) Key in "F". (STOP)

Note: If there is no change in the calibration value in item (b), omit

item (c) and depress "F" key.

e.g. Double sided FDD, SIDE 0 ALIGNMENT +3%, SIDE 1 ALIGNMENT -5%,
INDEX TIMING -25μs:
E0 3 F, E1 B 5 F, E5 B 25 F



Notes: 1. The index timing is calibrated in the SKA according to the following expression.

Calibrated timing = t - calibration value (μs)

2. If the calculated value with the above expression is positive, the polarity is plus, while the polarity is minus when the value is negative.

(Fig.410) Calibration of index burst timing

4-2-4-6. Humidity setting

For the check and adjustment of the track alignment using an alignment disk, set the environmental relative humidity to the SKA in order to improve the precision of measurement.
This setting is important when the relative humidity is considerably different from 50%.
The initial setting of the following is not required if the relative humidity is the same as the initial value (50%) of the SKA.

(1) Key in "E2". (CALIBRATION RH ALIGNMENT)

(2) The relative humidity set at that time is indicated in the latter two digits of the DATA indicator □□□□ (%).

(3) Input the relative humidity percentage in the measurement environment (two digits, Max.).

e.g. RELATIVE HUMIDITY 58%: E2 58

4-2-4-7. Setting of SKA gain

For this FDD, the SKA gain should be maintained at the initial state (H GAIN indicator is off). If the H GAIN indicator turns on by an erroneous key-in, turn it off by keying in "DD".

4-2-5. Others

(1) Total error test

In the check and adjustment in item 4-4, read/write error test is not included. After the adjustment or the replacement of the maintenance parts, it is recommended to perform a data error test by connecting the FDD to the user's system or the TEAC simulator KB. The window margin test is the most recommended item.

(2) Setting of FDD straps

It is required to confirm before the operation that the straps (short bars) on the PCBA MFD control are at the appropriate position for the system to be used in the check and adjustment.
When the SKA is used, depress a key which number is the same as the on-state short bar among DS0 ∿ 3 straps of the FDD and confirm that the indicator is on before various key operations.
If the IU short bar is on, you can turn on the front bezel indicator by "A" (IN USE) key of the SKA.

Notes: 1. For simplifying the explanation, following shows only the case when the DS0 short bar is on.
2. If the strap position of the FDD is changed from the initial setting at the system installation, be sure to change it back to the initial position after the maintenance operations.

(3) Connection of the probe ground

Connect the probe ground of the equipment as follows:

(a) For the observation at the test points (TP) 7 ∿ 10:
Connect the probe ground to the G test point (0V) on the PCBA MFD control.

(b) For the observation at the other test point:
Connect the probe ground to the G test point (0V) on the PCBA MFD control. Or GND (0V) terminal of the system power supply unit, or the SKA GND terminal may be used.

(c) For the observation of the SKA test point:
Connect the probe ground to the SKA GND terminal.

Note: When you use the SKA, almost all checks including the read amp. output at TP7 ∿ TP10 of the FDD will be done automatically through the check cables #1 and #2 and interface cable. Also these signals can be observed by an oscilloscope using the test points on the SKA.

(4) Maintenance environment

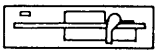
Maintenance of the FDD should be done on a clean bench at room temperature and humidity. It is recommended to execute the check and adjustment of the track alignment after leaving the FDD for at least 2 hours at room temperature and humidity. The magnetic head, disk, steel belt, etc. might suffer from dust and dirt if the maintenance is not undertaken in a clean environment.

(5) Orientation of the FDD

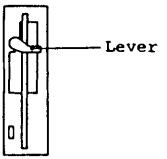
Position the FDD as shown in Fig.411 unless otherwise specified. Horizontal and vertical orientations with lever side up should be used.

(6) Head load

The FD-54 series have no head load solenoid. They are always in head load condition as far as a disk is inserted and the front lever is closed.



Horizontal setting



Vertical setting

(Fig.411) General orientation of the FDD during maintenance

(7) Work disk

When you use the SKA, use a soft sectored disk.

4-3. PREVENTIVE MAINTENANCE

4-3-1. Cleaning of Magnetic Head by Cleaning Disk

When you use the FDD in dusty environment, it is recommended to clean the magnetic head surface periodically (e.g. once a month) with a commercially available cleaning disk. Especially for a double sided FDD, it is difficult to clean the head surface, be sure to use the cleaning disk.
For typical usage under typical environmental condition, the cleaning is recommended when data errors often occur.

(A) Equipment

(1) Cleaning disk
(2) SKA or user's system

(B) Cleaning procedure

(1) General method

(a) Start the spindle motor and install an appropriate cleaning disk.

Notes: 1. Do not use a damaged cleaning disk on the surface.
2. For a single sided FDD, be sure to install a single sided cleaning disk. The cleaning surface of the disk should be in contact with the head surface.
When the FDD is placed horizontally, the magnetic head is located down and it faces the back side of the disk.
If a double sided cleaning disk is installed in a single sided FDD, it may damage the head pad.
3. For a double sided FDD, a double sided cleaning disk should be used. Side 0 (lower side) and side 1 (upper side) heads are cleaned simultaneously.

(b) Clean the head at a suitable track position for 10 ∿ 30 seconds, approx. In order to avoid the concentration on a specific track, it is a good way to make the head move between track 00 and the innermost track during cleaning.

Note: The most appropriate cleaning time is different for each type of cleaning disk used.
Excessively long cleaning time is not effective but has possibility to accelerate the head wear.

(c) Remove the cleaning disk.

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Start the spindle motor by key "5". (MON indicator turns on).

(c) Execute drive select by key "0". (DS0 indicator turns on).

(d) Key in "C0" and confirm that the TRACK indication of the SKA becomes "00". (RECALIBRATE)

(e) Install an appropriate cleaning disk. See item (1)-(a), "Notes".

(f) Key in "C6". (SEEK TEST)

(g) After 10 ∿ 30 seconds, depress "F" key.

(h) Eject the cleaning disk.

4-3-2. Direct Cleaning (Single sided FDD only)

This cleaning method is applied only to a single sided FDD.
If this method is applied to a double sided FDD, gimballed mechanism of the head might be damaged.
If visible dirt is on the head surface when the head pad arm is lifted up manually during maintenance, perform direct cleaning as follows:

(A) Equipment

(1) Absolute alcohol (Ethanol)
(2) Cotton swab or gauze

(B) Cleaning procedure

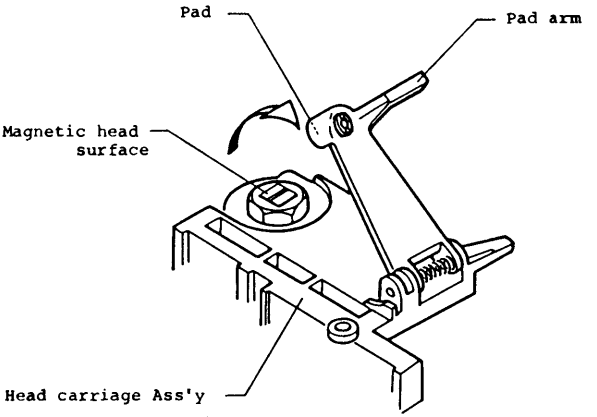
(1) Lightly dampen a cotton swab or a gauze with alcohol.

(2) Lift up the pad arm (see Fig.412) and clean the head surface carefully with the cotton swab or the gauze.

Note: Do not touch the pad surface.

(3) Wipe the head surface with clean dry cloth after the evaporation of the alcohol.

(4) After confirming that the dirt is cleaned off and no fluff is left on the head surface, let the pad arm down carefully.



(Fig.412) Direct cleaning of magnetic head (Single sided only)

4-4. CHECK AND ADJUSTMENT

4-4-1. Adjustment of Collet Shaft Plate

(A) Equipment

(1) Cross point screwdriver, M3
(2) Locking paint

(B) Adjustment procedure

(1) Remove two fixing screws of the shield cover (see Fig.413) and remove it.

(2) Loosen two fixing screws of the collet shaft plate Ass'y so that the collet shaft plate can be moved manually without getting out of place.

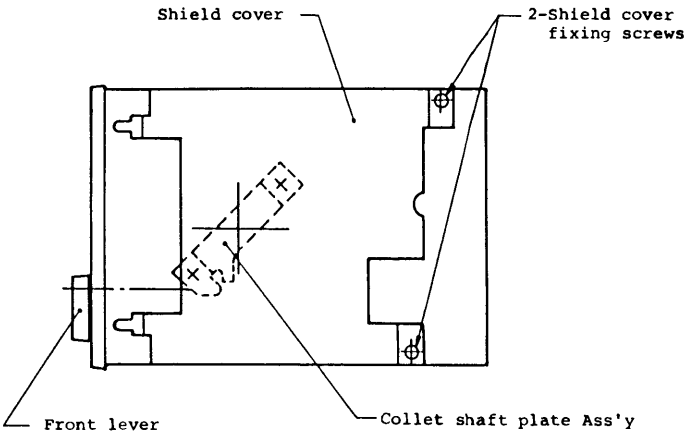
(3) Clamp the collet by turning the front lever.

(4) In this condition, adjust the collet shaft plate and tighten two fixing screws with the specified torque so that the visual distance of the gap between the collet shaft and the hole of the collet holder becomes even (see Fig.414).

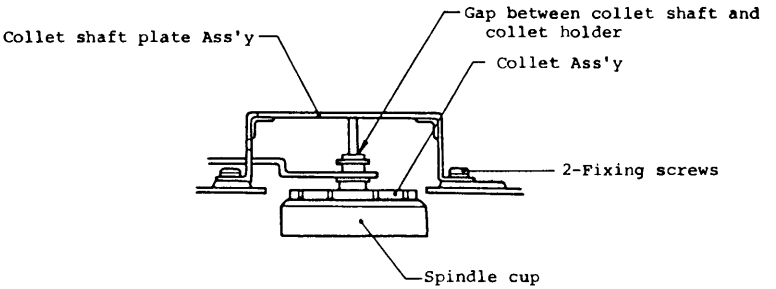
(5) Up and down the collet by turning the front lever and confirm that it does so smoothly without being cought by the spindle cup.

(6) Apply a drop of locking paint of the fixing screws.

(7) Install the shield cover in the reverse order of item (1).



(Fig.414) Location of collet shaft plate



'Fig.413) Gap of collet shaft plate

4-4-2. Adjustment of Front Lever Position

(A) Equipment

(1) Hexagon wrench key, 1.5mm
(2) MAX media jig (Jig D)

(B) Adjustment procedure

(1) Turn the front lever to close position and loosen a lever fixing set screw to pull out the lever for 0.5mm, approx.

(2) Tighten the set screw.

(3) Turn the front lever to open position and insert the MAX media jig as shown in Fig.415 (the notch side to be left).

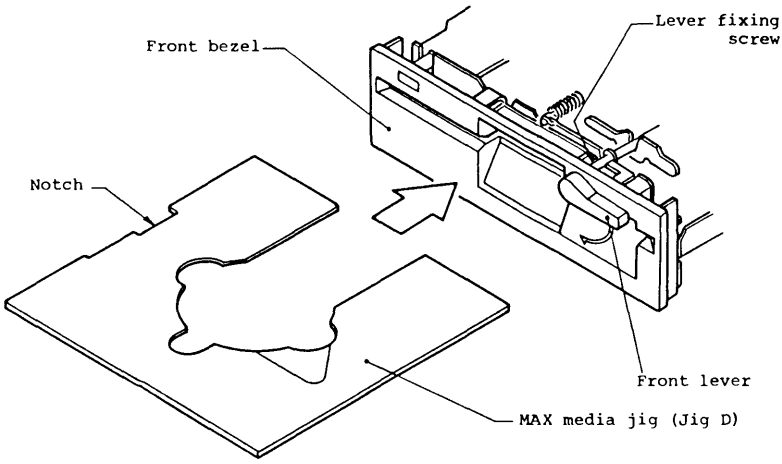
(4) Turn the front lever to close position and loosen the set screw again. Then push the lever against the MAX midia jig.
Confirm that the pin of the lever shaft goes into the slot of the front lever.

(5) Position the handle of the front lever forms right angle against the longitudinal side of the front bezel. And tighten the set screw with the specified torque. (See Fig.416).

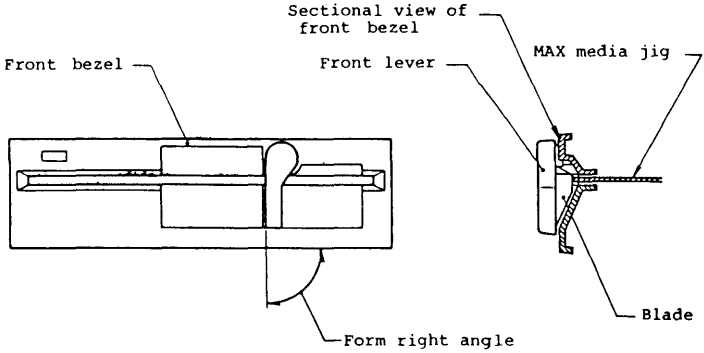
(6) Close the front lever and confirm that the blade of the lever does not nip the MAX media jig.

(7) Open the front lever and remove the jig.

Note: Refer to item 4-2-1 as to handling of the set screws.



(Fig.415) Adjustment of front lever



(Fig.416) Front lever position

4-4-3. Check and Adjustment of Disk Pad Lever (Bail)

This item applies only to the double sided FDDs.

(A) Equipment

(1) Cross point screwdriver, M2.6
(2) Binding agent

(B) Check and adjustment procedure

(1) Open the front lever to be able to insert the disk.

(2) Confirm a little gap (0.1 ∿ 0.3mm, approx.) is spaced between the bail and the top of the stop cam of the CSS Ass'y (C). (See Fig.418).

(3) If the item (2) is not satisfied, turn the outside adjusting screw (see Fig.417) of the bail so that the bail and the top of the stop cam are separated with 0.2mm, approx.

(4) In the process of inserting a disk slowly, confirm that the disk jacket does not touch the side 0 nor the side 1 head and goes into the FDD smoothly with appropriate space margin.

(5) Open and close the front lever two or three times to confirm the clampings of the disk are done smoothly.

(6) In the process of ejecting the disk slowly, confirm that the side 0 and side 1 heads do not catch the head window edge of the disk jacket (opening area of the jacket to make the head be in contact with the disk surface) and that the disk can be drawn out smoothly with appropriate space margin.

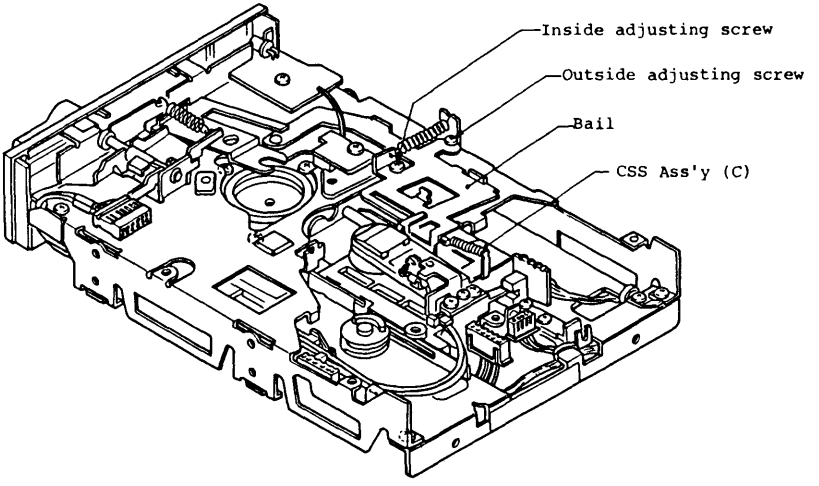
(7) Insert the disk again and close the front lever.

(8) Confirm that a little gap (0 ∿ 0.5mm, approx.) is spaced between the stop cam and the disk jacket without activating the stop cam of the CSS Ass'y when the disk jacket is depressed lightly with a finger from the front bezel side.

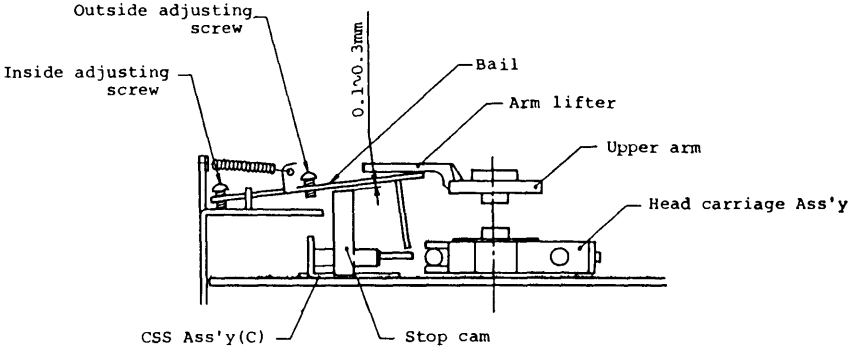
(9) If the item (8) is not satisfied, turn the inside adjusting screw (see Fig. 417) of the bail so that the gap between the disk jacket and the stop cam becomes 0.1 ∿ 0.2mm, approx.

(10) Apply binding agent to the two adjusting screw to fix it to the bail.

(11) Open the front lever to draw out the disk.



(Fig.417) Adjustment of bail



Note: The figure is viewed from the front bezel side.

(Fig.418) Gap of bail and stop cam

4-4-4. Check of File Protect Sensor

(A) Equipment

(1) MAX media jig (Jig D)
(2) Digital voltmeter (or oscilloscope)
(3) SKA or user's system

(B) Check procedure

(1) General method

(a) Place the FDD on the work bench with the LED indicator up and the front lever down. (See Fig.421).

(b) Connect a digital voltmeter or an oscilloscope (DC range,1V/div) to TP6 (File protect sensor) on the PCBA MFD control.

(c) Install the MAX media jig as in Fig.421 and set it so that the notch A area is located on the light pass from the file protect sensor.

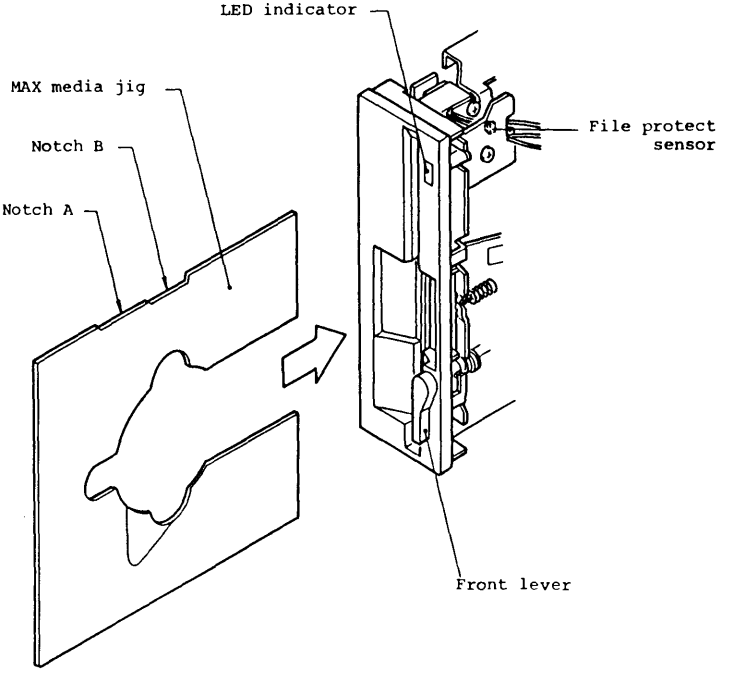
(d) Adjust the orientation of the FDD so that it is not exposed with strong light outside.

(e) Confirm that the voltage measured at TP6 when power is supplied to the FDD is within the following range.
Notch A position TP6 voltage: 0.5V, Max.

(f) Pull out the jig a little so that the notch B area is located on the light pass.

(g) Confirm that the voltage measured at TP6 when power is supplied to the FDD is within the following range.

Notch B position TP6 voltage: 3V, Min.



(Fig.421) Check of file protect sensor

(2) SKA method

(a) Connect the SKA according to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Execute the general method described in item (1)-(a) through (e). WRROT indicator of the SKA turns on when drive selection is executed by key "0". (DS0 indicator turns on).

(c) Execute the general method described in item (1)-(f) and -(g). WRROT indicator of the SKA turns off.

4-4-5. Check and Adjustment of Disk Rotation Speed

This item is only applied to the FDD which has a DD motor Ass'y with the variable resistor R1 for adjusting the rotational speed of the disk on the PCBA DD motor servo. Refer to Fig.311 as to the mounting position of the variable resistor R1.
For the DD motor Ass'y without the variable resistor, the rotation speed is fixed by the ceramic oscillator in the servo circuit and no adjustment is required.

(A) Equipment

(1) Common screwdriver, small size
(2) SKA or user's system
(3) Frequency counter (not required when the SKA is used)
(4) Work disk (soft sectored)

(B) Check and adjustment procedure

(1) General method

(a) Connect the frequency counter to TP4 (Index) of the PCBA MFD control or to the INDEX interface signal line.

(b) Start the spindle motor and install a work disk.

(c) Set the head to track 00.

(d) Confirm that the pulse interval at TP4 is within the following range.
TP4 pulse interval: 200±3msec

(e) If the value in item (d) is out of the specified range, adjust the variable resistor R1 on the PCBA DD motor servo to obtain the median value in the specified range in item (d).

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to PSA side.

(b) Start the spindle motor by key "5". (MON indicator turns on).

(c) Insert a soft sectored work disk.

(d) Execute drive select by key "0". (DS 0 indicator turns on).

(e) Key in "C0" and confirm that TRACK indication becomes "00". (RECALIBRATE)

(f) Key in "C3". (INDEX PERIOD)

(g) Confirm that the DATA indicator □□.□ (ms) indicates a value within the following range.
INDEX interval: 200.0±3.0msec

(h) If the value in item (g) is out of the specified range, adjust the variable resistor R1 on the PCBA DD motor servo to obtain the median value in the specified range in item (g).

4-4-6. Check and Adjustment of Head Touch

Note: The adjustment applies to a single sided FDD only.

(A) Equipment

(1) Work disk
(2) Common screwdriver, small size
(3) SKA or user's system
(4) Oscilloscope (not required when the SKA is used)
(5) DC clip on ammeter (not required when the SKA is used)
(6) Locking paint

(B) Adjustment procedure

(1) General method

(a) Connect an oscilloscope to TP9 or TP10 (Differentiation amp.) on the PCBA MFD control.
Oscilloscope range: AC mode, 0.2V

(b) Start the spindle motor and install a work disk.

(c) Set the head to the innermost track.

(d) Repeat the cycle of one write rotation and one read rotation.
Write data should be the fixed pattern of 2F (250KHz of WRITE DATA frequency).

(e) Write down the average read level measured during the read operation of item (d).

(f) Execute item (d) and (e) with a slight depression (very slight depression easy to release: 10 ∿ 20g) by a finger on the top of the upper head (double sided) or of the pad arm (single sided), and measure the average read level as in item (e).

(g) Confirm that the read level measured in item (e) is greater than 80% of that in item (f).

(h) For a double sided FDD, execute items (d) through (g) respectively for the side 0 and the side 1 heads.

(i) After making the head move to track 00, execute items (d) through (h).

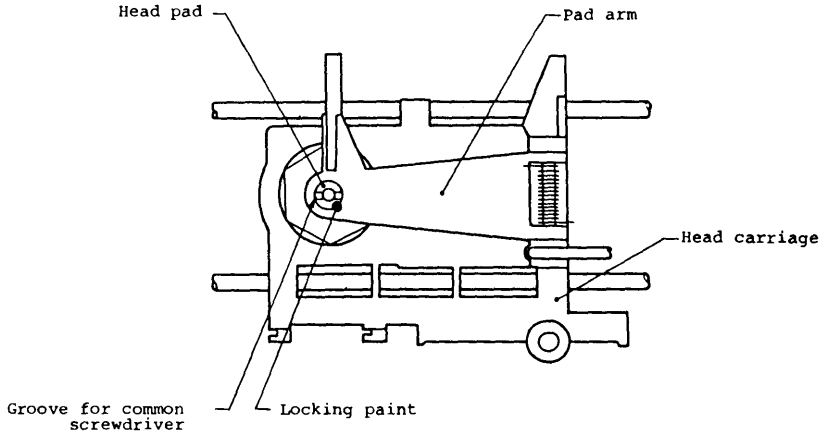
(j) Head touch adjustment for a single sided FDD:

i) At the innermost track, turn the groove on the upper side of the head pad by 30° steps, approx. with a common screwdriver (see Fig.420). At each turning of the groove, execute write and read operations in item (d).
Be sure to take apart the common screwdriver from the head pad during write or read operation.

Note: Be careful not to push the head pad strongly with the common screwdriver. Also do not touch the pad surface to which a disk will be in contact.

ii) After turning the pad position around 360°, set the position again to the position where the highest read level was obtained. Then execute items (d) through (g) at the innermost track.

iii) Continue the operation until the items (g) and (i) are sufficiently satisfied. Following causes are assumed for the insufficient result in item (g) or (i) after fine adjustment of the pad position.



(Fig.420) Adjustment of head pad position (single sided FDD)

① Inferior head pad:
Replace the pad according to item 4-5-8.

② Inferior disk:
Disk and/or jacket is deformed or damaged. Replace the work disk with a new one.

③ Inferior head:
Replace the head carriage Ass'y according to item 4-5-1.

iv) Remove the work disk and apply a drop of locking paint around the rotating area of the head pad. Be careful not to smear the groove for common screwdriver with the locking paint.

(k) Possible causes for the insufficient head touch in a double sided FDD:

Following causes are assumed for the insufficient result in items (g) through (i) on a double sided FDD.

i) Inferior disk:

Disk and/or jacket is deformed or damaged. Replace the work disk with a new one.

ii) Inferior head flexture:

Because of the failed performance of the bail or the CSS Ass'y in item 4-4-3, the flexture on which the head piece is located may be deformed. Remove the disk. Then open and close the front lever slowly to observe the gap between the side 0 and the side 1 heads from the front bezel. If the two head surfaces are not in parallel each other, it is considered to be the deformation.
Replace the head carriage Ass'y according to item 4-5-1.

(2) SKA method

(a) Connect the SKA according to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Start the spindle motor by key "5". (MON indicator turns on). Install a work disk and execute drive select by key "0". (DS0 indicator turns on).

(c) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(d) Key in "C1" (SEEK TMAX)

(e) Key in "D3". (WRITE/READ LEVEL PRE 2F)

(f) Write 2F and read operations are repeated.
The DATA indicator □□□□ (mV) indicates the average read level of TP7 and TP8 (Pre-amp.) after each cycle of operation (one rotation of write and one rotation of read) is finished.

(g) Observe the DATA indicator □□□□ (mV) with a slight depression (very slight depression easy to release: 10 ∿ 20g) by a finger on the top of the upper head (double sided) or of the pad arm (single sided).

(h) Confirm that the read level measured in item (f) is more than 80% of that in item (g).

(i) For a double sided FDD, depress "F" key to stop and then depress "4" key to execute items (e) through (h) for the side 0 and the side 1 heads respectively. The side is changed alternately by a depression of "4" key. If side 1 is selected, SIDE 1 indicator of the SKA turns on.

(j) Key in "C0" (RECALIBRATE) and execute items (e) through (i) in the similar way.

(k) Head touch adjustment for a single sided FDD:
Refer to item (j) of "General method".

(L) Possible causes for the inferior head touch in a double sided FDD:
Refer to item (k) of "General method".

4-4-7. Check and Adjustment of Asymmetry

(A) Equipment

(1) Work disk
(2) SKA or user's system
(3) Oscilloscope

(B) Check and adjustment procedure

(1) General method

(a) Connect an oscilloscope to TP5 (Read data) on the PCBA MFD control or to the READ DATA interface line.
Oscilloscope range : DC mode, 2V, 1μsec

(b) Start the spindle motor and install a work disk.

(c) Set the head to the innermost track.

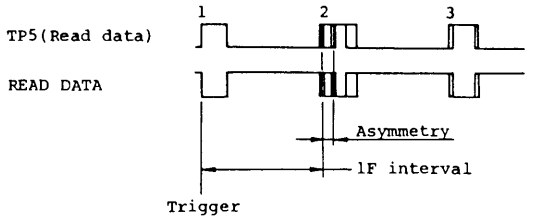
(d) Execute 1F write operation (125KHz of WRITE DATA frequency).

(e) Measure the asymmetry referring to Fig.421.

Note: Oscilloscope should be so set that three read data pulses can be observed. Asymmetry width should be measured at the second read data pulse from the trigger pulse.

(f) Confirm that the asymmetry is within the following range.
Innermost rrack 1F asymmetry : 0.6μsec, Max.

(g) For a double sided FDD, execute items (d) through (f) for the side 0 and the side 1 heads respectively.



(Fig.421) Measurement of asymmetry

(h) If the value in item (f) or (g) is out of the specified range, adjust according to the following procedure.
The adjustment can be done only for the PCBA versions or the PCBA revision numbers with the variable resistor R5 on the PCBA MFD control. No adjustment can be done without R5.

i) Adjust the variable resistor R5 so that the asymmetry takes the minimum value while repeating 1F write and 1F read operations alternately.

ii) For a double sided FDD, repeat the operation in item i) for the side 0 and the side 1 heads alternately. The variable resistor shall be so adjusted that both asymmetry for side 1 and side 0 heads take the minimum value.

(i) If the values in items (f) and (g) are out of the specified range in the PCBA without the variable resistor R5, or if the adjustment in item (i) cannot be done sufficiently even if R5 is mounted, following causes are assumed.

i) Leakage flux density in the environmental condition of the FDD is high:
If there is some flux source near the FDD such as magnet, transformer, motor, Brown tube, magnetized iron plate, etc., take

it apart from the FDD. Then measure the asymmetry and adjust again.

ii) Inferior disk:

Replace the work disk.

iii) Inferior head:

Replace the head carriage Ass'y according to item 4-5-1.

iv) Inferior PCBA MFD control:

Replace the PCBA according to item 4-5-6.

(2) SKA method

(a) Connect the SKA according to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Key in "B1F". (1F DUTY)

(c) Connect an oscilloscope to the DOUT terminal of the SKA.
Oscilloscope range : DC mode, 2V, 0.2μsec

(d) Start the spindle motor by key "5". (MON indicator turns on).

(e) Install a work disk.

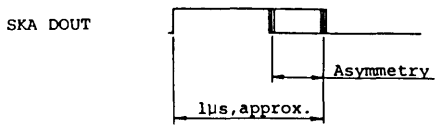
(f) Execute drive select by key "0". (DS0 indicator turns on).

(g) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(h) Key in "C1". (SEEK TMAX)

(i) Key in "D4". (WRITE/READ LEVEL PRE 1F)

(j) Measure the asymmetry as in Fig.422.



(Fig.422) Measurement of asymmetry (SKA)

(k) Confirm that the asymmetry is within the following range.
Innermost track 1F asymmetry : 0.6μsec, Max.

(L) For a double sided FDD, depress "4" key and execute items (i) through (k) for the side 0 and the side 1 heads respectively. The side is changed alternately by a depression of "4" key. If side 1 is selected, SIDE 1 indicator of the SKA turns on.

(m) If the value in item (k) or (L) is out of the specified range, adjust according to the following procedure. The adjustment can be done only for the PCBA versions or the PCBA revision numbers with the variable resistor R5 on the PCBA MFD control. No adjustment can be done without R5.

i) Adjust the variable resistor R5 so that the asymmetry takes the minimum value by keying in "D4".

ii) For a double sided FDD, execute the operation in item i) for both sides alternately by chainging the side by key "4". The variable resistor shall be so adjusted that both asymmetry for side 1 and side 0 heads take the minimum value.

(n) If the values in items (K) and (L) are out of the specified range in the PCBA without the variable resistor R5, or if the adjustment in item (m) cannot be done sufficiently even if R5 is mounted, refer to item (j) of "General method".

4-4-8. Check of Read Level

(A) Equipment

(1) Level disk
(2) SKA or user's system
(3) Oscilloscope (not required when the SKA is used)

(B) Check procedure

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP9 and TP10 (Differentiation amp.) on the PCBA MFD control.
Oscilloscope range : AC mode, 0.5V
Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and ADD both channels.

(b) Start the spindle motor and install a level disk.

(c) Make the head move to the innermost track.

(d) Execute 2F write operation for one rotation of the disk (250KHz of WRITE DATA frequency).

(e) Measure the average amplitude (Vp-p) of the read waveform as in Fig.423.

(f) Calculate the read level by substituting the following expression with the measured value in item (e) and READ LEVEL calibration value (see level disk label).

$$\text{Read level (true value)} = \text{Measured value} \times \frac{100}{\text{Calibration value}}$$

(Fig.423) Measurement of average read level (2F)

(g) Confirm that the true value of the read level is within the following range.
Innermost track read level : 1.4Vp-p, Min.

(h) For a double sided FDD, execute items (d) through (g) for the side 0 and the side 1 heads respectively.

(i) If the value in item (g) or (h) is out of the specified range, following causes are assumed.

i) Inferior disk:
Disk and/or jacket is deformed or damaged. Replace the level disk with a new one.

ii) Abnormal disk rotational speed:
Check and adjust according to item 4-4-5.

iii) Inferior head touch:
Check and adjust according to item 4-4-6.

iv) Inferior head:
Replace the head carriage Ass'y according to item 4-5-1.

v) Inferior PCBA MFD control:
Replace the PCBA MFD control according to item 4-5-6.

(k) Eject the level disk and release the Invert and ADD modes of the oscilloscope.

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Start the spindle motor by key "5". (MON indicator turns on).

(c) Install a level disk.

(d) Execute drive select by key "0". (DS0 indicator turns on).

(e) Key in "C0" and confirm that the TRACK indication becomes "00". (RECALIBRATE)

(f) Key in "C1". (SEEK TMAX)

(g) Key in "D7". (WRITE/READ LEVEL DIF 2F)
Calibration value of the level disk should be set previously in the SKA.

(h) Confirm that the DATA indicator □□□□ (mVo-p) indicates the value within the following range.
Innermost track read level : 700mVo-p, Min.

(i) For a double sided FDD, depress key "4" and execute items (g) and (h) for the side 0 and the side 1 heads respectively. The side is changed alternately by a depression of "4" key. If the side 1 is selected, SIDE 1 indicator of the SKA turns on.

(j) If the value in item (h) or (i) is out of the specified range, refer to item (i) of "General method".

(k) Eject the level disk.

4-4-9. Check of Resolution

(A) Equipment

(1) Level disk
(2) SKA or user's system
(3) Oscilloscope (not required when the SKA is used)

(B) Check procedure

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP7 and TP8 (Pre-amp.) on the PCBA MFD control.
Oscilloscope range : AC mode, 50mV ∿ 0.1V
Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and ADD both channels.

(b) Start the spindle motor and install a level disk.

(c) Make the head move to the innermost track.

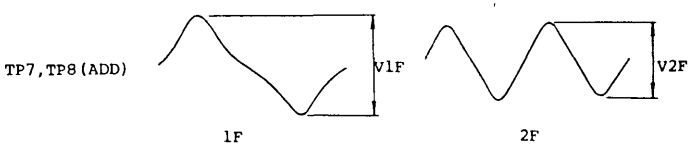
(d) Execute 1F write operation for one rotation of the disk (125KHz of WRITE DATA frequency).

(e) Measure the average amplitude (V1F) as in Fig.424.

(f) Execute 2F write operation as in item (d) (double in frequency to that in item (d)).

(g) Measure the average amplitude (V2F) as in Fig.424.

(h) Calculate the resolution by substituting the following expression with the measured values V1F, V2F, and RESOLUTION calibration value (see level disk label).



(Fig.424) Measurement of resolution

Resolution (true value) = V2F/V1F x 100/Calibration value (%)

(i) Confirm that the true value is within the following range.
Innermost track resolution: 55%, Min.

(j) For a double sided FDD, execute items (d) through (i) for the side 0 and the side 1 heads respectively.

(k) If the value in item (i) or (j) is out of the specified range, following causes are assumed.

i) Inferior disk:
Disk and/or jacket is deformed or damaged. Replace the level disk with a new one.

ii) Inferior disk rotational speed:
Check and adjust according to item 4-4-5.

iii) Inferior head touch:
Check and adjust according to item 4-4-6.

iv) Inferior head: Replace the head carriage Ass'y according to item 4-5-1.

v) Inferior PCBA MFD control:
Replace the PCBA MFD control according to item 4-5-6.

(L) Eject the level disk and release the Invert and Add modes of the oscilloscope.

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Start the spindle motor by key "5". (MON indicator turns on).

(c) Install a level disk.

(d) Execute drive select by key "0". (DS0 indicator turns on).

(e) Key in "C0" and confirm that the TRACK indication becomes "00". (RECALIBRATE)

(f) Key in "C1". (SEEK TMAX)

(g) Key in "D8". (RESOLUTION)
The calibration value of the level disk should be set previously in the SKA.

(h) Confirm that the DATA indicator □□□ (%) indicates the value within the following range.
Innermost track resolution: 55%, Min.

(i) For a double sided FDD, depress key "4" and execute items (g) and (h) for the side 0 head and the side 1 head respectively. The side is changed alternately by a depression of "4" key. If the side 1 is selected, SIDE 1 indicator of the SKA turns on.

(j) If the value in item (h) or (k) is out of the specified range, refer to item (k) of "General method".

(k) Eject the level disk.

4-4-10. Check and Adjustment of Track Alignment

(A) Equipment

(1) Cross point screwdriver, M3
(2) Common screwdriver, medium
(3) Alignment disk
(4) \SKA or user's system
(5) Oscilloscope
(6) Hygrometer.
(7) Locking paint

(B) Check and adjustment procedure

Note: Check and adjustment of track alignment should be done in an environment of general room temperature and humidity. Even if the environmental condition is within the specified operational condition, extreemly high or low temperature, or extreemly high or low humidity should be avoided. Check and adjustment should be done after two hours, Min. of storing in the above mentioned condition.
It is recommended that the orientation of the FDD for the track alignment check is the same as when the FDD is actually installed in the user's system.

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP9 and TP10 (Differentiation amp.) on the PCBA MFD control. Also connect the external trigger of the oscilloscope to TP4 (Index) and apply positive trigger.
Oscilloscope range : AC mode, 0.5V, 20msec
Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and Add both channels.

(b) Start the spindle motor and install an alignment disk.

(c) Set the head to the alignment check track.
Alignment check track: track 16

(d) Confirm that two lobe patterns as in Fig.425 can be observed (it is not necessary that the levels of VA and VB are equal).
If only one lobe pattern can be observed or if two lobes become one pattern, the head is not on the alignment check track.
In such event, execute step-out or step-in operation for 2 tracks space to obtain the most similar waveform to that in Fig.425.

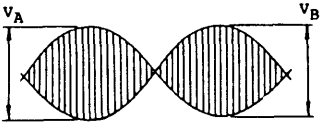
Note: The above number of tracks to be stepped is required to make the alignment track position be fit with the magnetized condition of the basic magnetized phase "A" of the stepping motor. If the stepped track numbers are inassured, set it again from track 00 (TRACK 00 output signal becomes TRUE).
For the FDD, the lobe pattern as in Fig.425 should be observed at the track of even number.

(e) After one or several step-outs from the check track, step in the head to the check track again and measure VA and VB at that time.

(f) Calculate the true value of misalignment by substituting the value in item (e) and ALIGNMENT calibration value (see alignment disk label, attention to the side).

$$\text{Misalignment (true value)} = \frac{VA-VB}{\text{Larger value in VA \& VB}} \times 100 - \text{Calibration value)} - (\text{Relative humidity} - 50) \times K$$

K is humidity compensation factor.
K = 0.26



(Fig.425) Alignment check lobe pattern

e.g. VA=0.58V, VB=0.61V, Calibration value= -6(%),
Relative humidity=65%

$$\text{Misalignment (true value)} = \left\{ \frac{0.58 - 0.61}{0.61} \times 100-(-6) \right\} - (65-50)$$
$$\times 0.26 \simeq -2.8\%$$

If the calculated value is positive, the magnetic head is shifted inward from the reference position, while the head is shifted outward from the reference position when the value is negative.

(g) Conversely, measure VA and VB when the head is on the alignment check track by stepping-out after one or several step-ins.

(h) Calculate the true value of misalignment as described in item (f).

(i) Confirm that both of the calculated values in items (f) and (h) are within the following range.
True value of misalignment: 30%, Max.

(j) For a double sided FDD, execute items (c) through (i) for the side 0 and the side 1 heads respectively.

(k) If the value in item (i) or (j) is out of the specified range, adjust the track alignment according to the following procedure:

i) Loosen two fixing screws of the stepping motor a little.

ii) Insert a common screwdriver from the back side of the FDD as shown in Fig.426 and depress it to the geared area of the stepping motor.

iii) Repeat step-in and step-out operations and adjust the misalignment to be the smallest on the alignment check track during both step-in and step-out operations by the screwdriver (stepping motor moves little by little).

Note: When you adjust the alignment by observing the lobe pattern using the oscilloscope, pay attention to the calibration value on the alignment disk label and the ambient relative humidity.

① Calibration value + (Relative humidity - 50) x K $\geq$ 0:
When the left side lobe pattern level, VA is assumed as "1", lobe pattern ratio should be so adjusted that the right side lobe pattern level VB takes the following value:

$$VB = 1 - \frac{\text{Calibration value} + (\text{Relative humidity} - 50) \times K}{100}$$

② Calibration value + (Relative humidity - 50) x K $\leq$ 0:
When the right side lobe pattern level, VB is assumed as "1", lobe pattern ratio should be so adjusted that the left side lobe pattern level VA takes the following value.

$$VA = 1 - \frac{\text{Calibration value} + (\text{Relative humidity} - 50) \times K}{100}$$

e.g. Calibration value = -6%, Relative humidity = 35% :

$$-6+(35-50)\times 0.26 = -9.9 < 0$$

$$VA = 1 - \frac{-6+(35-50)\times 0.26}{100} \fallingdotseq 0.90$$

iv) For a double sided FDD, repeat the adjusting operation in item iii) alternately for the side 0 and the side 1 heads unitl the both

misalignment take the smallest value.

v) Tighten the two fixing screws of the stepping motor little by little for adjusting the true value of misalignment after tightening the screws with the following specified torque to be within ±20%.
Stepping motor fixing torque: 9Kg.cm

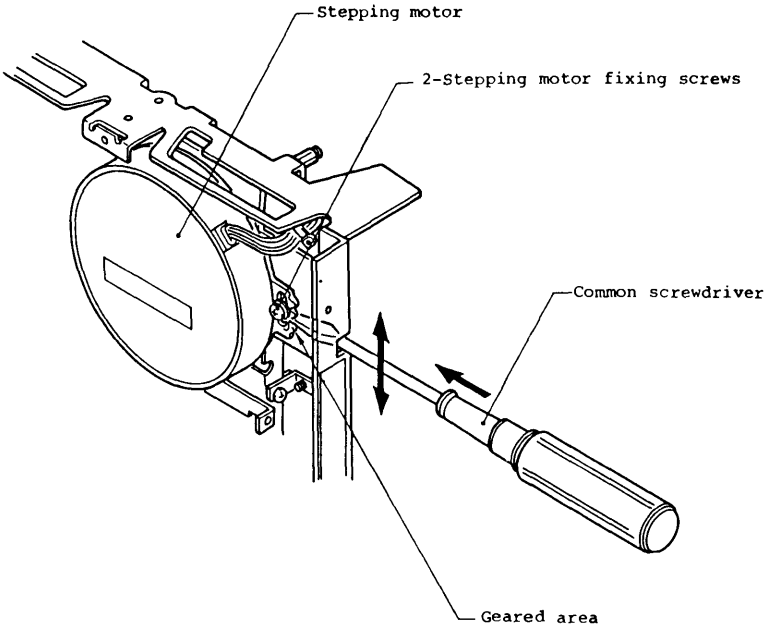
vi) Remove the alignment disk.

vii) Apply a drop of locking paint to the head of the stepping motor fixing screws.

viii) Check and adjust the track 00 sensor according to item 4-4-11.

ix) Check and adjust the track 00 stopper according to item 4-4-12.

(L) Release the Invert and Add modes of the oscilloscope.



(Fig.426) Adjustment of track alignment

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Use two channels of an oscilloscope. Connect the 1st channel to the DOUT terminal of the SKA and the 2nd channel to the DIF terminal of the SKA. Apply positive trigger by DOUT terminal.
Oscilloscope range
The 1st channel: DC mode, 2V, 20msec
The 2nd channel: AC mode, 1V, 20msec

(c) Key in "B9F" (INDEX observation)

(d) Start the spindle motor by key "5". (MON indicator turns on).

(e) Install an alignment disk.

(f) Execute drive select by key "0". (DS0 indicator turns on).

(g) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(h) Set the head to the alignment check track.
Key in "C2 16" and confirm that the TRACK indication becomes "16".

(i) Confirm that two lobe patterns as in Fig.425 can be observed by the oscilloscope (it is not necessary that the levels of VA and VB are equal).
If only one lobe pattern can be observed or if two lobes become one pattern, the head is not on the alignment check track.
In such event, execute step-in or step-out operation for 2 track space to obtain the most similar waveform to that in Fig.425. Step operation can be done by key "8" (STEP-IN) and key "9" (STEP-OUT).

By a depression of these keys, head will move for one track space.

Note: The above number of tracks to be stepped is required to make the alignment track position be fit with the magnetized condition of the basic magnetized phase "A" of the stepping motor.
For the FDD, the lobe pattern as in Fig.425 should be observed at the track of even number.

(j) Confirm that the H GAIN indicator of the SKA is off. If it is on, turn it off by depressing "DD" key.

(k) Key in "E3" (ALIGNMENT)
Calibration value of the alignment disk and environmental relative humidity should be set previously in the SKA.

(L) Confirm all the indications on the DATA □□□□ (%) indicator are within ±30%.
The initial digit of the DATA indicator is the symbol. ⊬ (+) mark indicates that the head is shifted inward from the reference position, while - mark indicates that the head is shifted outward.

(m) For a double sided FDD, execute the same check for the side 1 head according to the following procedure.

i) Key in "0" following the operation of item (L) (during execution of E3 command) and confirm that SIDE 1 indicator of the SKA turns on.

ii) Confirm as in item (L).

Note: In order to change the head to side 0, key in "0" again. (SIDE 1 indicator turns off).

(n) Depress "F" key (STOP).

(o) If the value in items (L) or (m) is out of the specified range, adjust

the track alignment according to the following procedure.

i) Loosen the two fixing screws of the stepping motor a little.
ii) Insert a common screwdriver from the back side of the FDD as shown in Fig.426 and depress it to the geared area of the steppint motor.
iii) Key in "E3" and adjust the misalignment so that the DATA indicator □□□□ (%) shows the smallest value. The stepping motor moves little by little by the screwdriver.
iv) For a double sided FDD, repeat the adjusting operation in item iii) alternately for side 0 and side 1 heads until the both misalignment take the smallest value.
v) Tighten the two fixing screws of the stepping motor little by little to obtain the value within ±20% on the DATA indicator when the screws are tightened with the following specified torque.
Stepping motor fixing torque: 9Kg.cm.
vi) Remove the alignment disk.
vii) Apply a drop of locking paint to the screw head of the stepping motor fixing screws.
viii) Check and adjust the track 00 sensor according to item 4-4-11.
ix) Check and adjust the track 00 stopper according to item 4-4-12.

(p) Release the Invert and Add modes of the oscilloscope.

4-4-11. Check and Adjustment of Track 00 Sensor

(A) Equipment

(1) Common screwdriver, M3
(2) Work disk
(3) Alignment disk
(4) SKA or user's system
(5) Oscilloscope (or digital voltmeter)
(6) Locking paint

(B) Check and adjustment procedure

(1) General method

(a) Use two channels of an oscilloscope and connect them as follows:

i) The 1st channel: STEP interface signal (pin No.20) or PCBA MFD control U4, pin 5.
ii) The 2nd channel: PCBA MFD control TP1 (Track 00 sensor). 1V range
iii) External trigger: DIRECTION SELECT interface signal (pin No.18) or PCBA MFD control U4, pin 11. (+) trigger

(b) Start the spindle motor and install a work disk.

(c) Make the head move to track 00.

(d) Confirm that the timings tA and tB of the Track 00 sensor signal (TP1) is within the following range when the DIRECTION SELECT (trigger signal) and the STEP signal (6ms interval) as shown in Fig.427 is supplied.

TP1 tA: 3.1 ∿ 5.4msec

TP1 tB: 0 ∿ 5.8msec

(e) If the value in item (d) is out of the specified range, adjust the position of the track 00 sensor according to the following procedure.

i) Loosen the fixing screw of the track 00 stopper (see Fig.429 and shift the stopper in the step-out direction (make apart from the rear side of the head carriage).

ii) Connect an oscilloscope to TP9 or TP10 (Differentiation amp.) of the PCBA MFD control.
Oscilloscope range: AC mode, 0.2V, 20msec

iii) Install an alignment disk. The track alignment should be adjusted correctly according to item 4-4-10.

iv) Make the head move to the position where the lobe pattern as in Fig.425 can be observed.

v) Remove the alignment disk.

vi) Step out the head for 16 tracks' space. (The head moves to track 00).

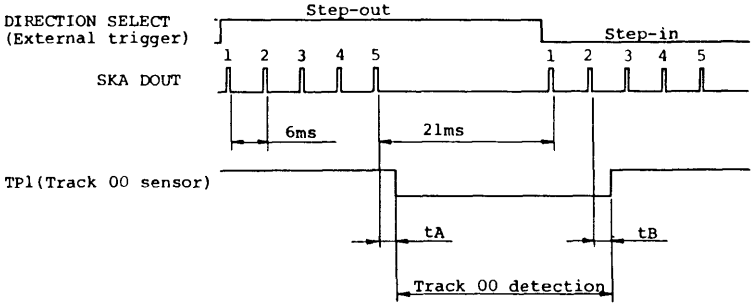
vii) Change the connection of the oscilloscope as item (a).

viii) Loosen the fixing screws of the track 00 sensor (see Fig.428) and move the sensor a little so that the timing tA in Fig.427 falls within the following range.
Adjusting target of TP1 tA: 3.4 ∿ 4.6msec

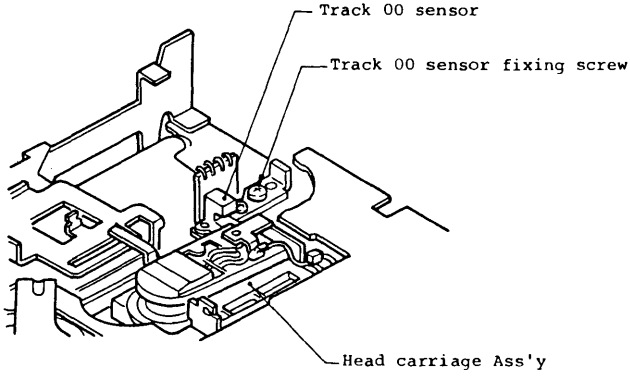
ix) Repeat the adjustment of the track 00 sensor position so that the value in item viii) satisfy the specification when the screw has been tightened with the specified torque.

x) Apply a drop of locking paint on the fixing screw head.

xi) Adjust the track 00 stopper according to item 4-4-12.



(Fig.427) Track 00 sensor waveform



(Fig.428) Adjustment of track 00 sensor

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Use two channels of oscilloscope and connect them as follows:

i) The 1st channel: SKA DOUT terminal
DC mode, 5V, 10msec

ii) The 2nd channel: PCBA MFD control TP1 (Track 00 sensor), 1V range

iii) External trigger: DIRECTION SELECT interface signal (Interface connector pin No.18) or Pin 3 of J3 (resistor network RA1 for terminator) on the PCBA MFD control.
(+) trigger.

(c) Key in "B8 F". (STEP observation)

(d) Start the spindle motor by key "5". (MON indicator turns on).

(e) Install a work disk.

(f) Execute drive select by key "0". (DS0 indicator turns on).

(g) Set the step rate and the settling time as follows referring to item 4-2-4-3.
Step rate : 6msec
Settling time : 15msec

(h) Key in "C0" and condirm that the TRACK indicator becomes "00".

(i) Key in "C5". (T00 TIMING, SEEK ±5)

(j) Measure the tA and tB timings according to Fig.427 and confirm the

timings are within the following range:
tA: 3.1 ∿ 5.4msec
tB: 0 ∿ 5.8msec

(k) Key in "F". (STOP)

(L) Turn the FD PWR switch of the SKA off at the track 00 position and then set it again to the PSA side. Confirm that the stop position of the head carriage did not change at power off and on.

(m) If the value in item (j) or (L) is out of the specified range, adjust the position of the track 00 sensor according to the following procedure.

i) Loosen the fixing screw of the track 00 stopper (see Fig.429) and shift the stopper in the step-out direction (make apart from the rear side of the head carriage).
ii) Connect the 2nd channel of the oscilloscope to TP9 or TP10 (Differentiation amp.) of the PCBA MFD control and change the trigger to this channel.
Oscilloscope range: AC mode, 0.2V, 20msec
iii) Install an alignment disk. The track alignment should be correctly adjusted according to item 4-4-10.
iv) Key in "C0" and confirm that the track indicator becomes "00". (RECALIBRATE).
v) Key in "C2 16" and confirm that two lobe patterns as in Fig.425 can be observed.
If normal lobe pattern cannot be observed, move the head to the track position where the typical lobe pattern can be observed by stepping in by key "8" or by stepping out by key "9".
vi) Remove the alignment disk.
vii) Key in "E4 16". (SET TRACK NUMBER)
viii) Key in "C2 00". (SEEK 00)
Don't key in "C0". (RECALIBRATE)

ix) Change the connection of the oscilloscope as in item (b).

x) Key in "C5". (T00 TIMING SEEK ±5)

xi) Loosen the fixing screw of the track 00 sensor (see Fig.428) and adjust the sensor position so that the timing tA in Fig.427 falls within the following range.

Adjusting target of tA: 3.4 ∿ 4.6msec

xii) Repeat the adjustment so that the values in item xi) fall within the specified range when the fixing screw has been tightened with the specified torque.

xiii) Apply a drop of locking paint to the fixing screw head.

xiv) Adjust the track 00 stopper according to item 4-4-12.

4-4-12. Check and Adjustment of Track 00 Stopper

(A) Equipment

(1) Cross point screwdriver, M3
(2) SKA or user's system
(3) Locking paint

(B) Check and adjustment procedure

(1) General method

(a) Set the head to track 00.

(b) Step out the head from the track 00 position.

(c) Confirm that the head carriage does not move by the step-out command (head carriage rests on track 00).

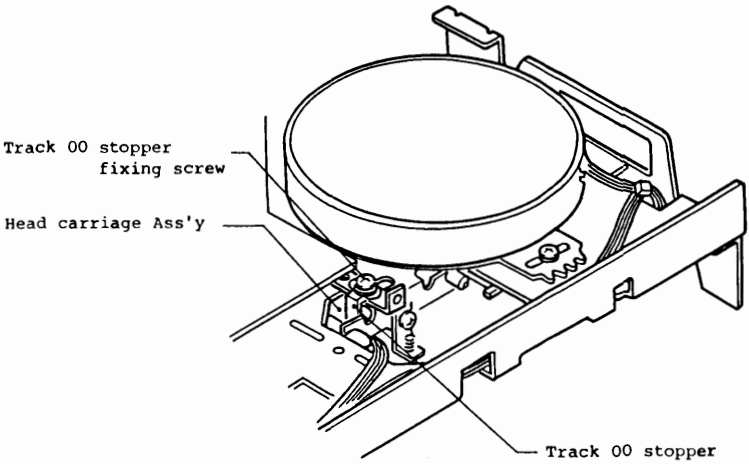
(d) Confirm that the gap between the head carriage and the extreme end of the track 00 stopper is 0.1 ∿ 0.4mm. (See Fig.429).

(e) Repeat step-in and step-out operations between track 00 and track 05. Confirm that no impact sound can be heard between the head carriage and the track 00 stopper.

(f) Turn off the FDD power and depress the head carriage lightly against the track 00 stopper with fingers.

(g) Confirm that the head carriage automatically returns to the initial position (track 00) when the power is turned on again.

(h) If any one of the items (d), (e), and (g) is not satisfied, adjust the track 00 stopper position according to the following procedure.



(Fig.429) Adjustment of track 00 stopper

i) Set the head to track 00.

ii) Loosen the fixing screw of the track 00 stopper. (See Fig.429).

iii) Adjust the stopper position so that the gap between the stopper and the head carriage becomes 0.25mm, approx. And then tighten the screw with the specified torque.

iv) Execute items (a) through (g).

v) Apply a drop of locking paint on the fixing screw head.

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Execute drive select by key "0". (DS0 indicator turns on).

(c) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE).

(d) Set the step rate and the settling time as follows referring to item 4-2-4-3.
Step rate : 6msec
Settling time : 15msec

(e) Key in "9". (STEP OUT)

(f) Confirm that the head carriage does not move even if "9" is keyed in (head carriage rests on track 00).

(g) Confirm that the gap between the head carriage and the extreme end of the track 00 stopper is 0.1 ∿ 0.4mm. (See Fig.429).

(h) Key in "C0" and key in "C5". (STEP TIMING, SEEK ±5)

(i) Confirm that no impact sound can be heard between the head carriage and the track 00 stopper.

(j) Turn off the FD PWR switch of the SKA and depress the head carriage lightly against the track 00 stopper.

(k) Confirm that the head carriage automatically returns to the initial position (track 00) when the FD PWR switch is set to the PSA side again.

(L) If any one of the items (g), (i), and (k) is not satisfied, adjust the track 00 stopper position according to the following procedure.

i) Key in "C0" and confirm that the TRACK indicator becomes "00" (RECALIBRATE)

ii) Loosen the fixing screw of the track 00 stopper. (See Fig.429).

iii) Adjust the stopper position so that the gap between the stopper and the head carriage becomes 0.25mm, approx.
And then tighten the screw with the specified torque.

iv) Execute items (a) ∿ (k).

v) Apply a drop of locking paint on the fixing screw head.

4-4-13. Check and Adjustment of Index Burst Timing

(A) Equipment

(1) Cross point screwdriver, M3
(2) Alignment disk
(3) SKA or user's system
(4) Oscilloscope (not required when the SKA is used)
(5) Locking paint

(B) Check and adjustment procedure

(1) General method

(a) Use two channels of the oscilloscope. Connect the 1st channel to TP4 (Index) on the PCBA MFD control and the 2nd channel to TP7 or TP8 (Pre-amp.). Apply positive trigger by TP4.
Oscilloscope range
The 1st channel: DC mode, 2V, 50μsec
The 2nd channel: AC mode, 1V, 50μsec

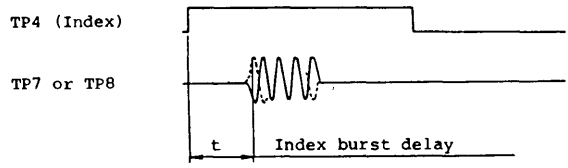
(b) Start the spindle motor and install an alignment disk.

(c) Set the head to track 01.

(d) Measure "t" in Fig.430.

(e) Substitute the following equation with the measured value in item (d) and INDEX TIMING calibration value (see alignment disk label).

Index burst timing (true value) = Measured value - Calibration value(μs)



(Fig.430) Index burst timing

(f) Confirm that the true value of the index burst timing is within the following range.
Index burst timing : 200±200µsec

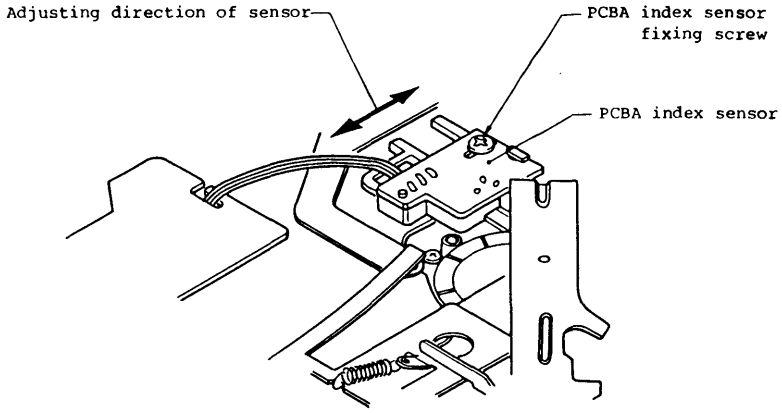
(g) If the value in item (f) is out of the specified range, adjust the index sensor Ass'y position according to the following procedure.

i) Loosen the fixing screws (see Fig.431) of the PCBA index sensor and adjust its position to make the true value of the index burst timing gall in the specified range in item (f).

ii) Repeat the adjustment so that the true value of the index burst timing falls in the range of item (f) when the fixing screw has been tightened with the specified torque.

iii) Apply a drop of locking paint on the fixing screw head.

(h) Remove the alignment disk.



(Fig.431) Adjustment of index sensor

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Start the spindle motor by key "5". (MON indicator turns on).

(c) Install an alignment disk.

(d) Execute drive select by key "0". (DS0 indicator turns on).

(e) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(f) Set the head to the index check track.
Key in "C2 01" and confirm that the TRACK indication becomes "01".

(g) Key in "E6". (INDEX TIMING)
The calibration value of the index timing should be set previously in the SKA.

(h) Confirm that the DATA indicator □□□□ (μs) indicates the value within the following range.
Index burst timing: 200±200μsec

(i) Key in "F". (STOP)

(j) If the value in item (h) is out of the specified range, adjust the index sensor Ass'y position according to the following procedure.

i) Loosen the fixing screws (see Fig.431) of the PCBA index sensor and its position so that the DATA indication under execution shows the median value in the specified range of item (h).

ii) Repeat the adjustment so that the DATA indication takes the median value when the fixing screw has been tightened with the specified torque.

iii) Depress "F" key. (STOP).

iv) Apply a drop of locking paint on the fixing screw head.

(k) Remove the alignment disk.

4-5. MAINTENANCE PARTS REPLACEMENT

4-5-1. Replacement of Head Carriage Ass'y

(A) Tools

(1) Cross point screwdriver, M3
(2) Cross point screwdriver, M2.6
(3) Hexagon wrench key, 1.5mm
(4) Box screwdriver for hexagon nut, M3
(5) A pair of tweezers
(6) Lubricant, Kantoh Kasei 946P
(7) Alcohol and gauze (several sheets)
(8) Locking paint
(9) SKA or user's system

(B) Replacement procedure

(1) Turn the front lever (Fig.505, No.42) to close position and remove the fixing screw (Fig.505, S11).

(2) Turn the front lever to open position and draw out the front lever Ass'y.

(3) Remove the fixing screws (Fig.505, S5) of the front bezel Ass'y (Fig. 505, No.41) to remove the Ass'y.

(4) Remove the fixing screw (Fig.505, S1) of the cord clamper to remove the clamper (Fig.505, No.39).

(5) Remove two fixing screws (Fig.505, S1) of the shield cover (Fig.505, No.44) to remove the cover.

(6) Remove three fixing screws (Fig.505, No.37 and S1) of the PCBA MFD

control(Fig.505, No.35) and lift it up.

(7) Disconnect all of the connectors mounted on the PCBA MFD control and remove the PCBA.

(8) Pull out the head cable from the disk guide U-groove and cable clamper and draw it out to the head carriage Ass'y (Fig.505, No.13) side.

(9) Holding the top of the band fixing plate B (Fig.505, No.17) and the head carriage Ass'y with your fingers to release the hook of the steel belt (Fig.505, No.19) and the band fixing plate B.

(10) Pull out the band fixing plate B and the band spring(Fig.505, No.18) at the same time from the head carriage Ass'y.

(11) Separate the steel belt from the hook of the band fixing plate A (Fig.505, No.16) to remove the band fixing plate A from the head carriage Ass'y.
When removing the band fixing plate A from the head carriage, it will be removed easily if it is shifted toward the front bezel side and then drawn out in a right angle.

(12) Remove the belt fixing screw (Fig.505, S8) on the capstan of the stepping motor Ass'y (Fig.505, No.12) and then remove the band washer (Fig.505, No.20) and the steel belt.

(13) Remove one of the two guide shaft clips (Fig.505, No.15) which fix the guide shafts. The clip for the rear side one should be removed.

(14) Draw out two guide shafts (Fig.505, No.14) toward the rear of the FDD and remove them from the fixing area of the front side chassis (Fig.505, No.1).
Then remove the head carriage Ass'y with two guide shafts and the front

side clip. Refer to Fig.432.

(15) Draw out two shafts from the head carriage and remove the front guide shaft clip.

(16) Prepare a new head carriage Ass'y and two guide shafts for installation.

Note: When replacing the head carriage Ass'y, replace the guide shafts at the same time because of matching the hole diameter of the carriage with that of the guide shaft. Guide shafts are to be designated in combination with the head carriage Ass'y. (Refer to item 4-1-3, (2)).
Guide shaft which goes through the hole of the head carriage smoothly with a little clearance is considered to be the best.

(17) Apply specified lubricant to the surface of one guide shaft. Then install it again to the new head carriage as it was.

Note: When applying the lubricant to the guide shaft, dip a piece of gauze to the lubricant and wipe the shaft and then wipe it again lightly with a dry and clean gauze.
The most appropriate quantity of the lublicant for the surface of the shafts forms a thin oil coating.

(18) Apply the lubricant to the another guide shaft and install it to the new head carriage as it was.

(19) Attach the guide shaft clip to the front bezel side groove of the shafts.

(20) Attach the new head carriage Ass'y in item (19) in the reverse order of items (13) and (14).

Note: Pre-load is applied between the two guide shafts to make them approach each other by the guide shaft clip in order to reduce the

variety of the installation position of the head carriage Ass'y. For installing the two guide shafts to the chassis, mount them with pressure to separate them.

(21) Install the steel belt (C) to the capstan of the stepping motor Ass'y in the reverse order of item (12).

Note: If the surface of steel belt or capstan is smeared, clean it carefully with alcohol and gauze.

(22) Connect the steel belt to the head carriage Ass'y using the band fixing plates A and B and band spring in the reverse order of items (9) through (11).

(23) Tighten the fixing screw of the steel belt slightly to the stepping motor Ass'y.

(24) After moving the head carriage several times manually, tighten the steel belt fixing screw carefully with the specified torque. At this time, be careful that the belt is tensioned straightly. Pay attention not to damage the surface of the belt or the capstan.

(25) Form the head cable in the reverse order of items (4) and (6) through (8) and attach the PCBA MFD control. Refer to item 4-2-3 as to the details of the head cable treatment.

(26) Loosen the fixing screw (Fig.505, S4) of the track 00 stopper (Fig.505, No.6) and shift the stopper toward the rear side of the FDD.

(27) Attach the front lever temporarily for the following check and adjustment.

(28) Make the head seek continuously between the track 00 and the innermost track and confirm that the steel belt does not meander nor undulate.

When the SKA is used, key in "C6" for this check and key in "F" for stop.
If the steel belt does meander or undulate, readjust the belt to run straightly by the screw in item (12). After the adjustment, tighten the screw carefully with the specified torque.

(29) Check for the head touch according to item 4-4-6.

(30) Check and adjust the asymmetry according to item 4-4-7. (Adjustment is applied only for the FDD with the variable resistor, R5 on the PCBA MFD control).

(31) Adjust the track alignment according to item 4-4-10.

(32) Adjust the track 00 sensor position according to item 4-4-11.

(33) Adjust the track 00 stopper position according to item 4-4-12.

(34) Check and adjust the index burst timing according to item 4-4-13.

(35) Check for the read level according to item 4-4-8.

(36) Check for the resolution according to item 4-4-9.

(37) Attach the shield cover in the reverse order of item (5).

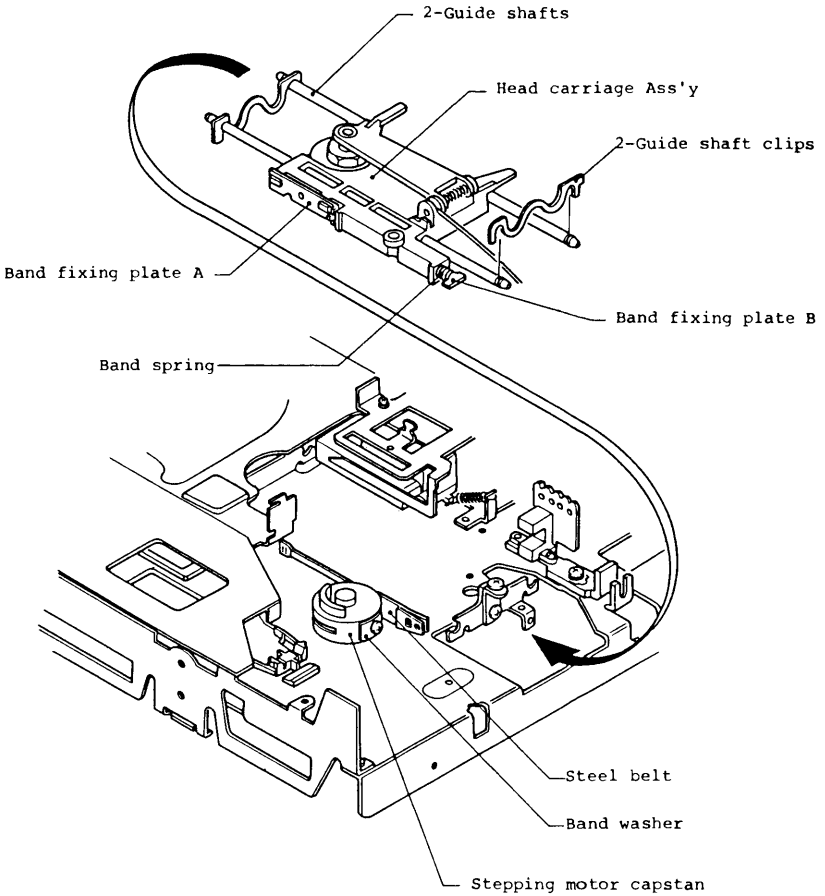
(38) Remove the fixing screw of the front lever to remove the lever.

(39) Attach the front bezel Ass'y and the front lever Ass'y in the reverse order of items (1) through (3).

(40) Adjust the front lever position according to item 4-4-2.

(41) It is recommended to connect the FDD to the system for overall test.

Refer to item 4-2-5 (1)).



(Fig.432) Replacement of head carriage Ass'y

4-5-2. Replacement of Stepping Motor Ass'y and Steel Belt

(A) Tools

(1) Cross point screwdriver, M3
(2) Cross point screwdriver, M2.6
(3) Hexagon wrench key, 1.5mm
(4) Box screwdriver for hexagon nut
(5) A pair of tweezers
(6) Alcohol and gauze
(7) Locking paint
(8) SKA or user's system

(B) Replacement procedure

(1) Remove the shield cover (Fig.505, No.44) by removing the two fixing screws (Fig.505, S1).

(2) Lift the PCBA MFD control (Fig.505, No.35) by removing the three fixing screws (Fig.505, No.37 and S1).

(3) Disconnect all the connectors mounted on the PCBA MFD control and remove the PCBA.

(4) Holding the top of the band fixing plate B (Fig.505, No.17) and the head carriage Ass'y with your fingers to release the hook of the steel belt (Fig.505, No.19) and the band fixing plate B.

(5) Pull out the band fixing plate B and the band spring (Fig.505, No.18) at the same time from the head carriage Ass'y.

(6) Separate the steel belt from the hook of the band fixing plate A (Fig.505, No.16) to remove the band fixing plate A from the head carriage Ass'y.

When removing the band fixing plate A from the head carriage, it will be removed easily if it is shifted toward the front bezel side and then drawn out in a right angle

(7) Remove the belt fixing screw (Fig.505, S8) on the capstan of the stepping motor Ass'y (Fig.505, No.12) and then remove the band washer (Fig.505, No.20) and the steel belt.

(8) Remove the stepping motor Ass'y by removing the fixing screws (Fig.505, S4).

(9) Install a new stepping motor Ass'y as it was.

(10) Fix a new α-shape steel belt temporarily to the capstan of the new stepping motor with the band washer and the screw in item (7).

Note: Fundamentally, the steel belt and the band spring should be replaced with the stepping motor. However, if there is no inferior points for these belt and spring, they may be used after cleaning the surface carefully with alcohol and gauze.

(11) Connect the steel belt and the head carriage using the band fixing plates A and B and band spring in the reverse order of items (4) through (6).

(12) After moving the head carriage several times manually, tighten the steel belt fixing screw in item (10) carefully with the specified torque. At this time, be careful so that the belt is tensioned straightly. Pay attention not to damage the surface of the belt or the capstan.

(13) Install the PCBA MFD control in the reverse order of items (2) and (3).

(14) Loosen the fixing screw (Fig.505, S4) of the track 00 stopper (Fig.505, No.6) and shift the stopper toward the rear side of the FDD.

(15) Make the head seek continuously between the track 00 and the innermost track and confirm that the steel belt does not meander nor undulate. When the SKA is used, key in "C6" for this check and key in "F" for stop the operation.
If the steel belt meanders or undulates, readjust the belt to run straightly by the screw in item (10). After the adjustment, tighten the screw carefully with the specified torque.

(16) Execute the continuous seek operation for five minutes.
When the SKA is used, key in "C6" and key in "F" for stopping the operation.

(17) Attach the shield cover with two fixing screws.

(18) Adjust the track alignment according to item 4-4-10.

(19) Adjust the track 00 sensor position according to item 4-4-11.

(20) Adjust the track 00 stopper position according to item 4-4-12.

4-5-3. Replacement of DD Motor Ass'y (Spindle motor)

(A) Tools

(1) Cross point screwdriver, M3
(2) A pair of tweezers
(3) Cutting pliers
(4) SKA or user's system

(B) Replacement procedure

(1) Remove the shield cover (Fig.505, No.44) by removing the two fixing screws (Fig.505, S1).

(2) Disconnect the spindle motor connector (J7).

(3) Cut and remove the cable tie (Fig.505, No.40) for binding the wiring. Throw away the removed cable tie.

(4) Draw out the PCB holder (Fig.505, No.38) which holds the PCBA servo of the DD motor Ass'y (C) (Fig.505, No.7) from the chassis (Fig.505, No.1).

(5) Remove three fixing screws (Fig.505, S2, S7) of the DD motor from the upper side of the FDD and remove the DD motor Ass'y from the lower side of the FDD.

(6) Install a new DD motor Ass'y in the reverse order of items (2) through (5).

Notes: 1. The spindle area of the DD motor Ass'y (clamping cup of the disk) is precisely machined. For installing the motor to the frame, place the spindle in parallel to the frame and push into the frame slowly. Handle the spindle very carefully not to damage

the spindle surface.

2. Collar B (Fig.505, No.5) is attached to the screw of the disk insertion side. Confirm that the collar B is not taken out in the process of tightening the screw.

(7) Adjust the collet shaft plate (Fig.505, No.29) position according to item 4-4-1.

(8) Bind a new bundle of cables to the chassis made of DD motor cable, T00 sensor Ass'y cable, and front OPT Ass'y cable using a new cable tie.

(9) Check for the file protect sensor according to item 4-4-4.

(10) Check or adjust the disk rotation speed according to item 4-4-5. (Adjustment is applied only for the motor with the variable resistor, R1 on the PCBA DD motor servo).

(11) Check and adjust the track alignment according to item 4-4-10.

(12) Check and adjust the index burst timing according to item 4-4-13.

(13) Attach the shield cover in the reverse order of item (1).

4-5-4. Replacement of Collet Ass'y

(A) Equipment

(1) Cross point screwdriver, M3
(2) A pair of tweezers
(3) Locking paint
(4) SKA or user's system

(B) Replacement procedure

(1) Remove the shield cover (Fig.505, No.44) by removing the two fixing screws (Fig.505, S1).

(2) Remove the collet shaft plate Ass'y (Fig.505, No.29 by removing two fixing screws (Fig.505, S3).

Note: For the drive with eject Ass'y (Option), remove the hooks of the eject spring A and eject spring B from the collet shaft plate. Then remove the collet shaft plate Ass'y.

(3) Pull out the collet Ass'y (Fig.505, No.30) from the U-groove of the clamp spring (Fig.505, No.27) to remove it.

(4) Install a new collet Ass'y in the reverse order. For installation at this step screw the collet shaft plate Ass'y temporarily.

(5) Adjust the collet shaft plate position according to item 4-4-1.

(6) Check and adjust the track alignment according to item 4-4-10.

(7) Attach the shield cover in the reverse order of item (1).

4-5-5. Replacement of PCBA T00 Sensor

(A) Tools

(1) Cross point screwdriver, M3
(2) Cross point screwdriver, M2
(3) A pair of tweezers
(4) Cutting pliers
(5) Locking paint
(6) SKA or user's system

(B) Replacement procedure

(1) Disconnect the track 00 connector (J4).

(2) Cut and remove the cable tie (Fig.505, No.40) for binding the wiring. Throw away the removed tie.

(3) Remove the PCBA T00 sensor (Fig.505, No.9) by removing the fixing screw (Fig.505, S10).

(4) Install a new PCBA T00 sensor in the reverse order of item (1) through (3).

(5) Loosen the fixing screw (Fig.505, S6) of the T00 bracket (Fig.505, No.8) and shift it toward the rear side of the FDD.

(6) Loosen the fixing screw (Fig.505, S4) of the track 00 stopper (Fig.505, No.6) and shift it toward the rear side of the FDD.

(7) Adjust the track 00 position sensor according to item 4-4-11.

(8) Adjust the track 00 stopper position according to item 4-4-12.

4-5-6. Replacement of PCBA MFD Control (C)

(A) Tools

(1) Cross point screwdriver, M3
(2) Box screwdriver for hexagon nut, M3
(3) SKA or user's system

(B) Replacement procedure

(1) Remove the shield cover (Fig.505, No.44) by removing two fixing screws (Fig.505, S1).

(2) Remove three fixing screws of the PCBA MFD control (Fig.505, No.35) and lift up the PCBA.

(3) Disconnect all of the connectors mounted to the PCBA MFD control and remove the PCBA.

(4) Install a new PCBA MFD control in the reverse order of items (2) and (3).

(5) Set the straps as they were on the old PCBA.

(6) Check and adjust the asymmetry according to item 4-4-7. (Adjustment is applied only for the PCBA MFD control with the variable resistor, R5.

(7) Check for the read level according to item 4-4-8.

(8) Check for the resolution according to item 4-4-9.

(9) Check for the track 00 sensor according to item 4-4-11.

(10) Attach the shield cover in the reverse order of item (1).

(11) It is recommended to connect the FDD to the system for overall test.
(Refer to item 4-2-5, (1)).

4-5-7. Replacement of Front OPT Ass'y

(A) Tools

(1) Cross point screwdriver, M3
(2) Hexagon wrench key, 1.5mm
(3) Box screwdriver for hexagon nut, M3
(4) Cutting pliers
(5) Locking paint
(6) SKA or user's system

(B) Replacement procedure

(1) Turn the front lever (Fig.505, No.42) to close position and remove the fixing screw (Fig.505, S11).

(2) Turn the front lever to open position and draw out the front lever Ass'y.

(3) Remove the front bezel Ass'y (Fig.505, No.41) by removing two fixing screws (Fig.505, S5).

(4) Remove the shield cover (Fig.505, No.44) by removing two fixing screws (Fig.505, S5).

(5) Cut and remove the cable tie (Fig.505, No.40) for binding the wiring. Throw away the removed tie.

(6) Disconnect the front OPT connector (J5).

(7) Draw out the cable from the space between the chassis (Fig.505, No.1) and the PCBA DD motor servo and then draw it out from the U-groove of the disk guide (Fig.505, No.3).

(8) Remove two separate fixing screws (Fig.505, S1 and S5) of the front OPT

Ass'y (Fig.505, No.34) to remove the Ass'y.

(9) Install a new front OPT Ass'y in the reverse order of item (6) through (8).

(10) Check for the file protect sensor according to item 4-4-4.

(11) Adjust the index burst timing according to item 4-4-13.

(12) Form the cables as they were using a new cable tie.

(13) Attach the shield cover in the reverse order of item (4).

(14) Attach the front bezel Ass'y and the front lever Ass'y in the reverse order of items (1) through (3).

(15) Adjust the front lever position according to item 4-4-2.

4-5-8. Replacement of Head Pad (Single sided only)

This item applies only to the single sided FDD.

(A) Tools

(1) A pair of tweezers
(2) Alcohol and gauze

(B) Replacement procedure

(1) Remove the shield cover (Fig.505, No.44) by removing two fixing screws (Fig.505, S5).

(2) Lift up the pad arm manually and peel the pad carefully with a pair of tweezers. (See Fig.433).

(3) Apply a new pad to the initial position. Be careful not to press the pad surface strongly.

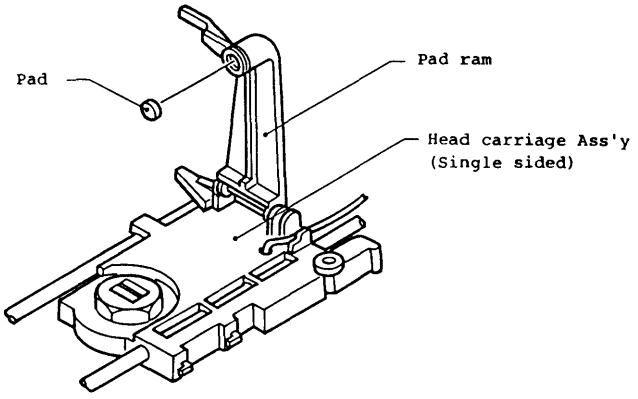
(4) Clean the magnetic head surface according to item 4-3-2.

(5) Adjust the head pad position according to item 4-4-6.

(6) Check for the read level according to item 4-4-8.

(7) Check for the resolution according to item 4-4-9.

(8) Attach the shield cover in the reverse order of item (1).



(Fig.433) Replacement of head pad

4-5-9. Replacement of Front Bezel Ass'y

(A) Tools

(1) Cross point screwdriver, M3
(2) Hexagon wrench key, 1.5mm

(B) Replacement procedure

(1) Turn the front lever (Fig.505, No.42) to close position and remove a fixing screw (Fig.505, S11).

(2) Turn the front lever to open position and draw out the front lever Ass'y.

(3) Remove the fixing screws (Fig.505, S5) of the front bezel Ass'y (Fig. 505, No.41) and draw out the front bezel.

(4) Install a new front bezel Ass'y in the reverse order of item (2) and (3).

Note: For the installation of the front bezel, be sure to hold the four installation and support arms of the upper and the lower chassis (Fig.505, No.1 and No.21) and press the longitudinal sides of the bezel against the chassis and tighten the fixing screws with the specified torque.

(5) Adjust the front lever position according to item 4-4-2.

4-5-10. Replacement of Front Lever Ass'y

(A) Tools

(1) Hexagon wrench key, 1.5mm

(B) Replacement procedure

(1) Turn the front lever (Fig.505, No.42) to close position and remove a fixing screw (Fig.505, S11).

(2) Turn the front lever to open position and draw out the front lever Ass'y.

(3) Install a new front lever Ass'y in the reverse order.

Note: For installation of the front lever Ass'y, match the slot of the lever to the pin of the lever shaft.

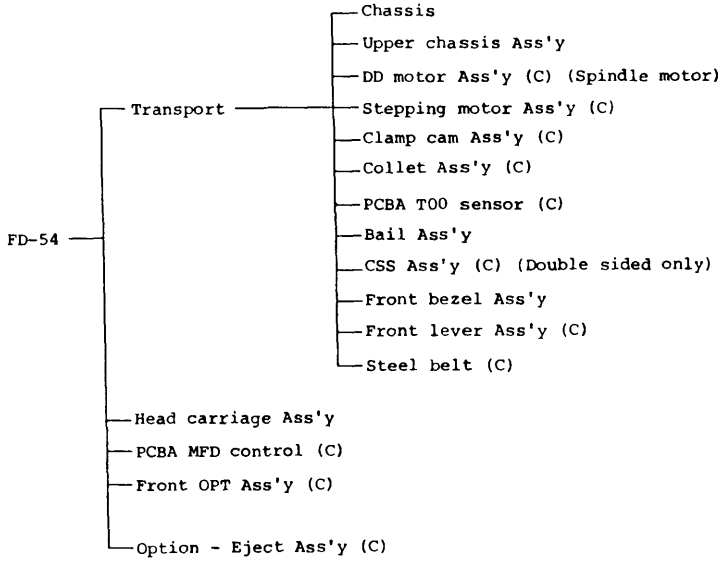
(4) Adjust the front lever position according to item 4-4-2.

SECTION 5

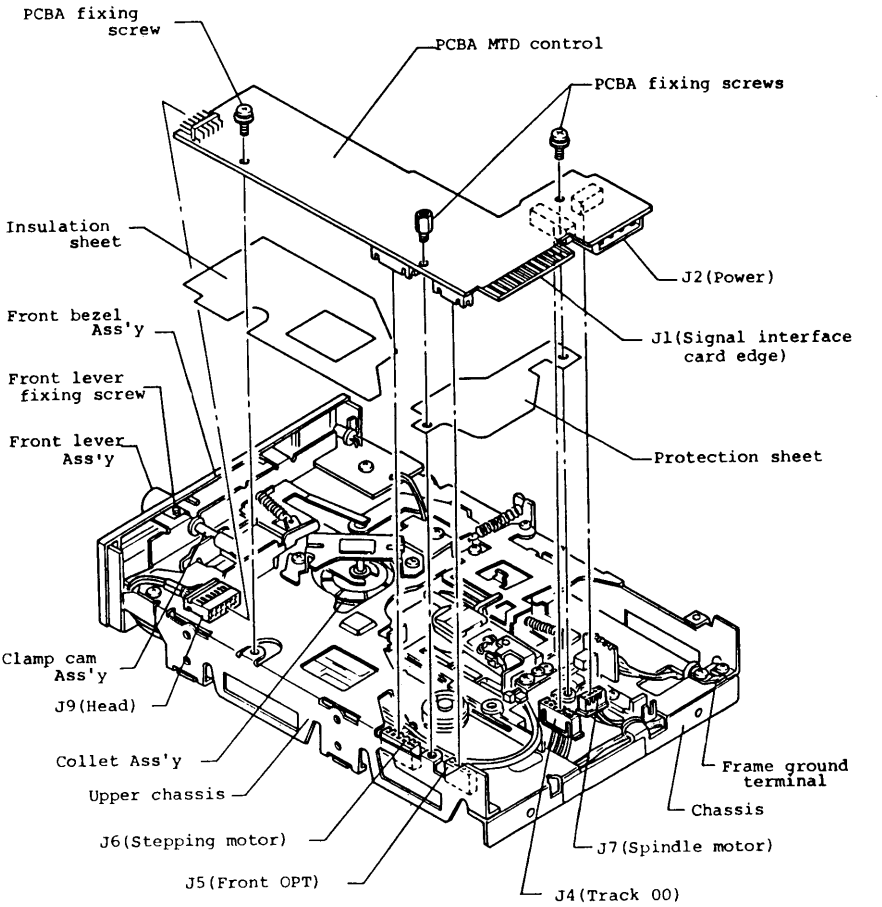
DRAWINGS & PARTS LIST

5-1. CONFIGURATION

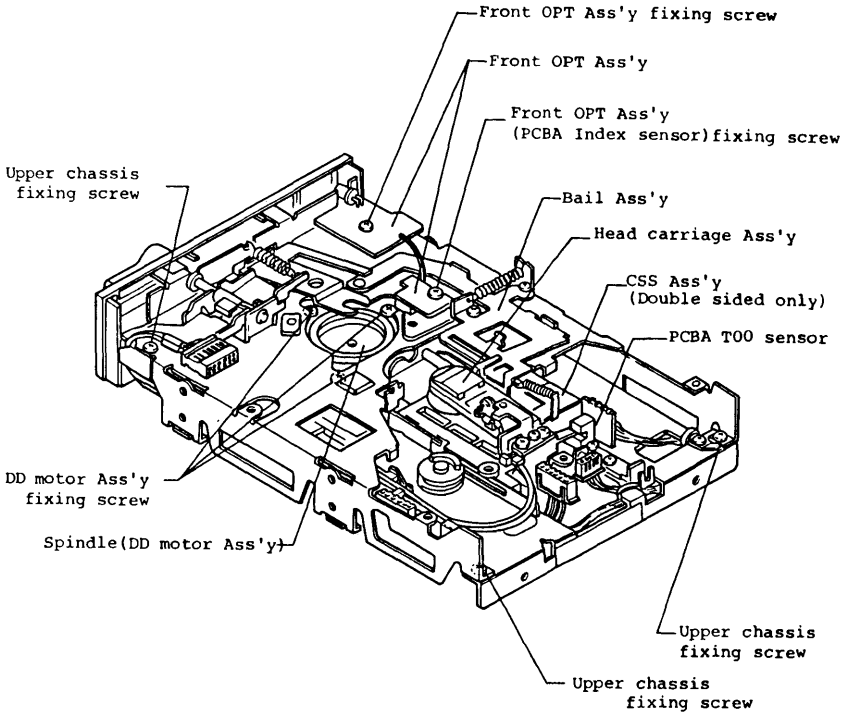
Following shows the configuration of the main parts of FD-54. (Refer to Fig.501 Fig.504). Refer to items 5-2 and 5-3 as to detailed break -downs.



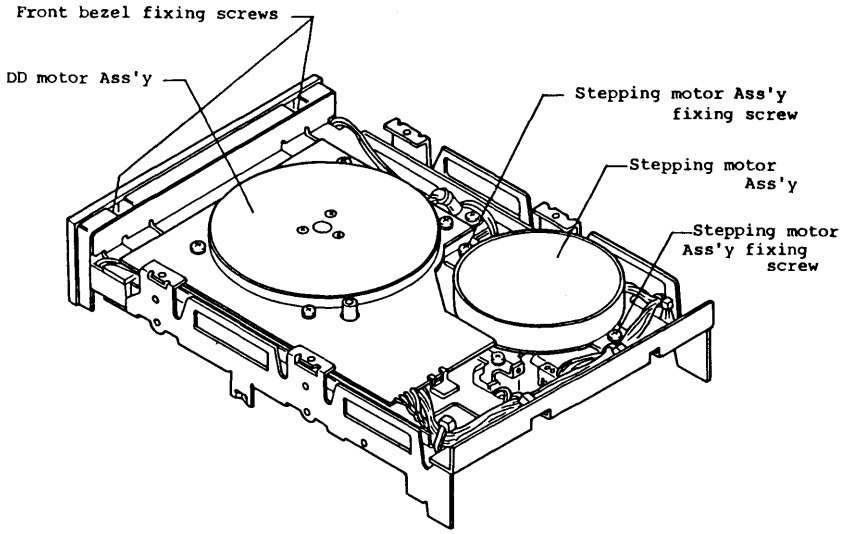
(Table 501) Main parts configuration of FD-54



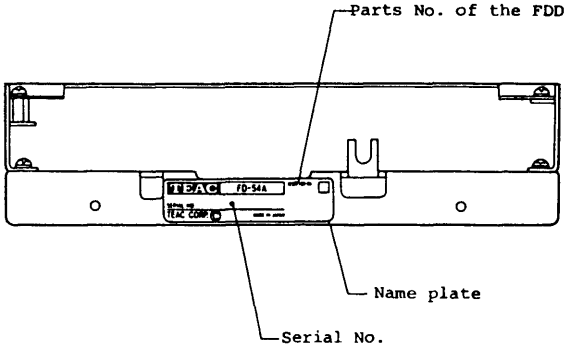
(Fig.501) External view (No.1)



(Fig.502) External view (No.2)



(Fig.503) External view (No.3)



(Fig.504) External view (No.4)

5-2. MECHANICAL BREAK-DOWN AND PARTS LIST

5-2-1. FDD (Refer to Fig.505)

Nos.	Parts Nos.	Parts name	Q'ty	Description
1	16152892-00	Chassis	1	
2	16802621-00	PCB fixing plate	1	
3	16787144-00	Disk guide	1	
4	16730435-00	Collar	2	
5	16730433-00	Collar B	1	
6	16802622-00	T00 stopper	1	
7	14733780-00	DD motor Ass'y(C)(Spindle motor)	1	
8	16757130-00	T00 bracket	1	
9	15532004-00	PCBA T00 sensor(C)	1	
10	17966927-00	CSS Ass'y(C)	1	FD-54B
11	13189135	Terminal	1	
12	14733770-00	Stepping motor Ass'y(C)	1	
13	17966912-00	Head carriage Ass'y(C)	*1	FD-54A
	17966863-00	Head carriage Ass'y(C)		FD-54B
14	16766631-XX	Guide shaft(C)	2	Note 4
15	16766638-00	Guide shaft clip	2	
16	16802624-00	Band fixing plate A	1	
17	16802623-00	Band fixing plate B	1	
18	16385130-00	Band spring	1	
19	16792300-00	Steel belt (C)	1	
20	16766636-00	Band washer	1	

(Table 502) FDD parts list (1/3)

Nos.	Parts Nos.	Parts name	Q'ty	Description
21	16152891-00	Upper chassis	1	
22	16787150-00	Insulation sheet	1	
23	16787151-00	Disk pad B	1	Note 3
24	16802616-00	Set arm	1	
25	17966929-00	Clamp cam Ass'y(C)	1	
26	16787148-00	Clamp shaft holder	1	
27	16392019-00	Clamp spring	1	
28	16381104-00	Clamp return spring	1	
29	17966933-00	Collet shaft plate Ass'y	1	
30	17966923-00	Collet Ass'y(C)	1	
31	17966935-00	Bail Ass'y(A)	*1	FD-54A
	17966936-00	Bail Ass'y(B)		FD-54B
32	16787157-00	Disk pad A-2	1	Note 3
32B		Disk pad	1	Note 3
33	16381106-00	Disk pad lever spring	1	
34	15090730-00	Front OPT Ass'y(C)	1	
35	15532006-XX	PCBA MFD control(C)	1	Note 5
36	16787152-00	Protection sheet	1	
37	16730434-00	Fixing shaft	1	
38	16787149-00	PCB holder	1	
39	16322054-00	Cord clamper	1	
40	16362418-00	Cable tie	4	

(Table 502) FDD parts list (2/3)

Nos.	Parts Nos.	Parts name	Q'ty	Description
41	17966807-50	Front bezel Ass'y	1	Note 6
42	17966924-00	Front lever Ass'y(C)	1	Note 6
43	16381109-00	Front lever spring	1	
44	17966937-00	Shield cover Ass'y	1	

(Table 502) FDD parts list (3/3)

Notes: 1. As to the parts with an asterisk in the Q'ty column, select appropriate one for the model.

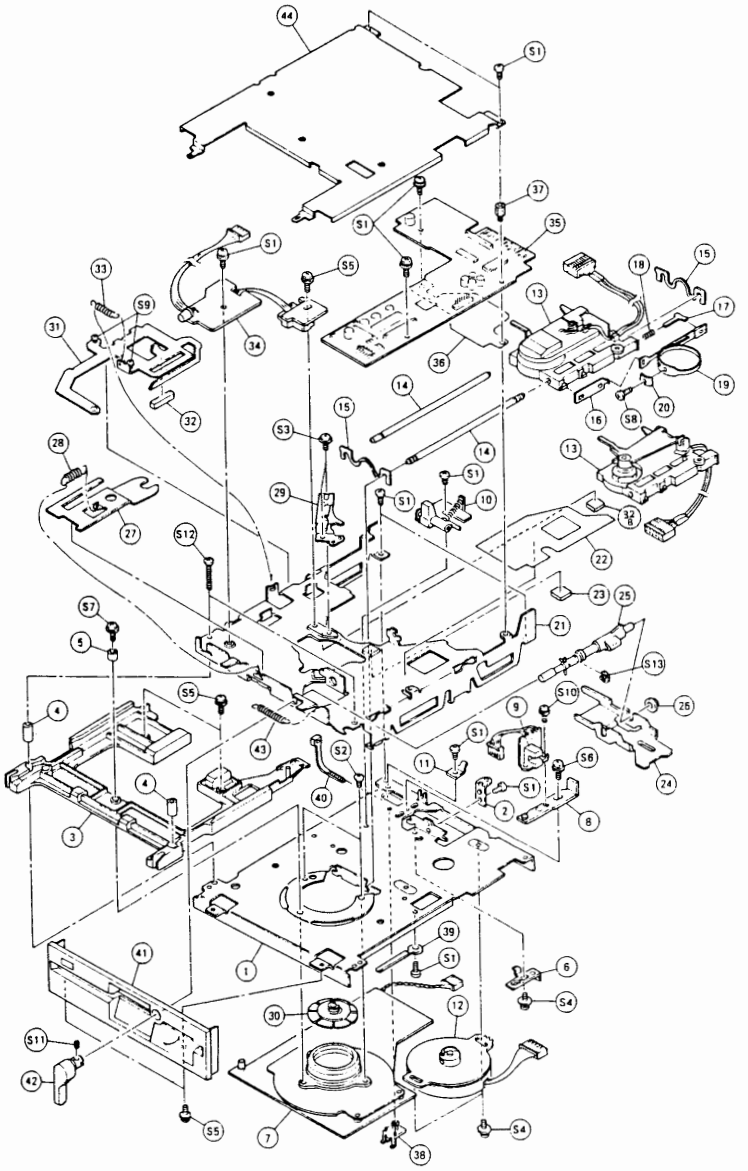
2. As to the parts with model name of FD-54 in the Description column, the parts is used only for the model.

3. Disk pads are included in the Ass'y No.21 and No.31.

4. Guide shafts are always used in combination with the head carriage Ass'y due to make the corresponding diameter match with the hole of the head carriage. When you replace the head carriage Ass'y, be sure to replace the guide shafts together.

5. The parts number versions of the PCBA MFD control (C) are different depending on each model. Refer to the name plate on the actual PCBA installed to designate the same version.

6. The parts numbers of the front bezel Ass'y and the front lever Ass'y are those of FD-54, standard color, black.



(Fig.505) Mechanical section break-down

5-2-2. Screw, Washer

Nos.	Parts Nos.	Parts name	Description
S1	16410304	Screw,bind,3x4,S,ZMC	
S2	16411304	Screw,bind,3x4, B,BNM	
S3	16400304	Screw,pan,three pieces,3x4,S,ZMC	
S4	16498647	Screw,pan,three pieces,3x5,S,ZMC	
S5	16410306	Screw,bind,3x6,S,ZMC	
S6	16498579	Screw,pan,three pieces,3x6,S,ZMC	
S7	16476308	Screw,pan,flat,flat washer,3x8,B,BNM	
S8	16470004	Screw,pan,sems,2.6x4,S,ZMC	
S9	16400004	Screw,pan,2.6x4,S,ZMC	
S10	16400204	Screw,bind,2x4,S,ZMC	
S11	16498260-00	Set screw,3x3	
S12	16410316	Screw,bind,3x16,S,ZMC	
S13	16351140	E-ring,3J	

(Table 503) Parts list of screw & washer

5-3. PCBA PARTS LIST

Following shows all the parts mounted on the PCBAs of FD-54 series.

5-3-1. PCBA MFD Control (C)

Parts Nos.	Parts name & rating	Location
13447358-00	LSI TEAC 7358-00	U1
13441922-00	LSI TEAC 1922-00	U2
13441983	TTL IC 74LS368A	U3
13441235	TTL IC 74LS04	U4
13428139	Transistor array,M54578P	U5
13424286	Transistor,2SC2021R	Q3,Q4
13421211	Transistor,2SA881 Q·R	Q1
13411378	Diode,pair,MA154WA	CRA1,CRA2,CRA5,CRA6, **CRA3,**CRA4
13411406	Diode,pair,MA154WK	CRA7
13411243	Diode,1S954	CR1,CR4∿CR8
13411339	Diode,DS442X	CR8
13415408	Diode,zener,RD6.8EN2	CR2
13497262	Resistor array,SA 9-1KΩ,J	RA1
13497310	Resistor array,SA 5-15KΩ,J	RA3

(Table 504) PCBA MFD control (C) parts list (1/4)

Parts Nos.	Parts name & rating	Location
13497266	Resistor array,SA 3-4.7KΩ,J	RA4
13497286	Resistor array,SC 4-2.2KΩ,J	RA2
13497228-00	Resistor array,T-7228	RA5
13497227-00	Resistor array,T-7227	RA7
13497229-00	Resistor array,T-7229	RA6
11187105	Resistor,RD,1/6W,1MΩ,J	R16
11187473	Resistor,RD,1/6W,47KΩ,J	**R15,R18
11187682	Resistor,RD,1/6W,6.8KΩ,J	R17
11187222	Resistor,RD,1/6W,2.2KΩ,J	R20
11198104	Resistor,RD,1/4W,100KΩ,J	R10
11198497	Resistor,RN,1/4W,1.24KΩ,F	R19
11051121	Resistor,RN,1W,120Ω,J	R21
11051390	Resistor,RN,1W,39Ω,J	R13,R14
13040341	Jumping wire	**S1
12903343	Capacitor,CE,10V,100μF,M	C2
12903353	Capacitor,CE,25V,47μF,M	C24
12903345	Capacitor,CE,16V,22μF,M	C6,C8
12903227	Capacitor,CS,20V,15μF,M	C7,C9
12903154	Capacitor,CS,16V,47μF,M	**C33,C34
12903152	Capacitor,CS,16V,2.2μF,K	C36
12903178	Capacitor,CS,35V,0.22μF,K	C13,C14
12903177	Capacitor,CS,35V,0.15μF,M	C11,C12
12903375	Capacitor,CS,16V,1μF,M	C17

(Table 504) PCBA MFD control (C) parts list (2/4)

Parts Nos.	Parts name & rating	Location
12903372	Capacitor,CS,16V,0.33μF,M	C5
12903080	Capacitor,CC,25V,YU,0.1μF,M	C26,C28
12903335	Capacitor,CC,25V,X,0.022μF,Z	C3,C4,C10,C15,C16,C20 C27,C31,C32
12902530	Capacitor,CC,500V,F,0.01μF,Z	C1
12901421	Capacitor,CC,50V,B,2200PF,K	C25
12901417	Capacitor,CC,50V,B,1000PF,K	C29
12900771	Capacitor,CC,50V,SL,180PF,J	C18,C19
12902588	Capacitor,CC,50V,CH,56PF,J	C22
12902578	Capacitor,CC,50V,CH,22PF,J	C23
12454222	Capacitor,CQ,100V,2200PF,G	C30
12454152	Capacitor,CQ,100V,1500PF,G	C35
12454101	Capacitor,CQ,100V,100PF,G	C21
13295084-00	Ceramic oscillator,480KHz	Y1
14723507	Coil,chalk,330μH,J	L1∿L3
13121234	Connector,S6P,polarizing	*J9
13121152	Connector,W12P,polarizing	
13121361	Connector,S5P	TP7∿10,G
13121363	Connector,S7P	TP1∿6,G
13121332	Connector,W14P	HS∿1U

(Table 504) PCMB MFD control (C) parts list (3/4)

Parts No.s	Parts name & rating	Location
13121109	Connector,4P	J2
16322368	Connector,clamp	for J2 installation
13121175	Connector,4P	J7
13121176	Connector,5P	J5
13121177	Connector,6P	J4,J6
13121149	Short bar	HSM,HL,IU,HS,DS0~3,HM straps
16271169-XX	Name plate	

(Table 504) PCBA MFD control (C) parts list (4/4)

Notes: 1. Parts with an asterisk are different depending on the PCBA versions. Select either of them.

2. Parts with a double asterisks are not used in some PCBA versions.

3. Refer to the schematic diagram of the PCBA as to the details of the parts with asterisks.

4. Name plate version is different depending on the PCBA version used.

Parts No.s	Parts name & rating	Location
13121109	Connector,4P	J2
16322368	Connector,clamp	for J2 installation
13121175	Connector,4P	J7
13121176	Connector,5P	J5
13121177	Connector,6P	J4,J6
13121149	Short bar	HSM,HL,IU,HS,DS0~3,HM straps
16271169-XX	Name plate	

(Table 504) PCBA MFD control (C) parts list (4/4)

Notes: 1. Parts with an asterisk are different depending on the PCBA versions. Select either of them.

2. Parts with a double asterisks are not used in some PCBA versions.

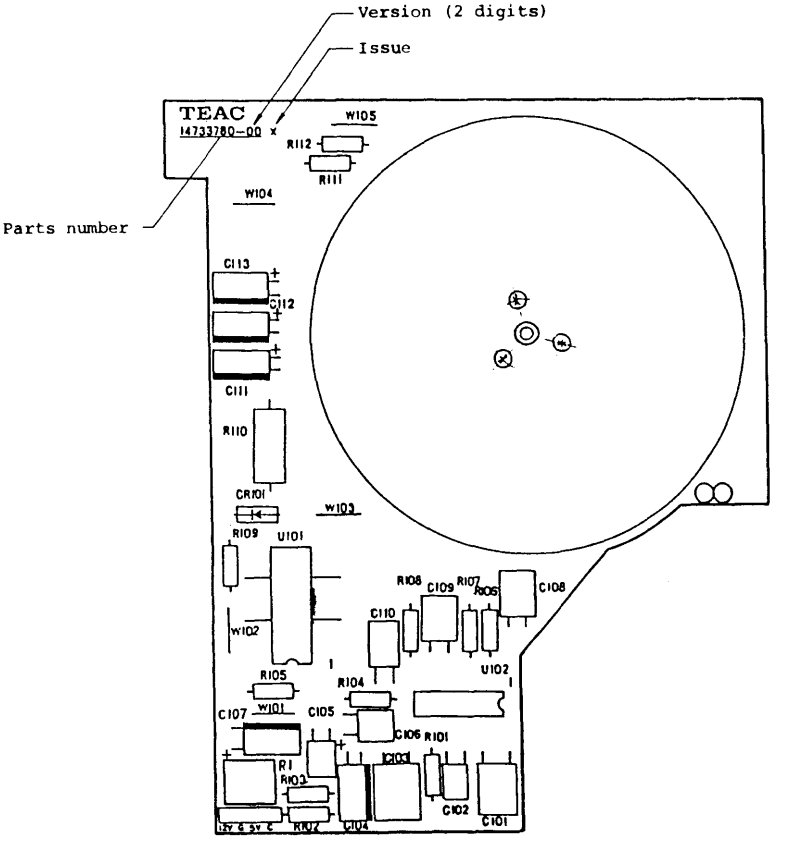
3. Refer to the schematic diagram of the PCBA as to the details of the parts with asterisks.

4. Name plate version is different depending on the PCBA version used.

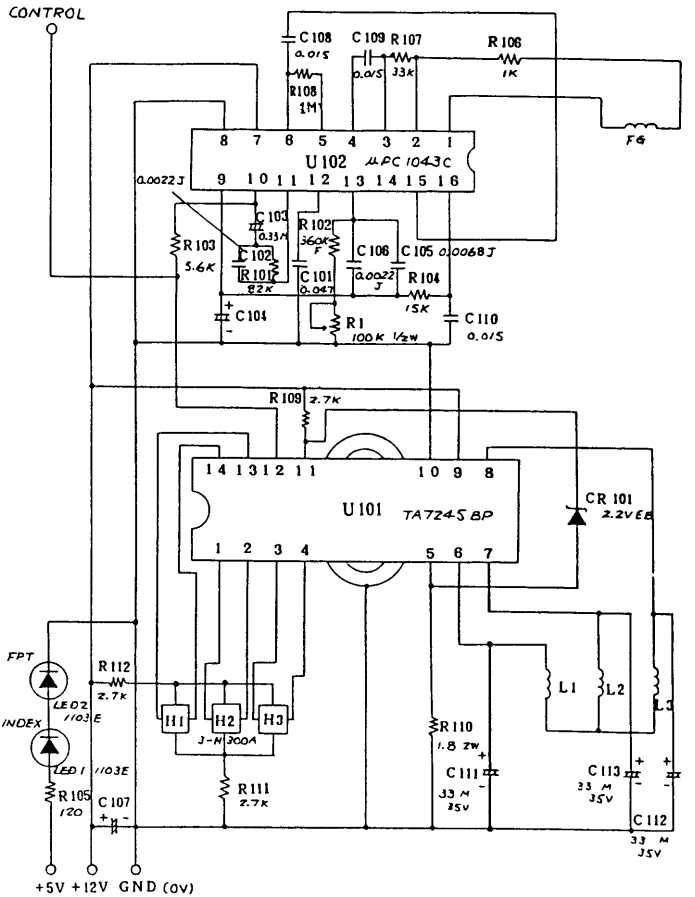
5-4. SCHEAMTIC DIAGRAMS AND PARTS LOCATION

SPARE PAGE

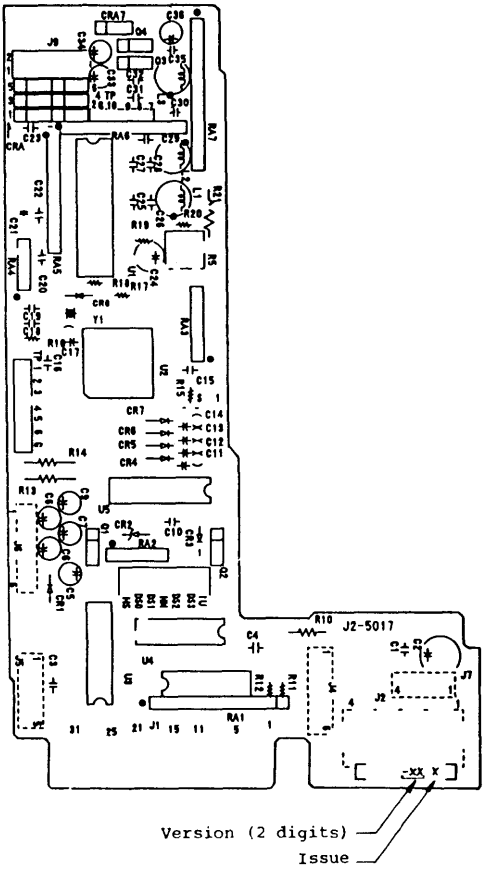
SPARE PAGE



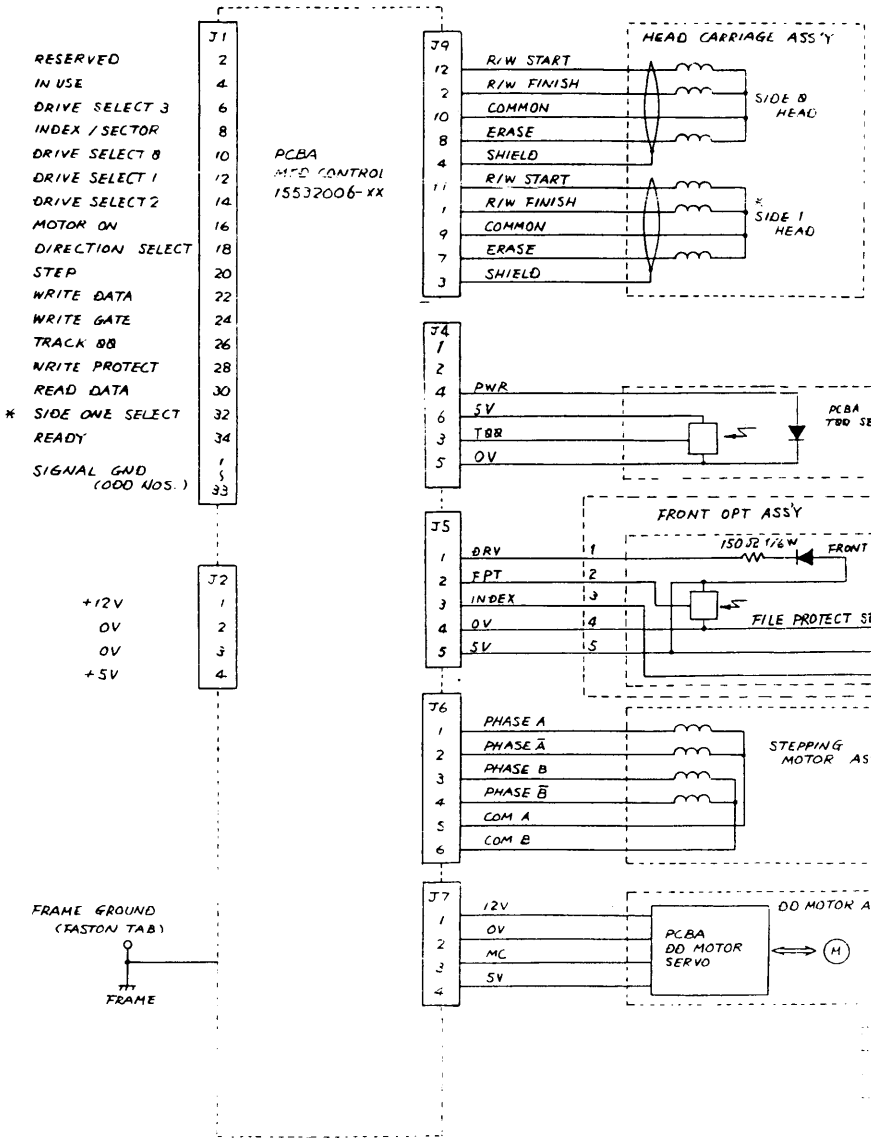
PCBA DD MOTOR SERVO (Type C)
PARTS LOCATION



PCBA DD MOTOR SERVO (Type C)
SCHEMATIC DIAGRAM



PCBA MTD CONTROL, PARTS LOCATION



VERSION TABLE

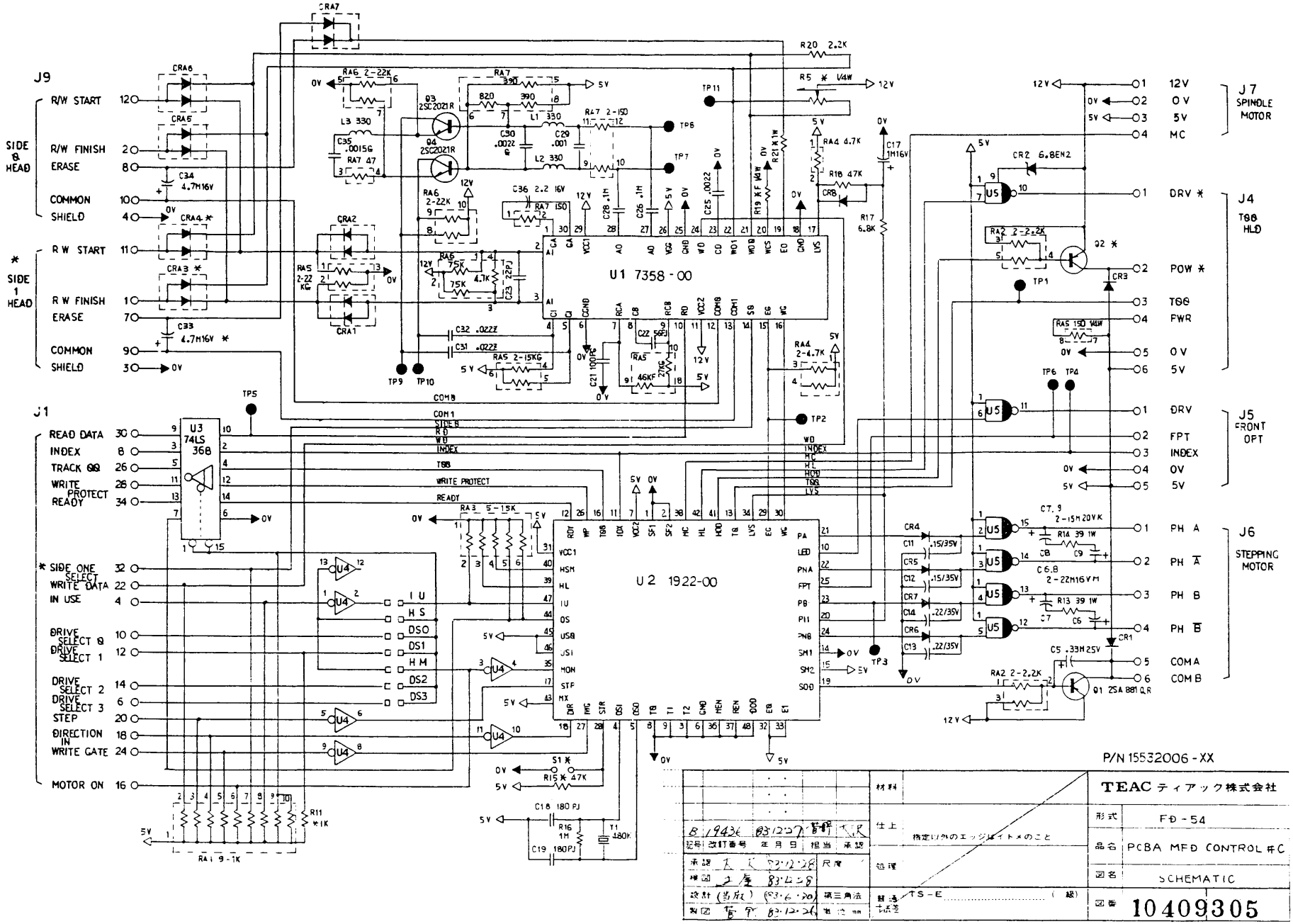
FDD VERSION	MAIN SPEC	* PARTS & SIGNALS	NOTE
A-00	S SIDE		
B-02	D SIDE	S1 HEAD SIDE ONE SELECT	
A-04	S SIDE	MECHANISM ONLY (WITHOUT PCBA MFD CONTROL & T00 SENSOR)	

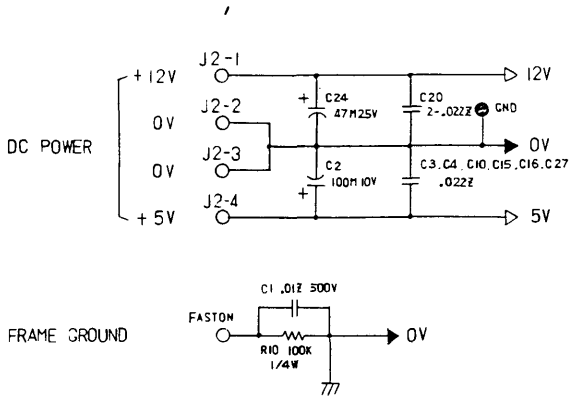
2. ABBREVIATED NAMES ARE AS FOLLOWS
S SIDE : SINGLE SIDE D SIDE : DOUBLE SIDE
S1 HEAD : SIDE ONE HEAD

NOTE 1. PARTS AND SIGNALS WITH AN ASTERICK (*) ARE USED ONLY FOR THE DOUBLE SIDED MODEL.

P/N 19307120-XX

	材料	TEAC ティアック株式会社
B 1986 12 26	仕上	形式
	処理	品名 FD-54
		図名 TOTAL DIAGRAM
		図番 10409304


J9
R/W START
R/W FINISH
ERASE
COMMON
SHIELD
SIDE 0 HEAD
R W START
R W FINISH
ERASE
COMMON
SHIELD
SIDE 1 HEAD
J1
READ DATA
INDEX
TRACK 00
WRITE PROTECT
READY
SIDE ONE SELECT
WRITE DATA
IN USE
DRIVE SELECT 0
DRIVE SELECT 1
DRIVE SELECT 2
DRIVE SELECT 3
STEP
DIRECTION IN
WRITE GATE
MOTOR ON
U1 7358-00
U2 1922-00
U3 74LS 368
J7 SPINDLE MOTOR
12V
0V
5V
MC
J4 T00 HLD
DRV *
POW *
T00
PWR
J5 FRONT OPT
DRV
FPT
INDEX
J6 STEPPING MOTOR
PH A
PH Ā
PH B
PH B̄
COM A
COM B
P/N 15532006-XX
TEAC ティアック株式会社
形式 FD-54
品名 PCBA MFD CONTROL #C
図名 SCHEMATIC
図番 10409305



PCBA VERSIONS	MAIN SPEC,	* PARTS
-00	48tpi S.Side A.STD	R19 (1.24K). R21 (120) S1 J9 (6P)
-01	48tpi D.Side B STD	R19 (1.24K). R21 (120). R15 (4.7K) CRA3. CRA4. C33. J9 (12P) SIDE 1 HEAD

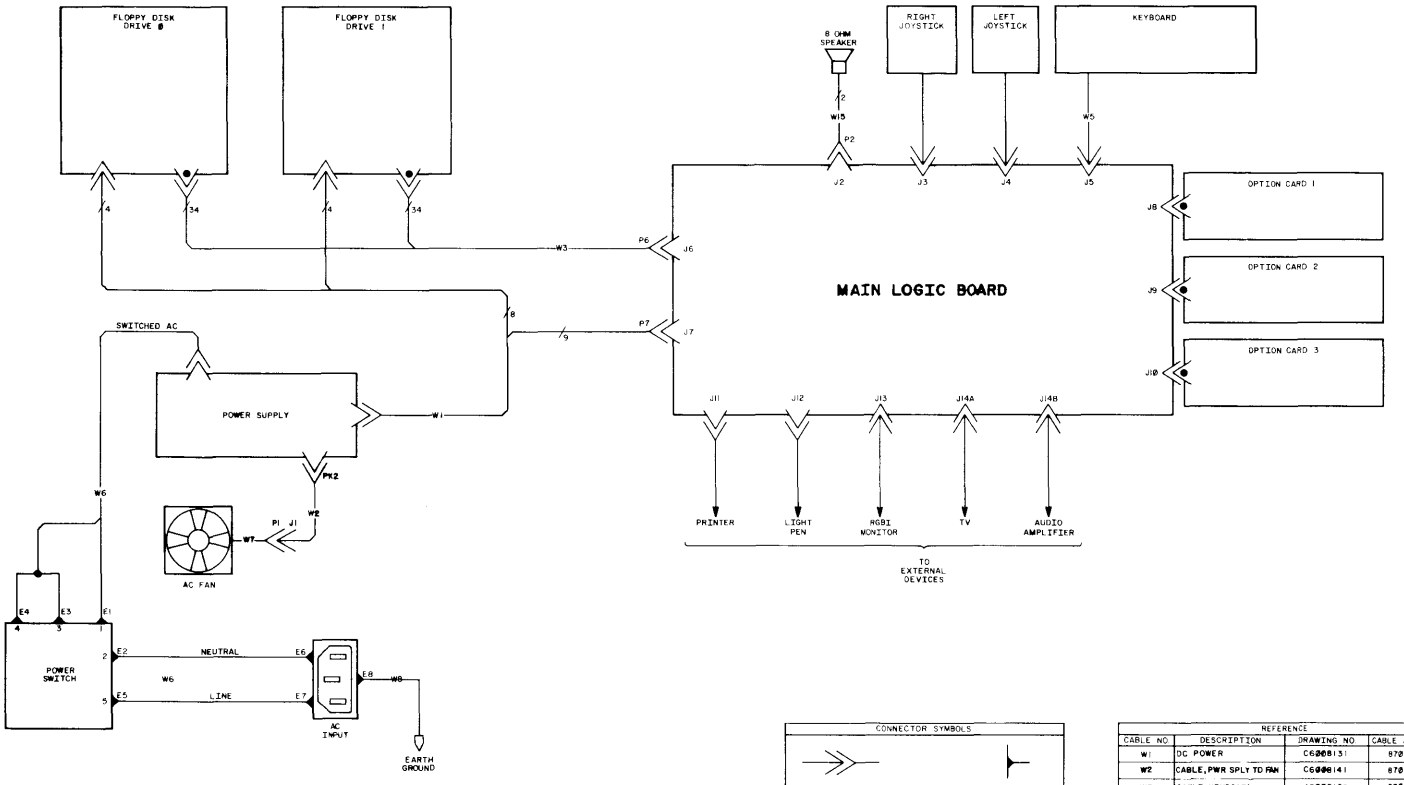
VERSION TABLE P/N 15532006 -XX

6. POLARIZING KEY POSITIONS FOR CONNECTORS (J) ARE :
   J1: BETWEEN PIN4 AND 6 , J9: PIN6
5. REFER TO SHORT BAR SELECTION TABLE (HSM~DS3) AS TO THE SHIPPING POSITIONS.
4. TOLERANCE SYMBOLS FOR R. RA. AND C ARE :
   F: ±1% , G: ±2% , J: ±5% , K: ±10% , M: ±20% , Z: +80-20%
3. CAPACITOR (C) VALUES ARE IN MICROFARADS, 50V OR HIGHER, ±10% (K). UNLESS OTHERWISE SPECIFIED.
2. RESISTOR (R) AND RESISTOR ARRAY (RA) VALUES ARE IN OHMS, 1/8W OR GREATER, ±5% (J). UNLESS OTHRWISE SPECIFIED.

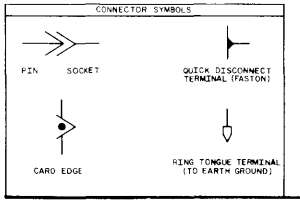
NOTES 1. PARTS WITH AN ASTERISK (*) ARE DIFFERENT IN EACH PCBA VERSION. REFER TO VERSION TABLE. UNLISTED PARTS ARE NOT USED IN THAT VERSION.

材料		TEAC ティアック株式会社	
仕上	指定以外のエッジはイトメのこと	形式	FD-54
処理		品名	PCBA MFD CONTROL #C
普通寸法差	TS-E (級)	図名	SCHEMATIC
記号 改訂番号 年月日 担当 承認		図番	10409305
承認 大沢 83.12.28 R屋			
検図 土屋 83.12.28			
設計 (当放) (83.6.30) 第三角法			
製図 菅野 83.12.26 単位 mm			

CONNECTORS AND PIN DESIGNATIONS



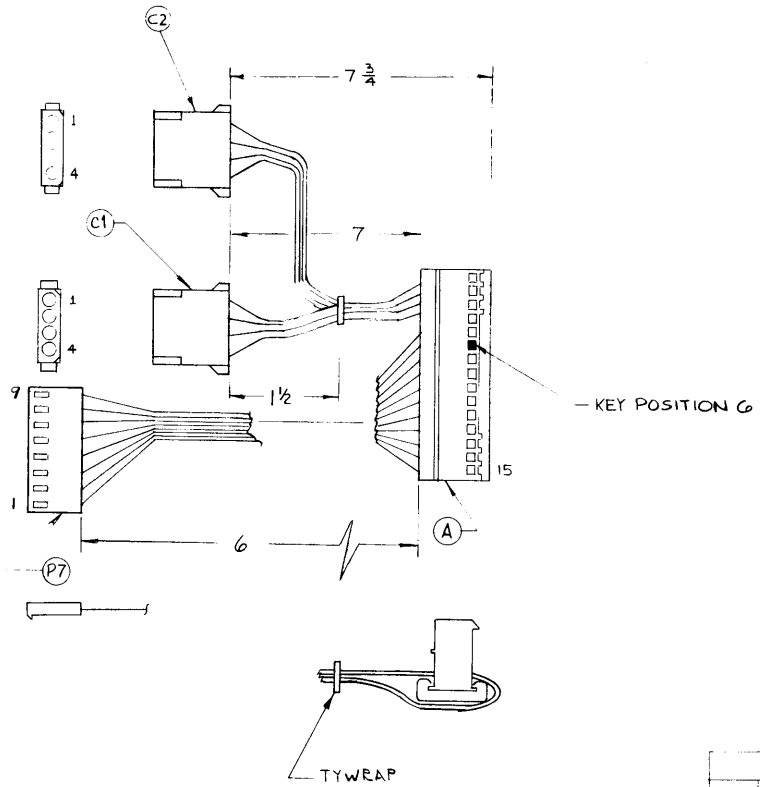
Connector/Cable Interconnection (8000231)



CABLE NO.	DESCRIPTION	REFERENCE DRAWING NO	CABLE ASSY P/N
W1	DC POWER	C60**0**8131	870-9558
W2	CABLE, PWR SPLY TO FAN	C60**0**8141	870-9575
W5	CABLE, KEYBOARD	A60**0**8129	870-9567
W6	AC PWR	C60**0**8121	870-9553
W3	SIGNAL, FLOPPY DISK	C60**2**8057 ⚠	870-9447
W7	FAN	C26**0**0069	
W8	EARTH GROUND	A60**0**8125	870-9552
W15	SPEAKER	C60**0**8170	870-9470

⚠ CABLE DWG C60**0**8057 WILL BE USED IF CABLE TWIST IS REQUIRED TO CONNECT TO FLOPPY DISK DRIVES, OTHERWISE USE CABLE DWG C60**0**8118

NOTES:

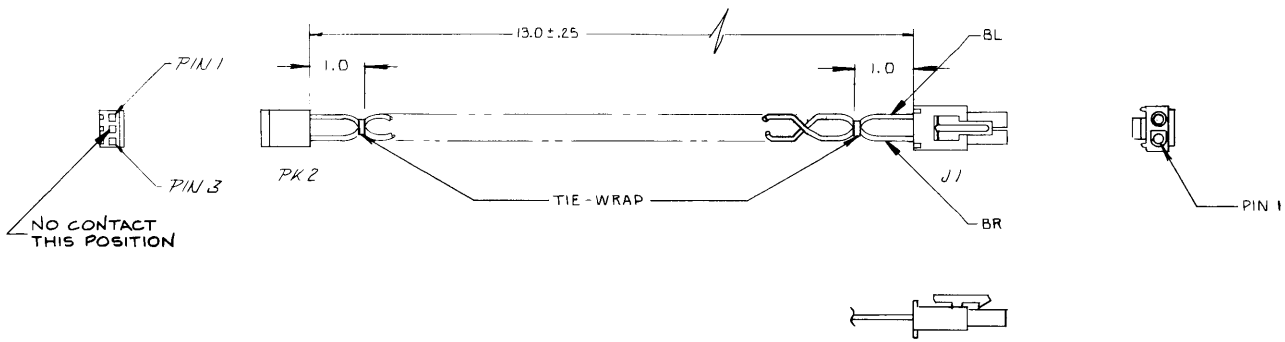


Cable, Assembly W1(6008131)

WIRE LIST						
FUNCTION	COLOR	AWG	A	P7	C1	C2
-12 V	WHITE	18	15	8		
GROUND	BLACK	18	14	7		
GROUND	BLACK	18	13	6		
GROUND	BLACK	18	12	5		
+5V	RED	18	11	3		
+5V	RED	18	10	2		
+5V	RED	18	9	1		
GROUND	BLACK	18	8	4		
+12V	VIOL.	18	7	9		
KEY			6			
+12V	VIOL.	18	5		1	
+12V	VIOL.	18	5			1
GROUND	BLACK	18	4		2	
GROUND	BLACK	18	4			2
GROUND	BLACK	18	3		3	
GROUND	BLACK	18	3			3
+5V	RED	18	2		4	
+5V	RED	18	2			4
NC CONN.			1			

3 - OR EQUIVALENT
2 - TOLERANCE: ± 1/4
1 - TY-WRAPS AS REQUIRED

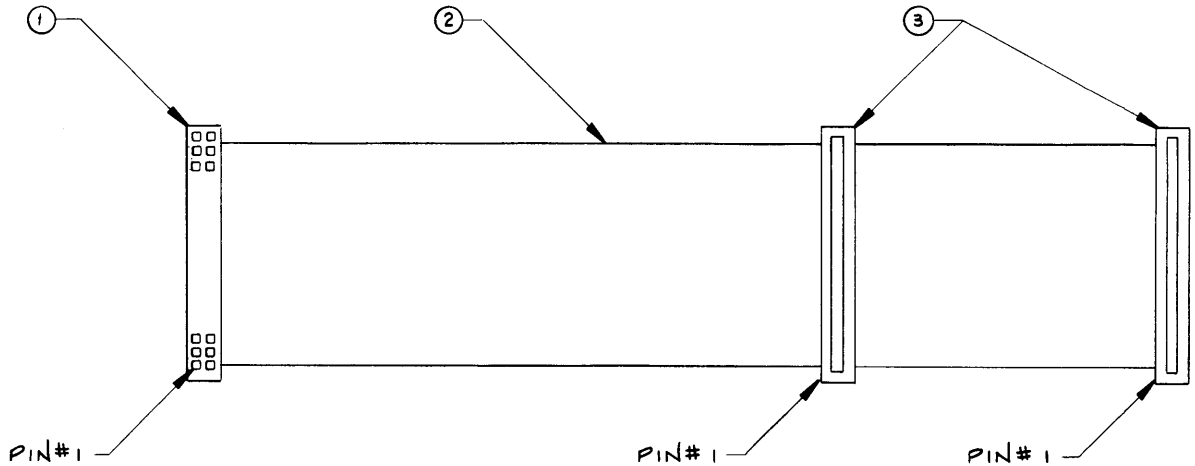
PARTS LIST				
ITEM	QTY	DESCRIPTION	MANUF./PART NO.	REMARKS
A	1	CONNECTOR-15 POSITION	MOLEX 09-06-1157	WITH LOCKING RAMP
P7	1	CONNECTOR- 9 POSITION	MOLEX 09-50-3091	WITH LOCKING RAMP
C1-C2	2	CONNECTOR- 4 POSITION	AMP 1-480424-0	
	9	CONTACTS FOR P7	MOLEX 08-50-0105	
	8	CONTACTS FOR C1 & C2	AMP 61117-1	
KEY	1	FOR ITEM A	MOLEX 15-04-0288	POSITION 6 OF A
COVER	1	FOR ITEM A	MOLEX 15-05-7154	

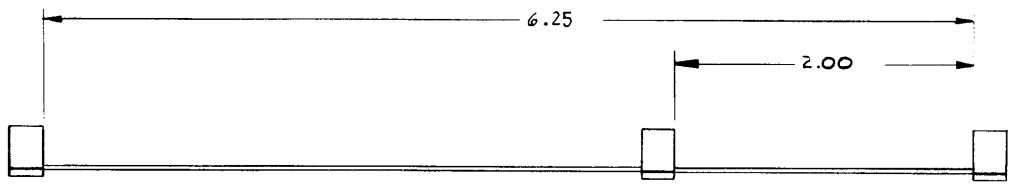


WIRE LIST									
FUNCTION	WIRE		CONNECTOR				PIN#		
	AWG	COLOR	PK2	J1					
LINE	18	BRN	1	1					
NEUTRAL	18	BLU	3	2					

Cable, Assembly W2(6008141)

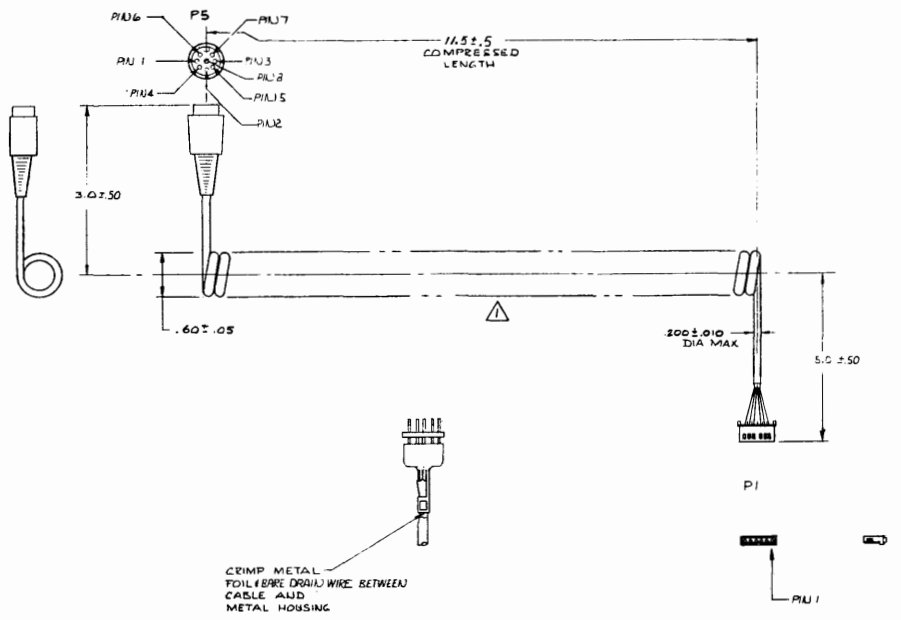
PARTS LIST				
DES	QTY	DESCRIPTION	MFG/PN	REMARKS
PK2	1	CONNECTOR 2 POS	MOLEX / 26-03-4030	
	2	CONTACTS	MOLEX / 08-50-0187	
J1	1	CONNECTOR 2 POS	MOLEX / 19-09-1029	OR EQUIVALENT
	2	CONTACTS	MOLEX 02-09-2101	OR EQUIVALENT
BR	AR	WIRE 18 AWG BROWN		80°C (LINE)
BL	AR	WIRE 18 AWG BLUE		80°C (NEUTRAL)





PARTS LIST				
ITEM	QTY	DESCRIPTION	MFG / PART NO.	REMARKS
①	1	CONNECTOR-34 POS. RECEPTACLE	MOLEX-15-29-3343	
②	1	CABLE-RIBBON, 34 CONDUCTOR		.050 PITCH
③	2	CONNECTOR-34 PIN EDGE CARD	3M-3463-0001/AMP499930-3	

Cable, Signal W3(6008118)



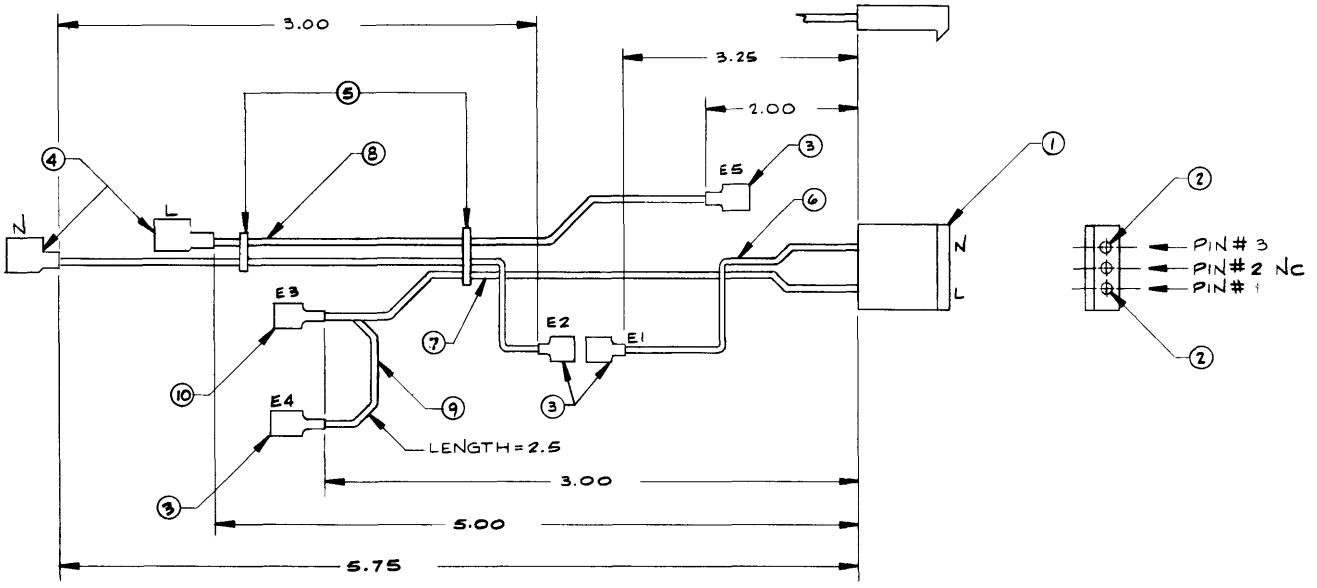
WIRE LIST								
FUNCTION	WIRE		CONNECTOR / PIN NO					
	AWG	COLOR	P5	P1				
KBDDAT	26	WHITE	1	6				
KBDCLK	26	GRN	4	4				
+5DBS+	26	YEL	2	3				
+5V DC	26	RED	7	2				
GND	26	BLACK	3	1				
RESET*	26	BLUE	6	5				

Keyboard Assembly W5(6008129)

PARTS LIST				
DES	QTY	DESCRIPTION	MFG / PART NO	REMARKS
P5	1	CONN 8 PIN DIN	HOSHIDEN TCP-0288-ON-0A01	
P1	1	6 CKT HOUSING	MOLEX #50-37-5063	
	6	CONTACT	MOLEX #08-70-1039	

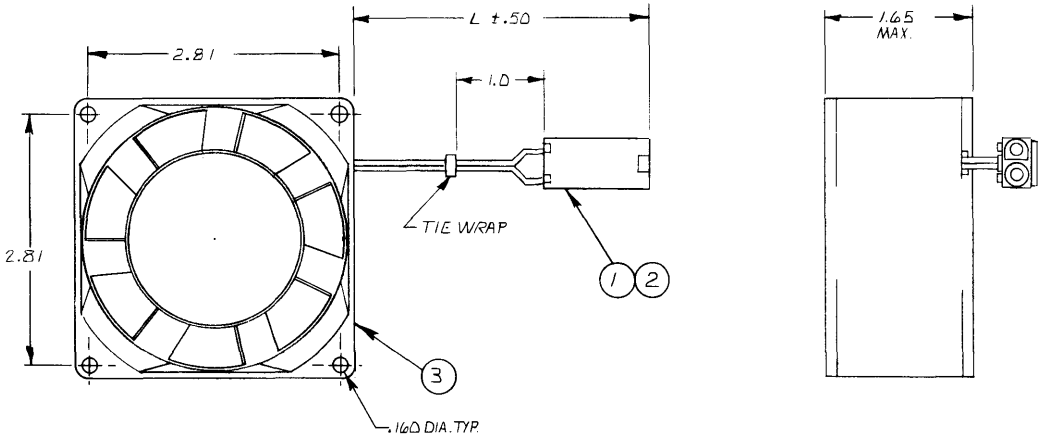
⚠ CABLE IS 6 CONDUCTOR SHIELDED;
EACH CONDUCTOR IS 26 AWG, 7 WIRE STRANDED;
FOIL SHIELD WITH DRAIN WIRE;
OUTER JACKET IS TANDY FAWN/GRAY TPR.

NOTES (UNLESS OTHERWISE SPECIFIED):



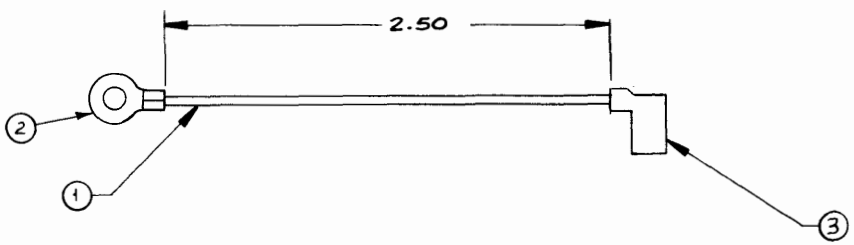
Cable, Assembly W6(6008121)

PARTS LIST				
LTR	QTY	DESCRIPTION	PART MFG NO	REMARKS
1	1	CONNECTOR - 3 PIN	MOLEX 26-03-4030 (2)	
2	2	CONTACT	MOLEX 08-50-0187 (2)	
3	4	FASTON-(.25 X .032)	AMP# 2-520183-2 (2)	FULLY INSULATED
4	2	FASTON-RIGHT ANGLE(.25X032)	AMP # 2-520128-2 (2)	FULLY INSULATED
5	2	TY-WRAP		
6	1	WIRE - 18 AWG, BLUE		
7	1	WIRE - 18 AWG, BROWN		
8	1	WIRE - 18 AWG BROWN		
9	1	WIRE - 18 AWG BROWN		
10	1	FASTON (.25 X .032)	AMP#3-350819-2 (2)	FULLY INSULATED



Cable, Assembly W7(2600009)

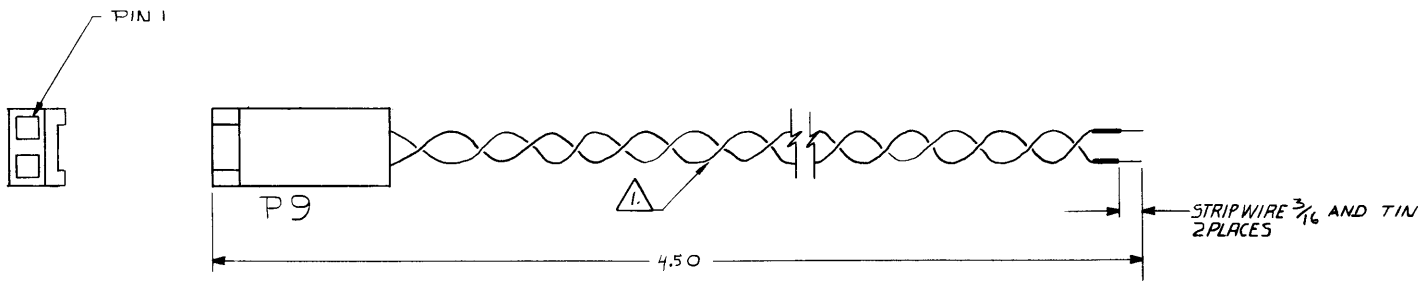
ITEM NO.	QTY.	DESCRIPTION	MFG / PART NO.	DIM. L	REMARKS
1	1	CONNECTOR-MALE	MOLEX/19-09-2029	—	
2	2	PINS	MOLEX/02-09-1132	—	
3	1	FAN	ROTRON/3U2E1	5.0	
			TORIN/31022-20	3.75	ALTERNATE
			NMB/EP075-38-GZL1	5.50	ALTERNATE
			VENTILS/VS284	3.75	ALTERNATE



PARTS LIST				
ITEM	QTY	DESCRIPTION	MFG PART NO.	REMARKS
1	1	WIRE - 18 AWG, GREEN W/ YELLOW STRIPE		
2	1	RING TERMINAL	AMP* 350981-2 (2)	
3	1	FASTON (.25 X .032) RIGHT ANGLE	AMP # 2-520128-2 (2)	

(2) OR EQUIVALENT
1. CABLE TOLERANCE ± .25

Cable, ground W8(6008125)

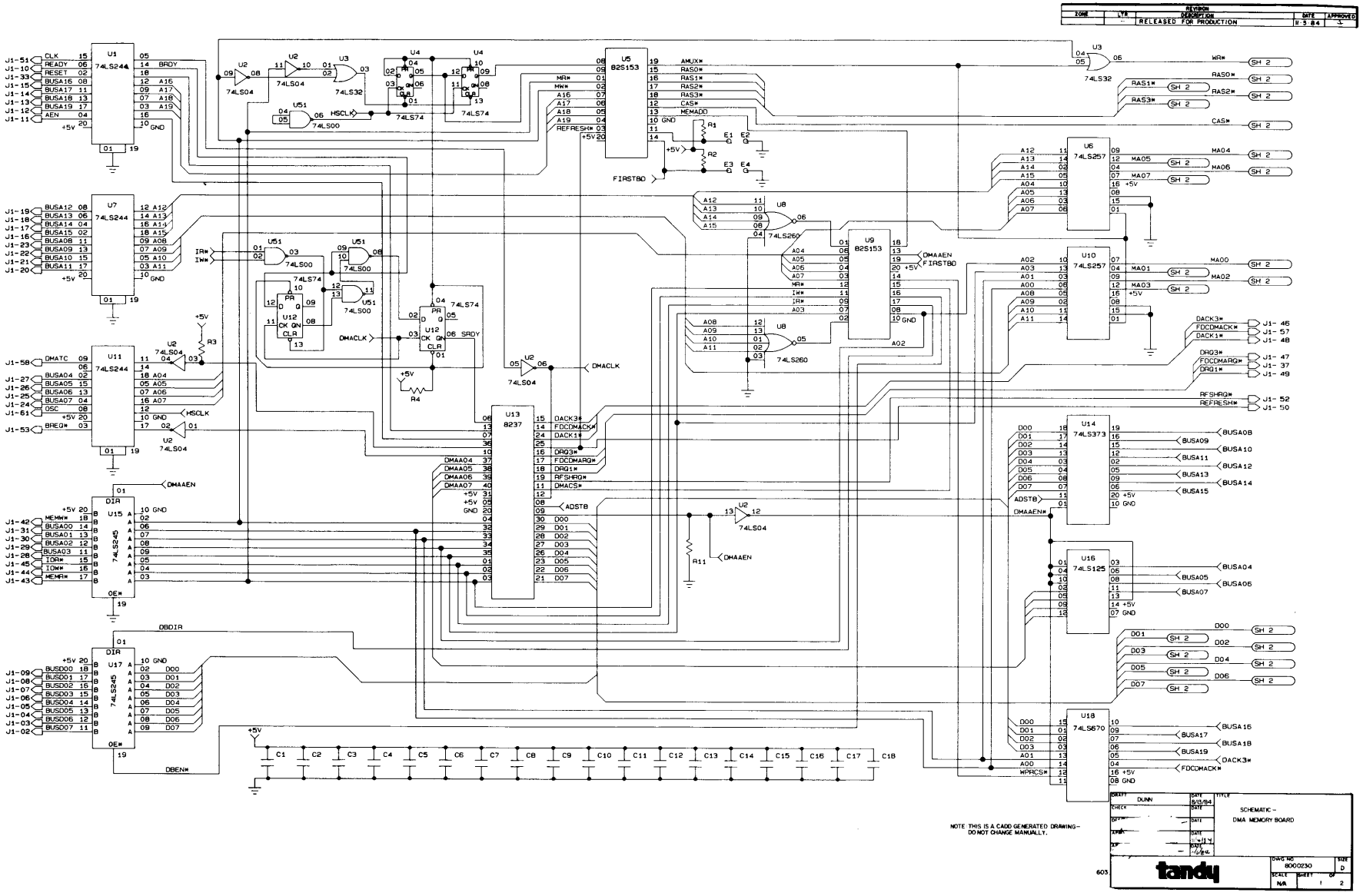


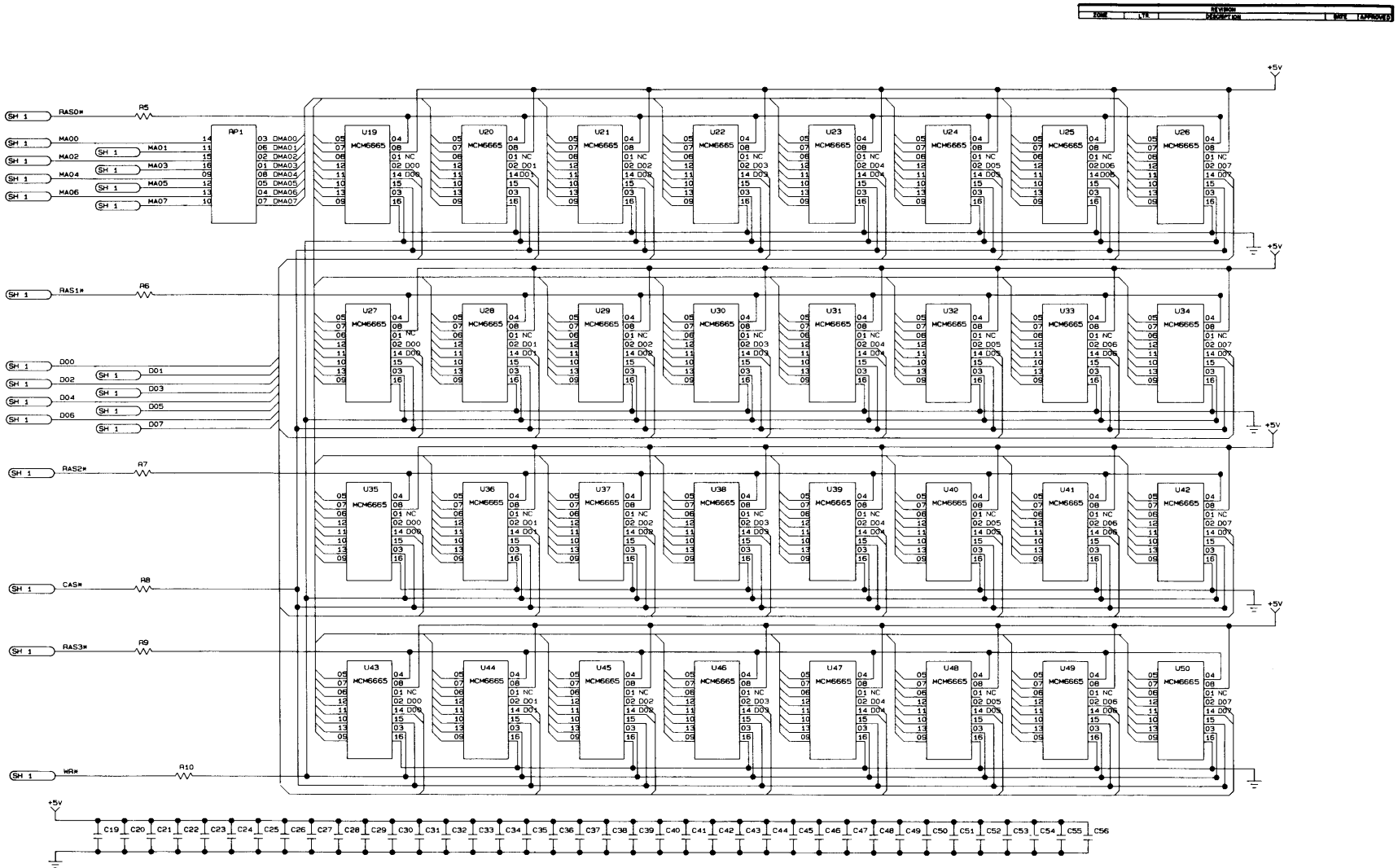
WIRE LIST				
FUNCTION	WIRE		CONNECTOR / PIN NO.	
	AWG	COLOR	P-9	
SPKROUT	24	GRY	1	TO SPEAKER + TERMINAL
GND	24	BLK	2	TO SPEAKER - TERMINAL

Cable, Assembly W15(6008070)

PARTS LIST				
DES	QTY	DESCRIPTION	MFG / PART NO.	REMARKS
P9	1	CONN SOCKET 2 POS	MOLEX / 22-01-3027	
	2	CONTACT	MOLEX / 08-50-0113	

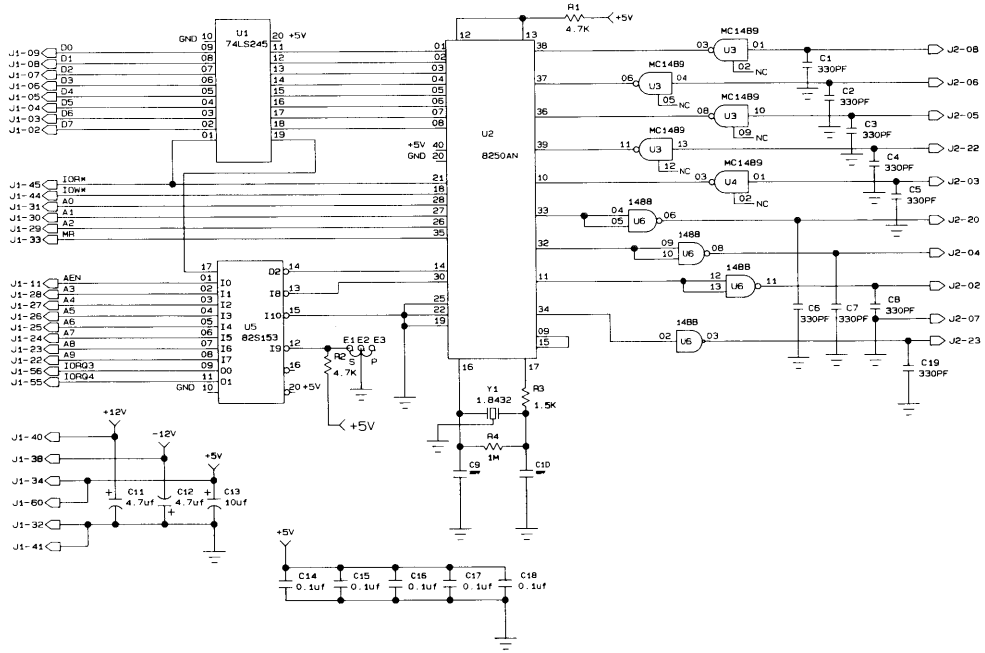
Memory DMA


REVISION
RELEASED FOR PRODUCTION
NOTE THIS IS A CADD GENERATED DRAWING- DO NOT CHANGE MANUALLY.
SCHEMATIC - DMA MEMORY BOARD
DWG NO 8000230
tandy


ZONE
LTR
REVISION DESCRIPTION
DATE
APPROVED
RAS0*
RAS1*
RAS2*
RAS3*
CAS*
WR*
MA00
MA01
MA02
MA03
MA04
MA05
MA06
MA07
D00
D01
D02
D03
D04
D05
D06
D07
R5
R6
R7
R8
R9
R10
RP1
DMA00
DMA01
DMA02
DMA03
DMA04
DMA05
DMA06
DMA07
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U48
U49
U50
MCM6665
+5V
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
C50
C51
C52
C53
C54
C55
C56
NOTE
THIS IS A CADD GENERATED DRAWING -
DO NOT CHANGE MANUALLY.
DWG NO
8000230
SIZE
D
SCALE
NONE
SHEET
2
OF
2

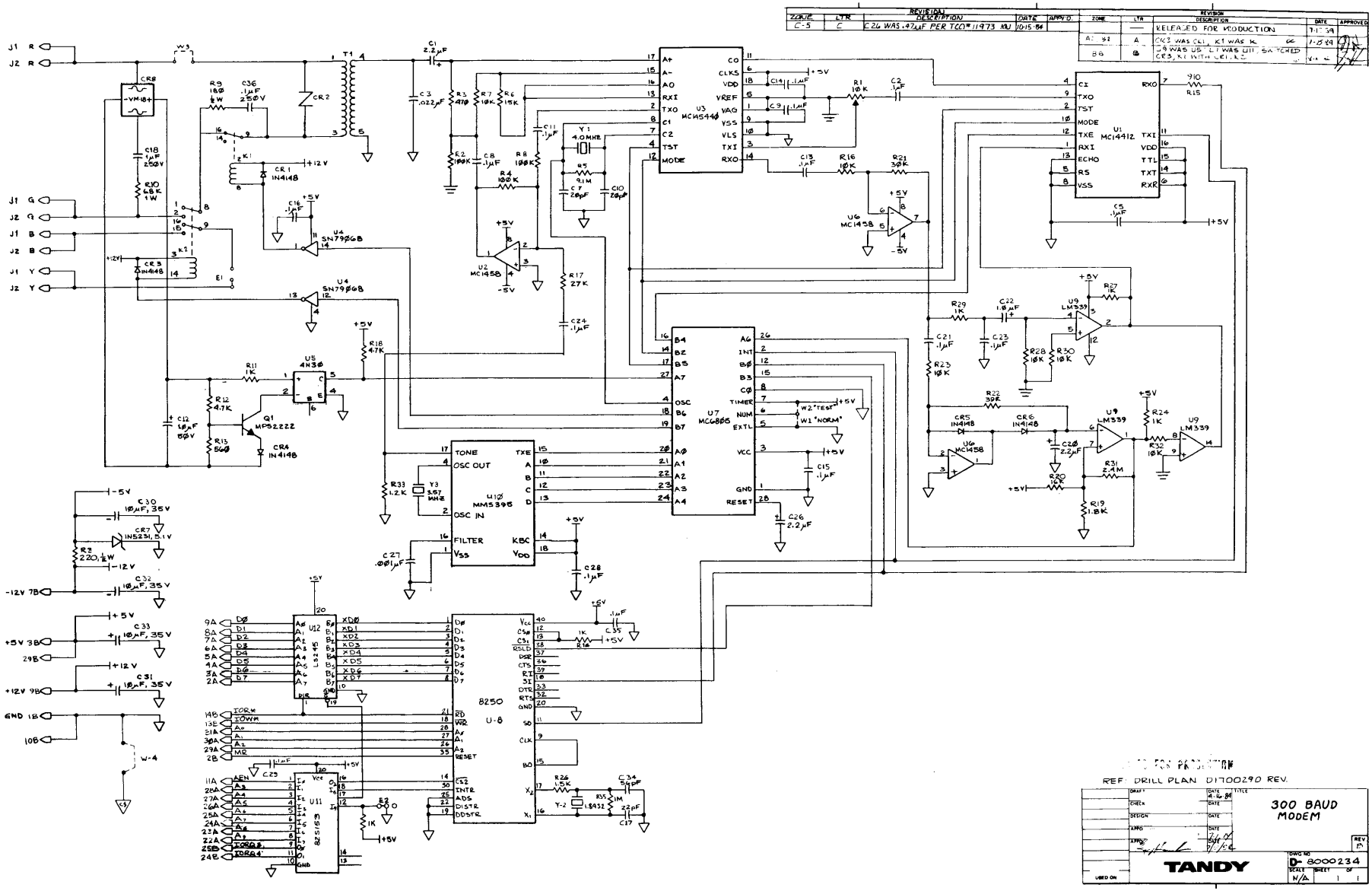
RS-232

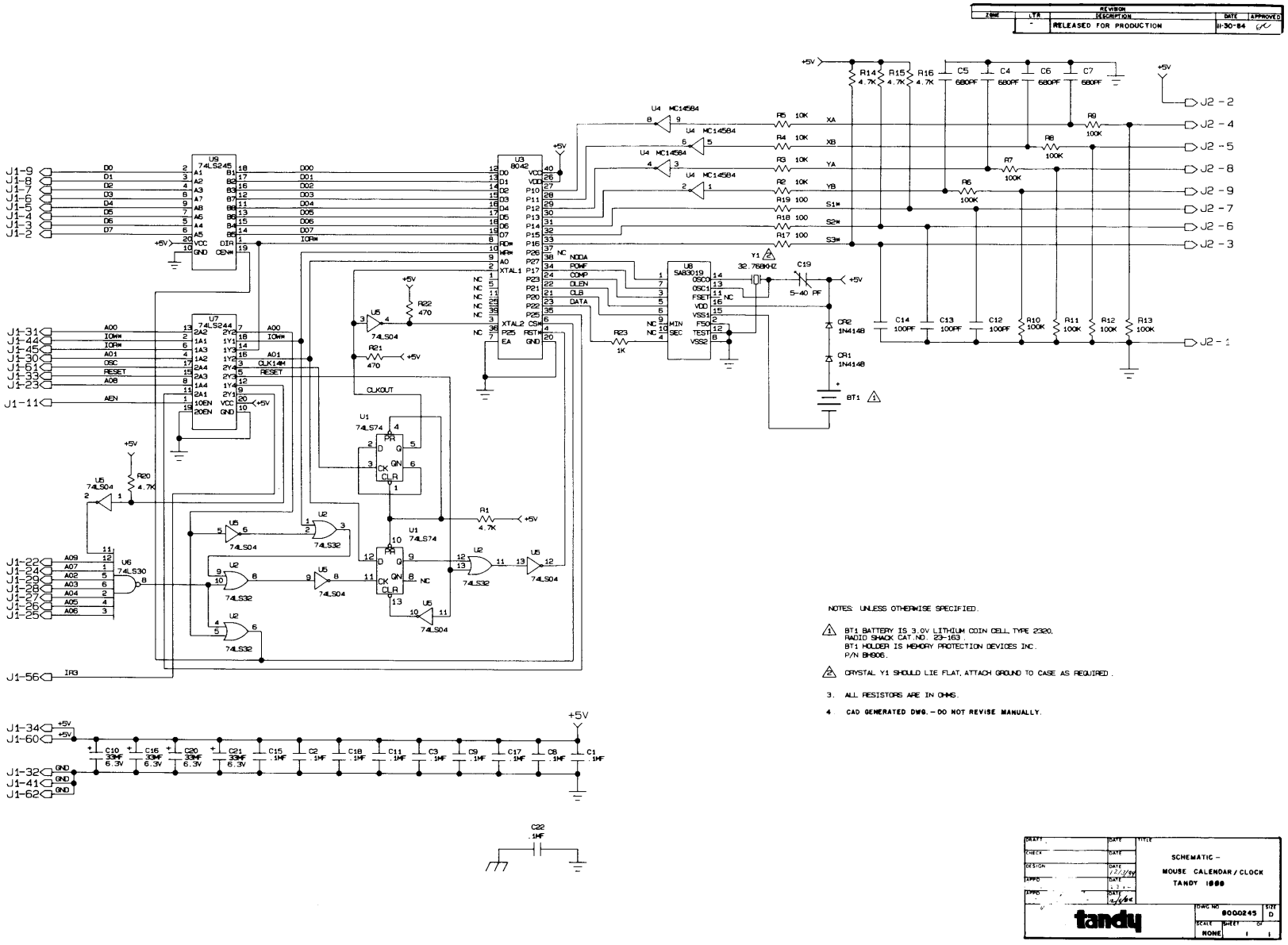
ZONE	LTR	REVISION DESCRIPTION	DATE	APPROVED
	-	RELEASED FOR PRODUCTION	11/5/84	DH
	A	ADDED BLOCK DH	1/28/85	



THIS IS A CADD GENERATED DRAWING - DO NOT CHANGE MANUALLY

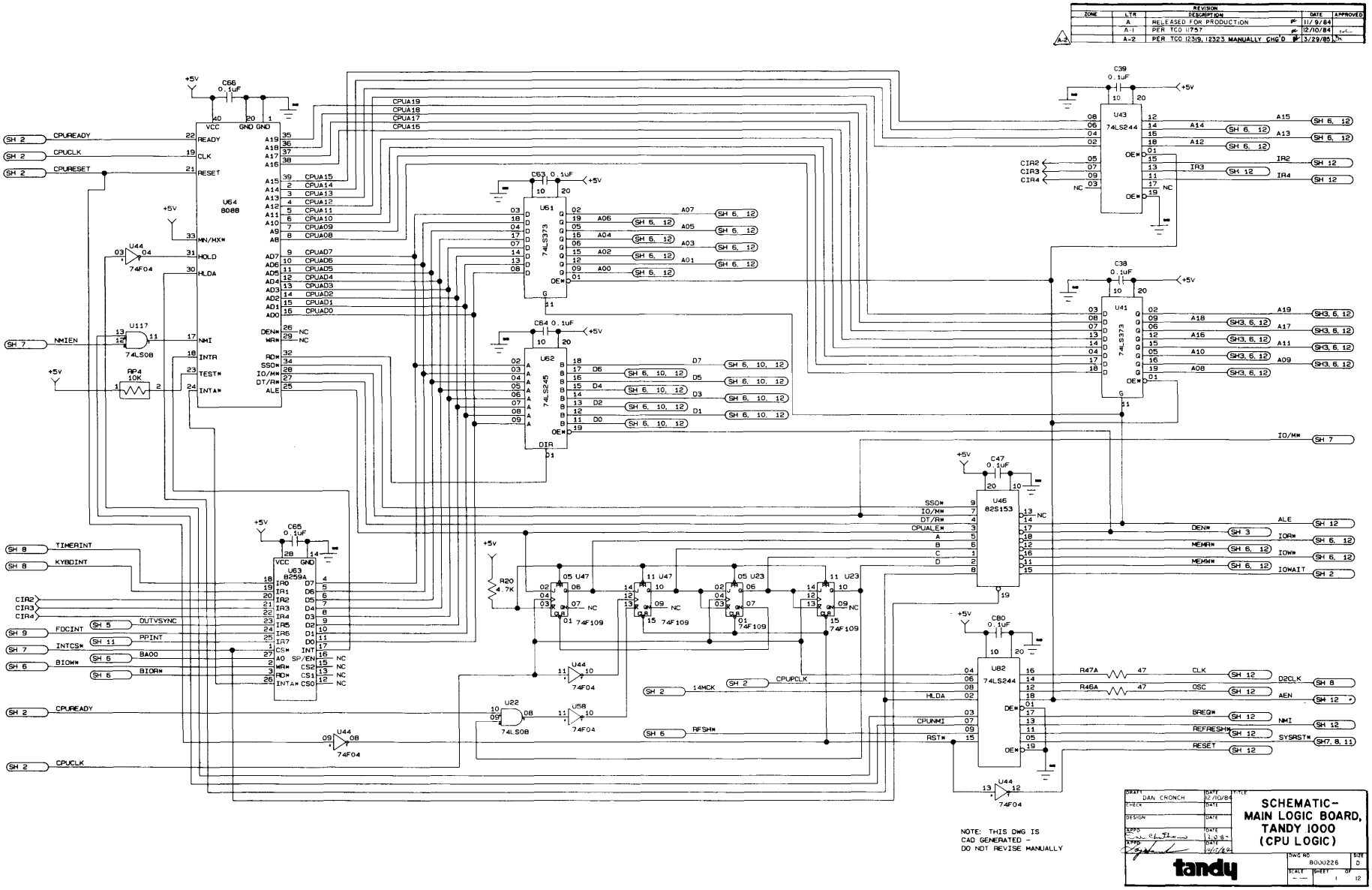
DRAFT DUNN	DATE 8-13-84	TITLE: SCHEMATIC - RS232 DOMESTIC PROJECT
CHECK	DATE	
	DATE 11-6-84	
	DATE 1-15-85	
APP	DATE 1/16/85	
tandy	DWG NO 8000235	SIZE D
	SCALE -	SHEET 1 OF 1

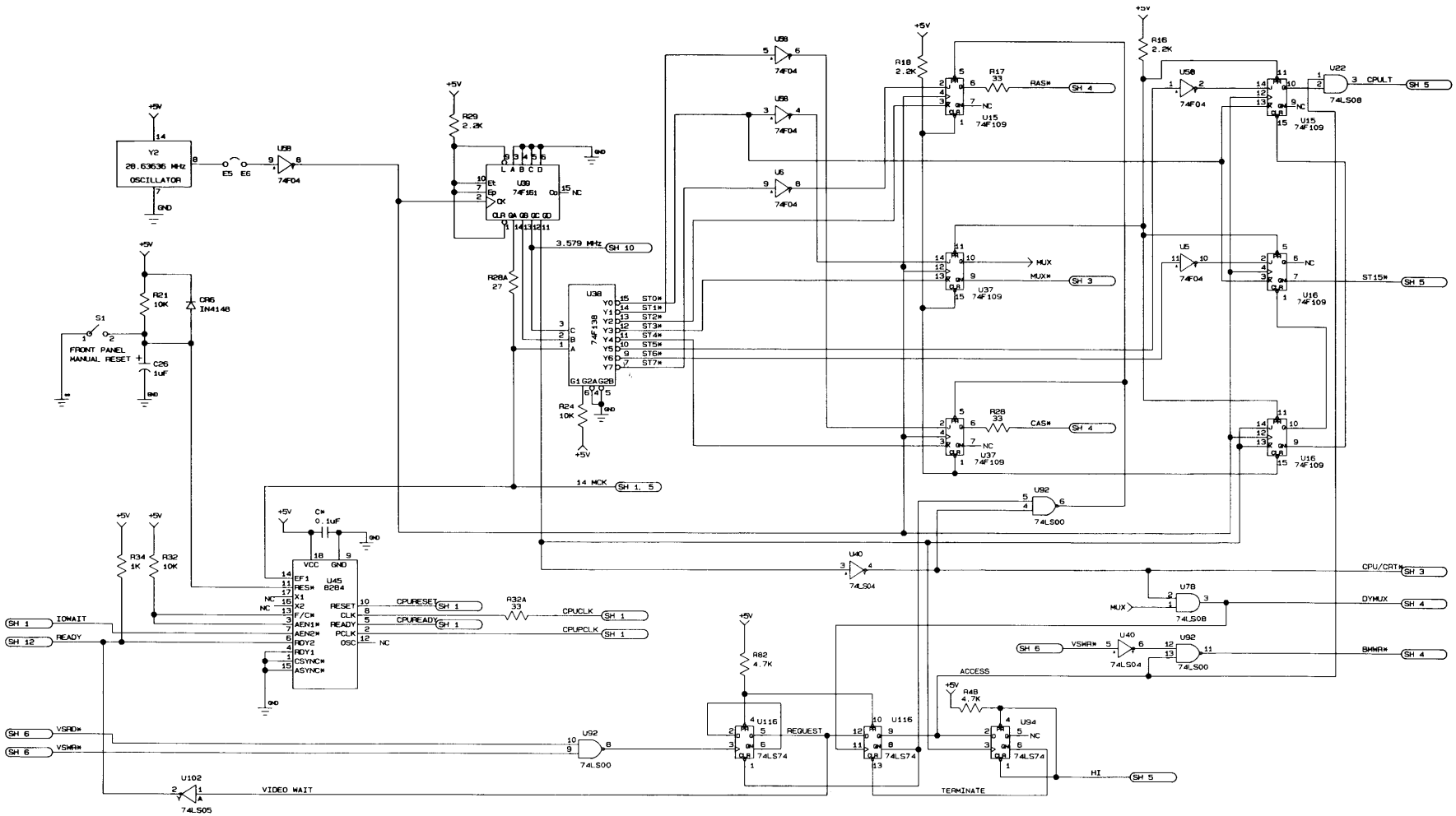

REVISIONS
ZONE LTR DESCRIPTION DATE APPVD
C-5 C C24 WAS .47µF PER TCO# 11973 MJ 10-15-84
REVISION
ZONE LTR DESCRIPTION DATE APPROVED
— — RELEASED FOR PRODUCTION 7-11-84
A-91 A C43 WAS C41, K1 WAS K 1-8-85
B-6 B C9 WAS U5 'L' WAS OUT, SA TCRED
CR3, K1 WITH LETTER
REF DRILL PLAN D1700290 REV.
300 BAUD MODEM
TANDY
D-8000234
SCALE N/A SHEET 1 OF 1
U1 MC14412
U3 MC14544Ø
U7 MC6885
U10 MM5395
U12 LS245
U11 8250
U-8
U2 MC1458
U6 MC1458
U9 LM339
U5 4N3Ø
Q1 MPS2222
CR1 IN4148
CR2
CR3 IN4148
CR4 IN4148
CR5 IN4148
CR6 IN4148
CR7 IN5231, 5.1V
SW4
Y1 4.Ø MHz
Y2 1.8432
Y3 3.57 MHz
J1 R
J2 R
J1 G
J2 G
J1 B
J2 B
J1 Y
J2 Y
-12V 7B
+5V 3B
29B
+12V 9B
GND 1B
10B

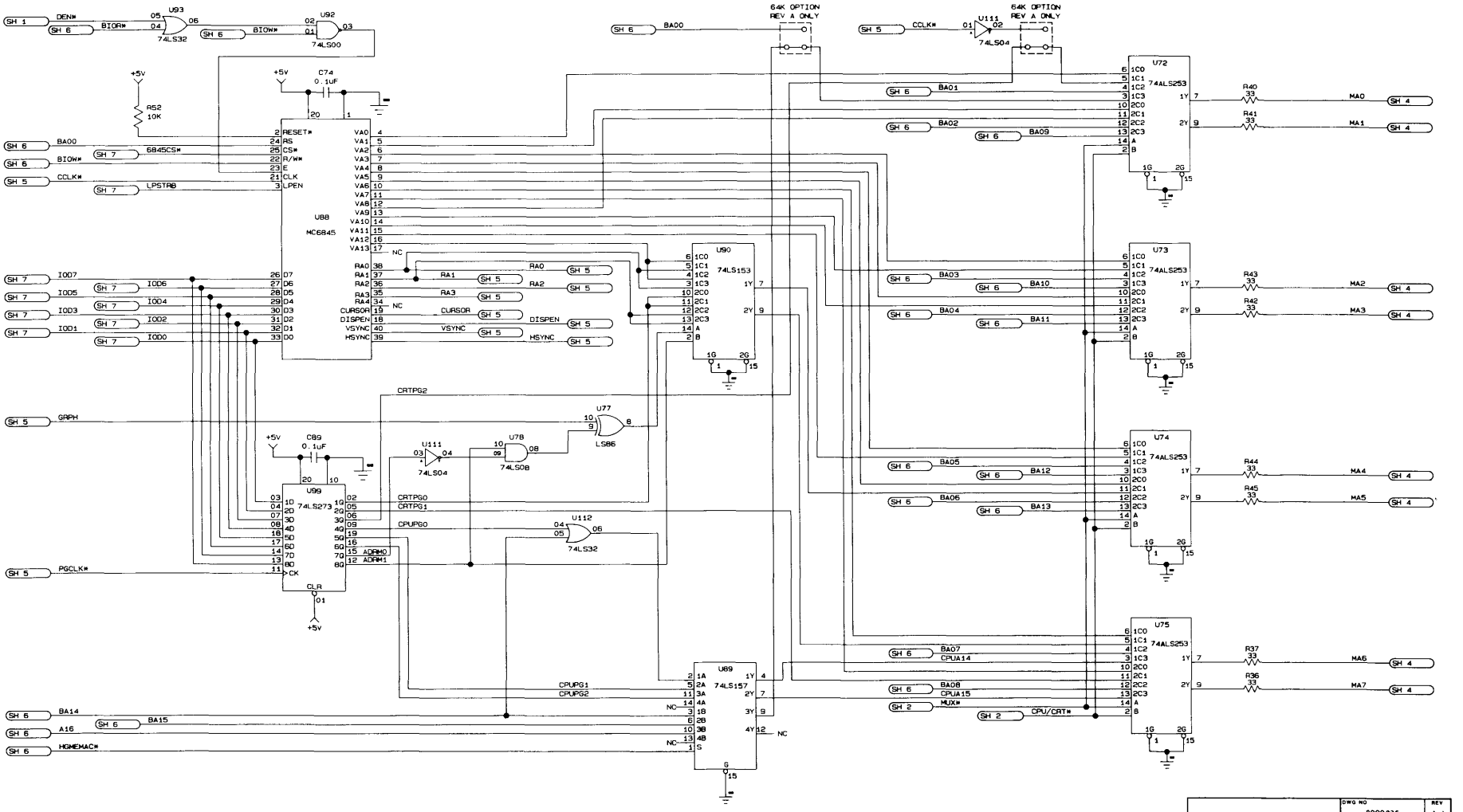

REVISION
ZONE LTR DESCRIPTION DATE APPROVED
- RELEASED FOR PRODUCTION 11-30-84
U3 8042
U4 MC14584
U5 74LS04
U6 74LS30
U7 74LS244
U8 SAB3019
U9 74LS245
U1 74LS74
U2 74LS32
Y1 32.7680-KZ
BT1
CR1 1N4148
CR2 1N4148
J1-9
J1-8
J1-7
J1-6
J1-5
J1-4
J1-3
J1-2
J1-31
J1-44
J1-45
J1-30
J1-51
J1-33
J1-23
J1-11
J1-22
J1-24
J1-29
J1-28
J1-27
J1-26
J1-25
J1-56
J1-34
J1-60
J1-32
J1-41
J1-62
J2 - 2
J2 - 4
J2 - 5
J2 - 8
J2 - 9
J2 - 7
J2 - 6
J2 - 3
J2 - 1
XA
XB
YA
YB
S1M
S2M
S3M
CLKOUT
IRQ
NOTES: UNLESS OTHERWISE SPECIFIED.
1. BT1 BATTERY IS 3.0V LITHIUM COIN CELL, TYPE 2320, RADIO SHACK CAT.NO. 23-163. BT1 HOLDER IS MEMORY PROTECTION DEVICES INC. P/N BH306.
2. CRYSTAL Y1 SHOULD LIE FLAT, ATTACH GROUND TO CASE AS REQUIRED.
3. ALL RESISTORS ARE IN OHMS.
4. CAD GENERATED DWG. - DO NOT REVISE MANUALLY.
SCHEMATIC - MOUSE CALENDAR/CLOCK TANDY 1000
tandy
DWG NO 8000245
SIZE D
SCALE NONE
SHEET 1 OF 1

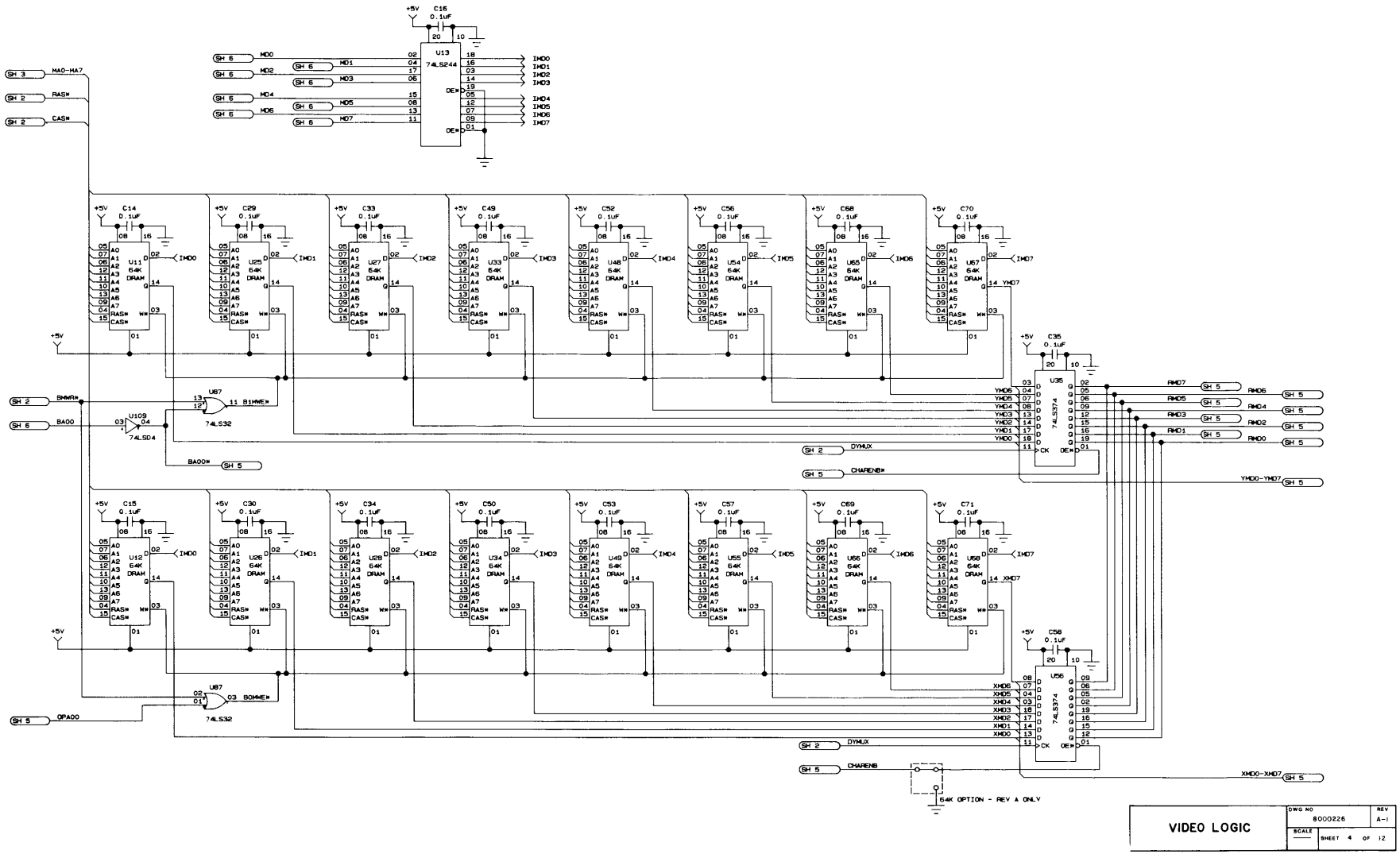
SCHEMATICS

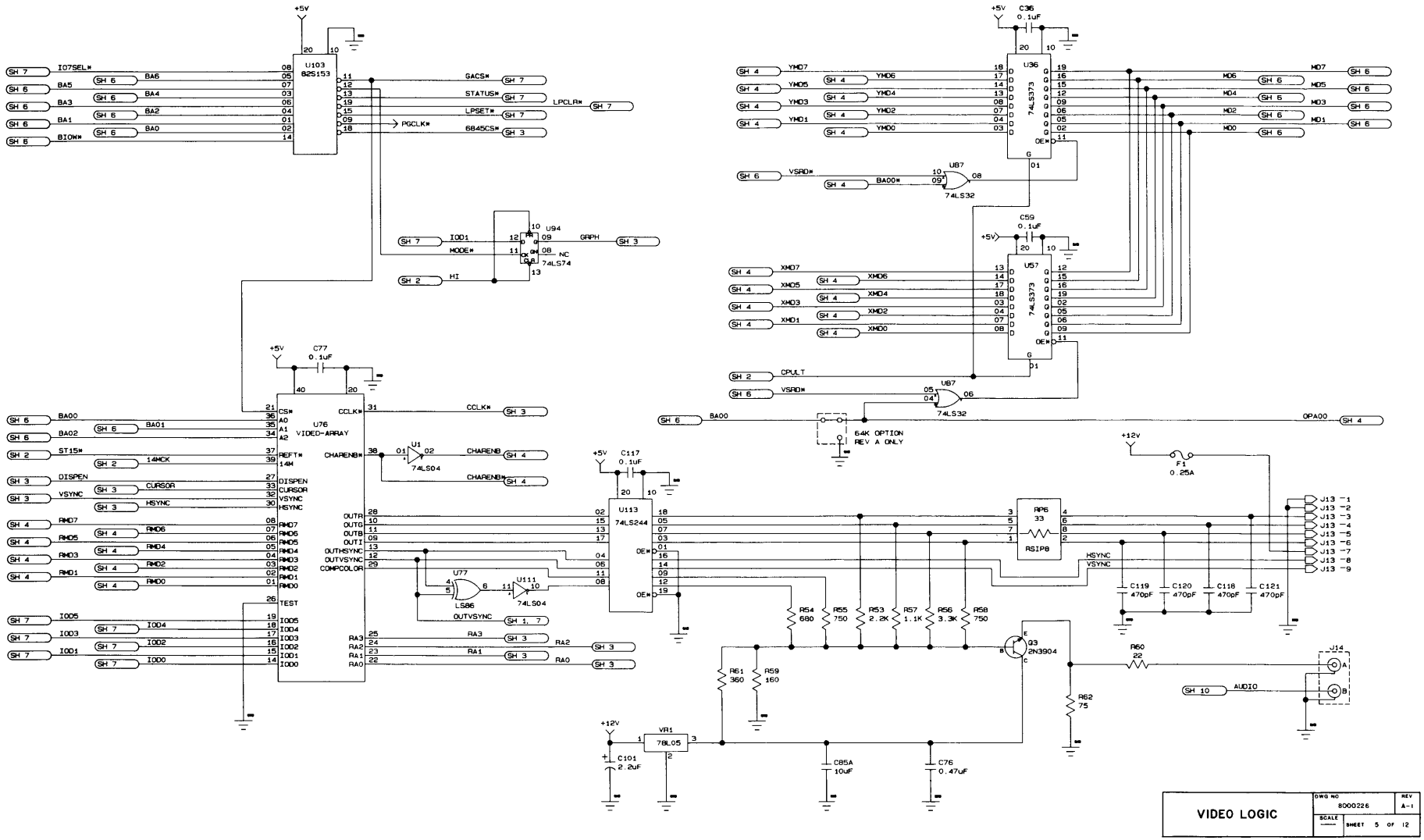
Main Logic

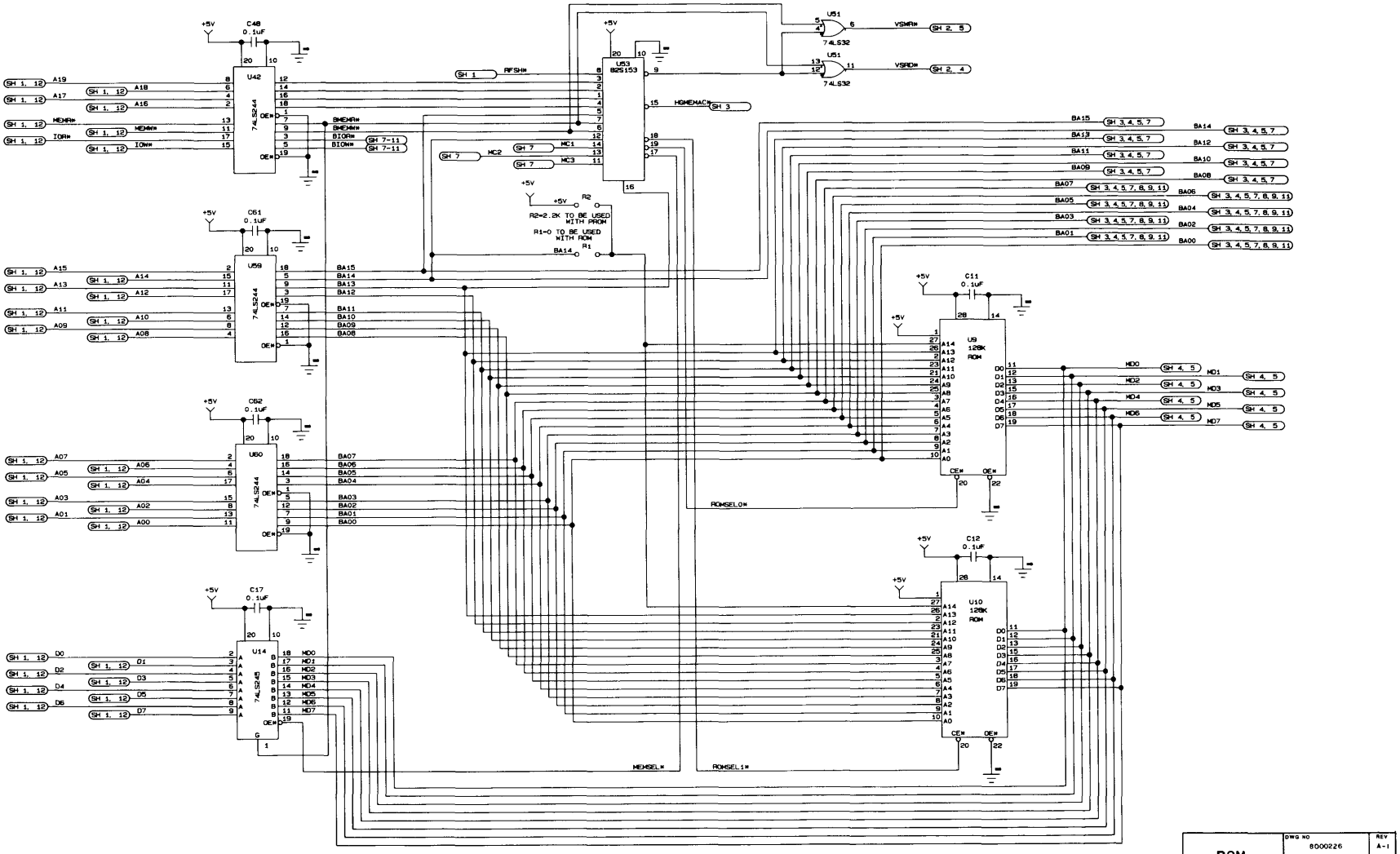


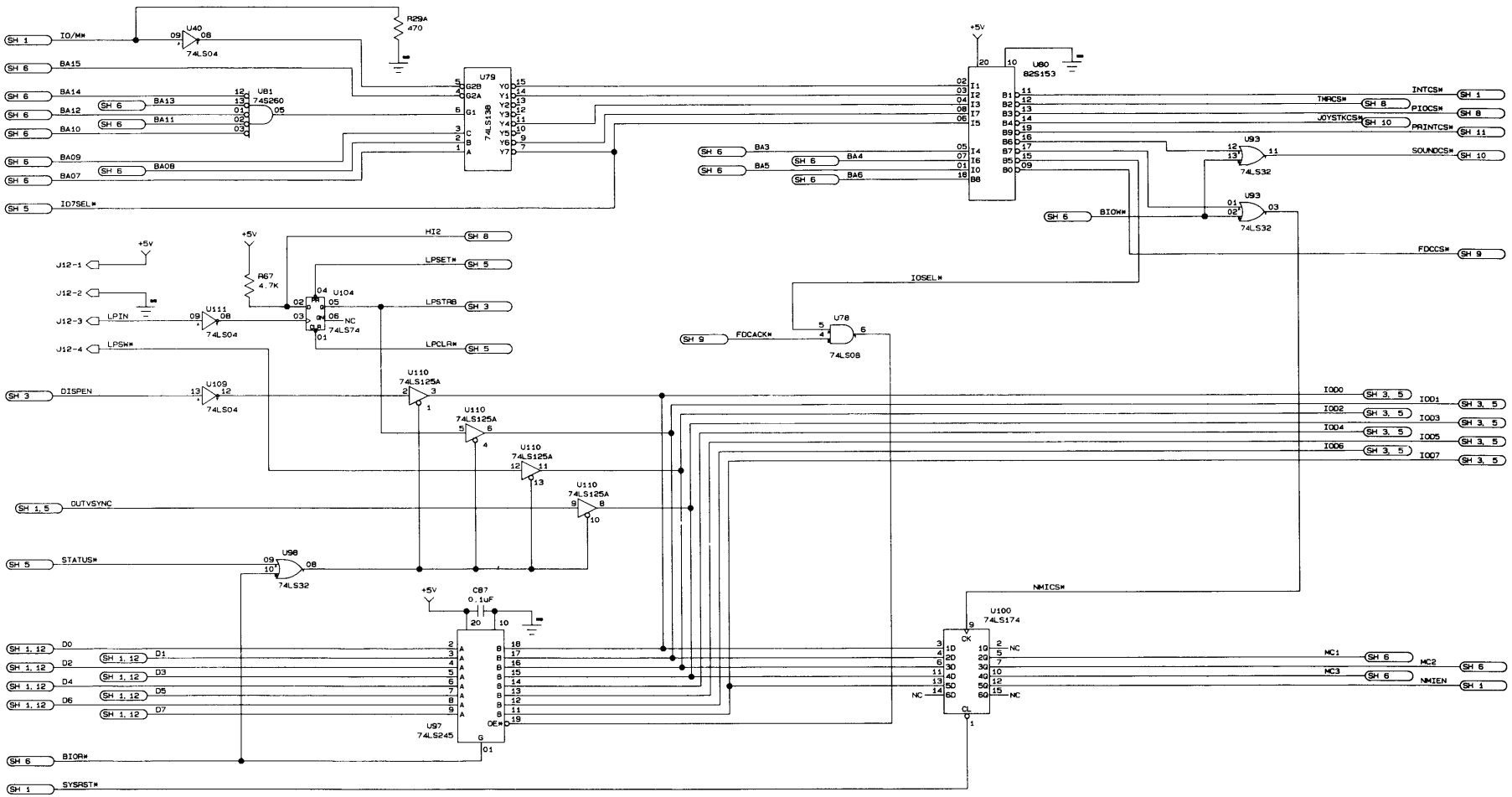

VIDEO LOGIC
DWG NO 8000226
REV A-1
SCALE
SHEET 2 OF 12
Y2
28.63636 MHz
OSCILLATOR
74F04
74F161
74F138
74F109
74LS08
74LS04
74LS00
74LS74
74LS05
R21 10K
CR6 IN4148
S1
FRONT PANEL MANUAL RESET
C26 1uF
R29 2.2K
R28A 27
R24 10K
R18 2.2K
R16 2.2K
R17 33
R28 33
R34 1K
R32 10K
C* 0.1uF
R32A 33
R82 4.7K
R48 4.7K
3.579 MHz
14 MCK
RAS*
CAS*
MUX
MUX*
ST15*
CPULT
CPU/CRT*
DYMUX
BMWR*
VSWR*
CPURESET
CPUREADY
CPUCLK
CPUPCLK
IOWAIT
READY
VSRD*
VSWR*
VIDEO WAIT
REQUEST
ACCESS
TERMINATE
HI
ST0*
ST1*
ST2*
ST3*
ST4*
ST5*
ST6*
ST7*

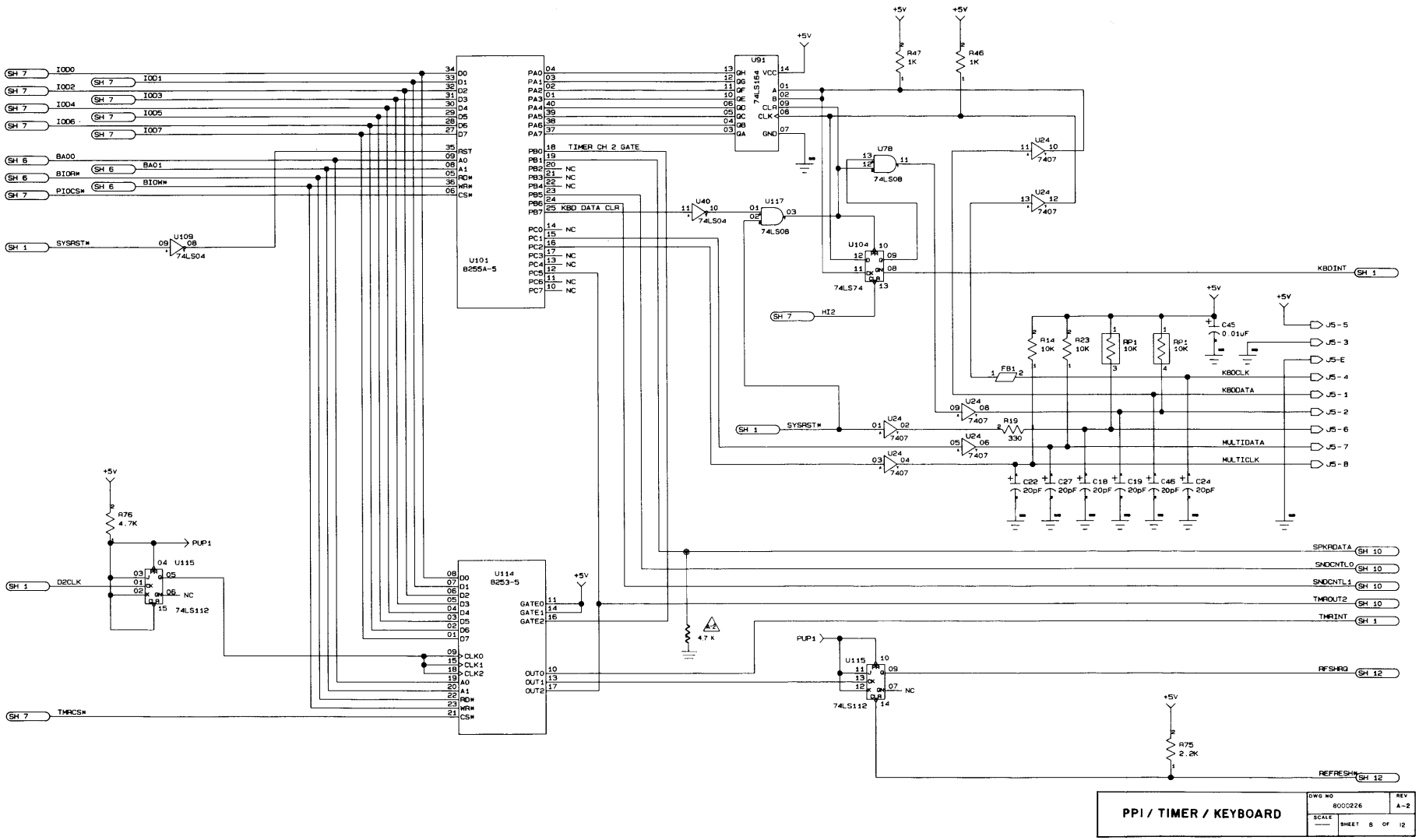

VIDEO LOGIC
DWG NO 8000226
REV A-1
SCALE
SHEET 3 OF 12

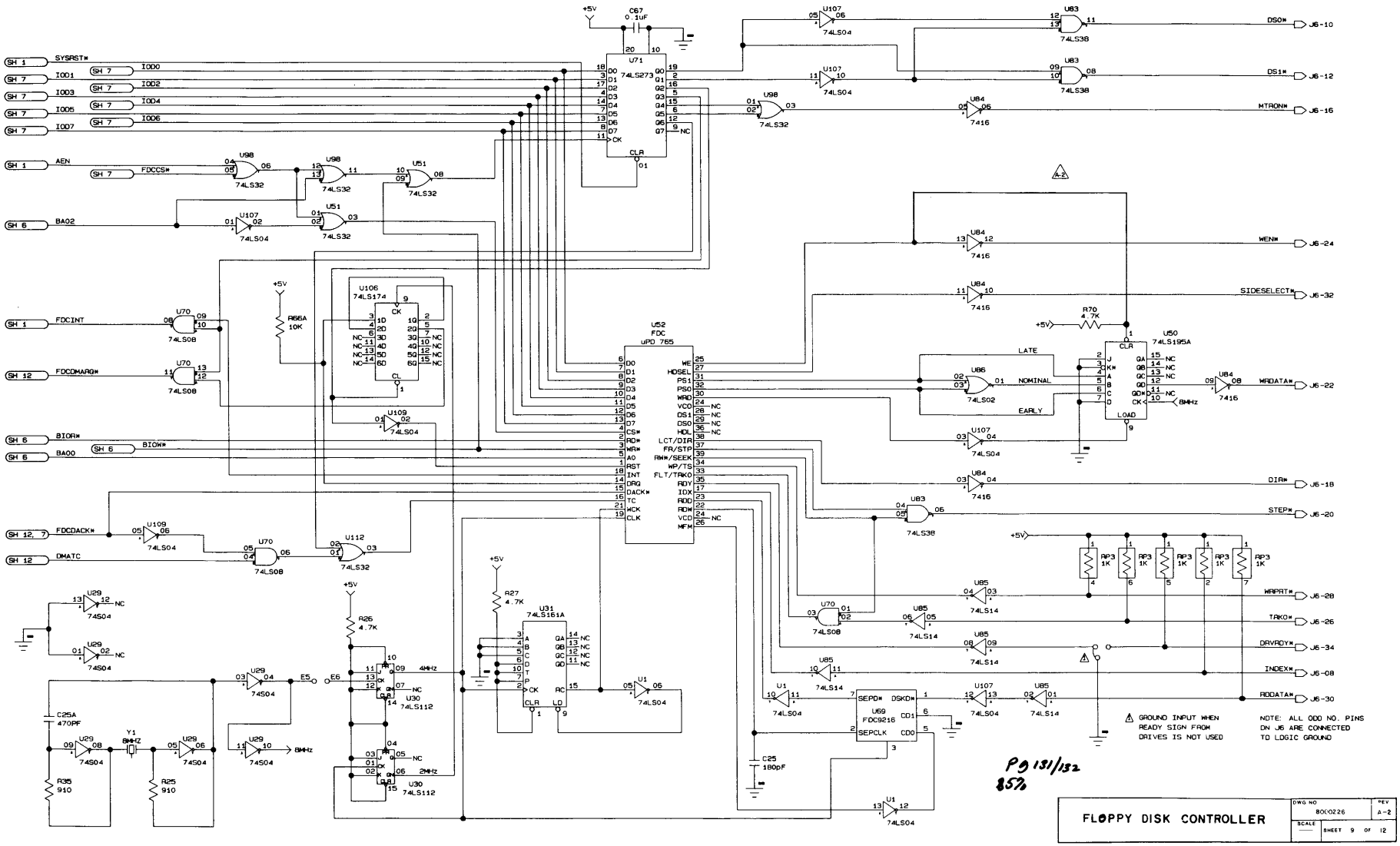

MA0-MA7
RAS#
CAS#
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
IMD0
IMD1
IMD2
IMD3
IMD4
IMD5
IMD6
IMD7
U13
74LS244
C16
0.1uF
C14
C29
C33
C49
C52
C56
C68
C70
U11
U25
U27
U33
U48
U54
U55
U67
64K DRAM
RAS#
CAS#
WR#
BMWR#
BA00
U87
74LS32
U109
74LS04
BA00#
B1MWE#
DYMUX
CHARENB#
C35
U35
74LS374
YMD0
YMD1
YMD2
YMD3
YMD4
YMD5
YMD6
YMD7
YMD0-YMD7
C15
C30
C34
C50
C53
C57
C69
C71
U12
U26
U28
U34
U49
U55
U66
U56
XMD0
XMD1
XMD2
XMD3
XMD4
XMD5
XMD6
XMD7
XMD0-XMD7
C58
OPA00
BOMWE#
CHARENB
64K OPTION - REV A ONLY
VIDEO LOGIC
DWG NO 8000226
REV A-1
SCALE —
SHEET 4 OF 12


VIDEO LOGIC
DWG NO 8000226
REV A-1
SCALE
SHEET 5 OF 12
U103 82S153
U76 VIDEO-ARRAY
U36 74LS373
U57 74LS373
U113 74LS244
U94 74LS74
U87 74LS32
U1 74LS04
U77 LS86
U111 74LS04
VR1 78L05
Q3 2N3904
RP6 33 RSIP8
F1 0.25A
64K OPTION REV A ONLY
IO7SEL*
BA6
BA5
BA4
BA3
BA2
BA1
BA0
BIOW*
GACS*
STATUS*
LPSET*
PGCLK*
6845CS*
LPCLR*
GRAPH
MODE*
HI
CCLK*
CHARENB*
14MCK
ST15*
DISPEN
CURSOR
VSYNC
HSYNC
RMD7
RMD6
RMD5
RMD4
RMD3
RMD2
RMD1
RMD0
TEST
IOD5
IOD4
IOD3
IOD2
IOD1
IOD0
OUTR
OUTG
OUTB
OUTI
OUTHSYNC
OUTVSYNC
COMPCOLOR
OUTVSYNC
RA3
RA2
RA1
RA0
YMD7
YMD6
YMD5
YMD4
YMD3
YMD2
YMD1
YMD0
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
VSRD*
BA00*
XMD7
XMD6
XMD5
XMD4
XMD3
XMD2
XMD1
XMD0
CPULT
BA00
OPA00
HSYNC
VSYNC
AUDIO
R54 680
R55 750
R53 2.2K
R57 1.1K
R56 3.3K
R58 750
R61 360
R59 160
R60 22
R62 75
C119 470pF
C120 470pF
C118 470pF
C121 470pF
C85A 10uF
C76 0.47uF
C101 2.2uF
C77 0.1uF
C117 0.1uF
C36 0.1uF
C59 0.1uF
+5V
+12V

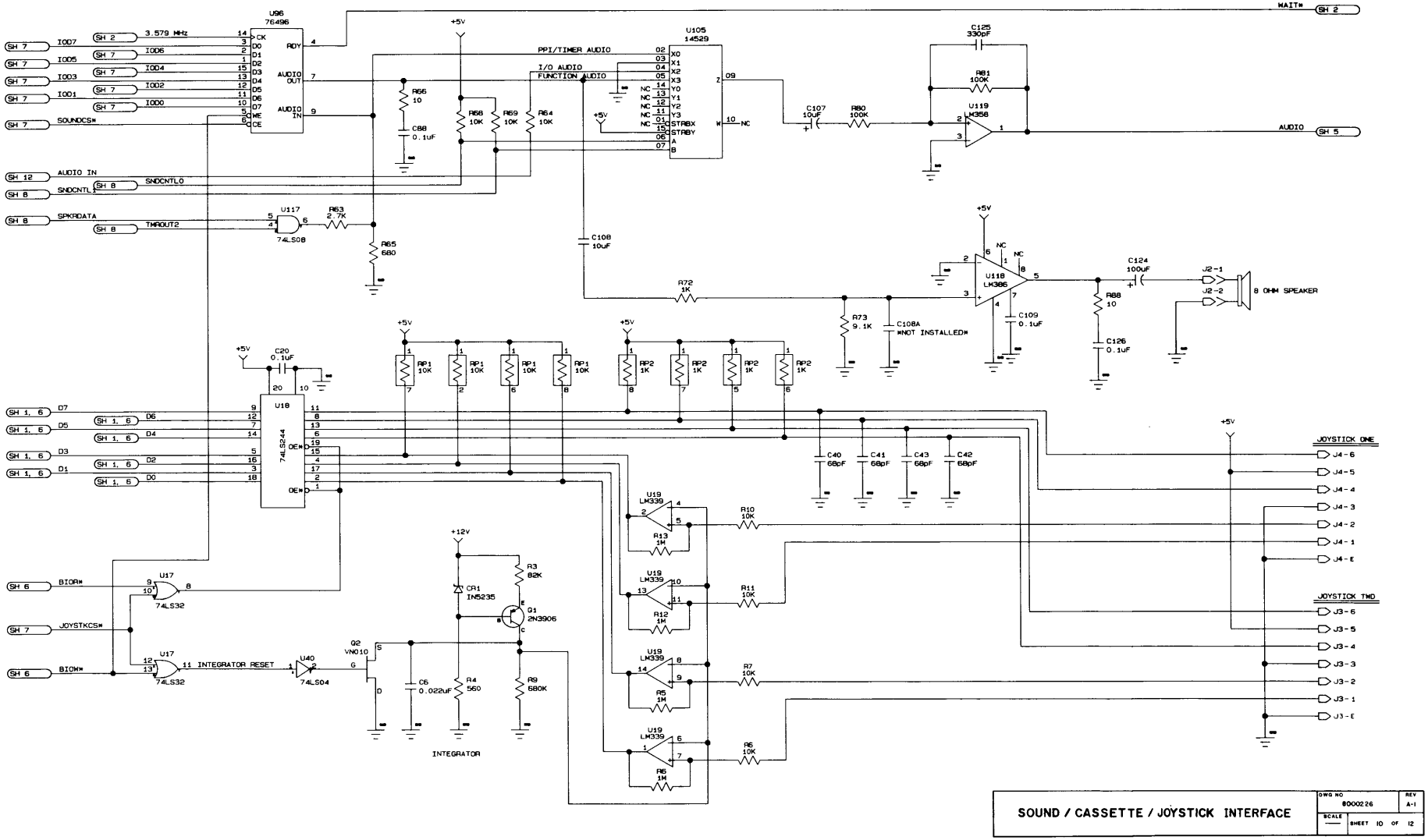

ROM
DWG NO 8000226
REV A-1
SCALE —
SHEET 6 OF 12

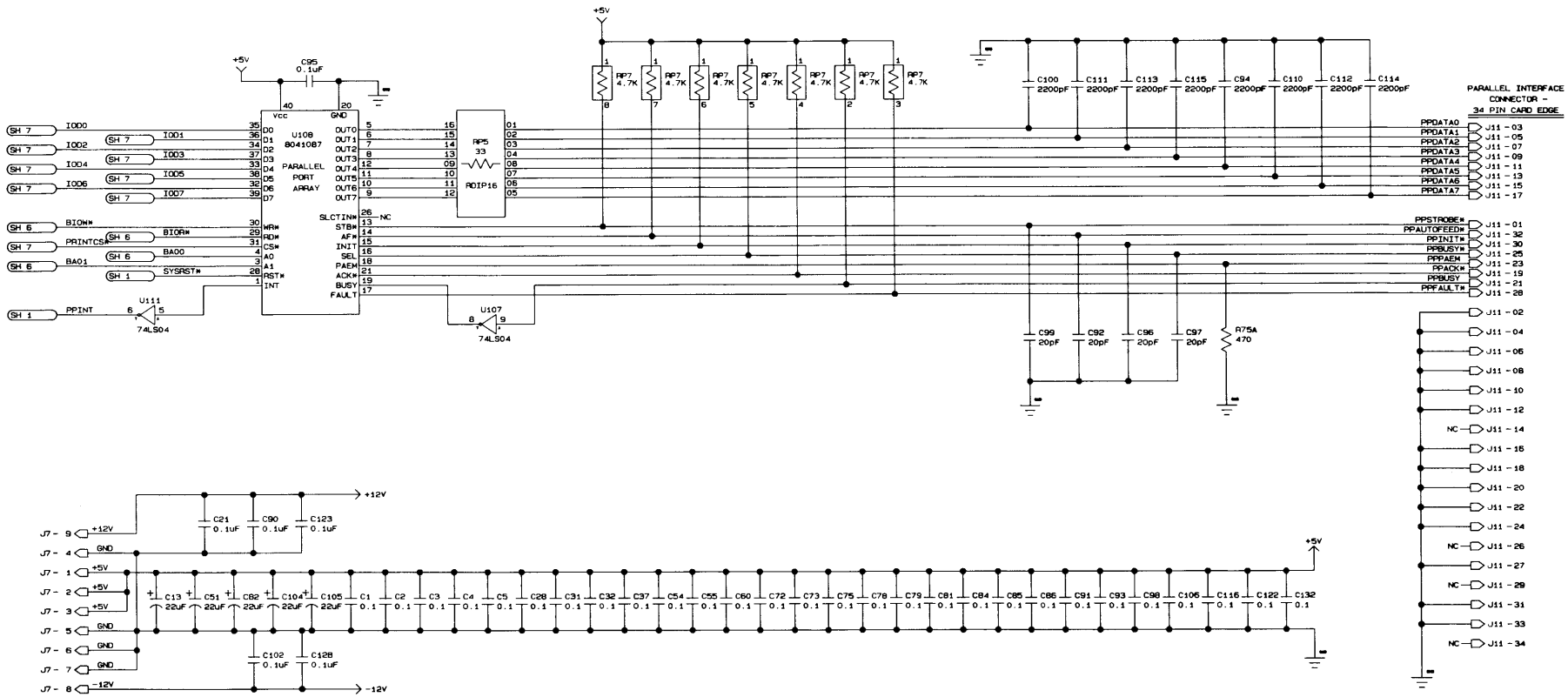

I/O BUS INTERFACE
DWG NO 8000226
REV A-1
SCALE —
SHEET 7 OF 12

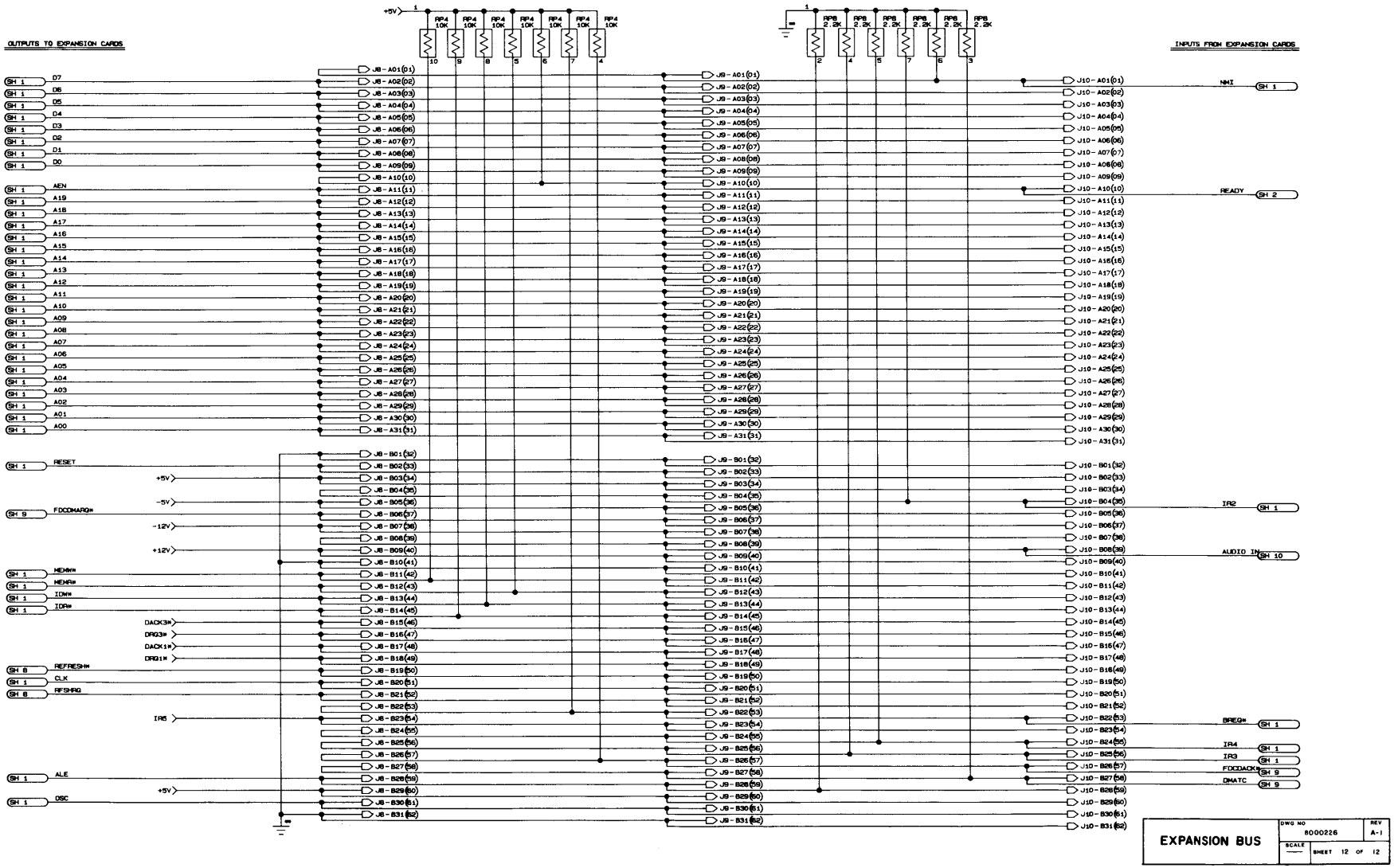

PPI / TIMER / KEYBOARD
DWG NO 8000226
REV A-2
SCALE
SHEET 8 OF 12
U101 8255A-5
U114 8253-5
U91 74LS164
U109 74LS04
U40 74LS04
U117 74LS08
U78 74LS08
U104 74LS74
U115 74LS112
U24 7407
R47 1K
R46 1K
R76 4.7K
R75 2.2K
R19 330
RP1 10K
RP2 10K
R14 10K
R23 10K
C45 0.01uF
C22 20pF
C27 20pF
C18 20pF
C19 20pF
C46 20pF
C24 20pF
FB1
TIMER CH 2 GATE
KBD DATA CLR
SYSRST*
HI2
D2CLK
TMRCS*
KBDINT
KBDCLK
KBDDATA
MULTIDATA
MULTICLK
SPKRDATA
SNDCNTL0
SNDCNTL1
TMROUT2
TMRINT
RFSHRQ
REFRESH*
J5-5
J5-3
J5-E
J5-4
J5-1
J5-2
J5-6
J5-7
J5-8
IOD0
IOD1
IOD2
IOD3
IOD4
IOD5
IOD6
IOD7
BA00
BA01
BIOR*
BIOW*
PIOCS*


SYSRST*
IOD0
IOD1
IOD2
IOD3
IOD4
IOD5
IOD6
IOD7
AEN
FDCCS*
BA02
FDCINT
FDCDMARQ*
BIOR*
BIOW*
BA00
FDCDACK*
DMATC
U52
FDC
uPD 765
U71
74LS273
U106
74LS174
U31
74LS161A
U30
74LS112
U59
FDC9216
U50
74LS195A
C67
0.1uF
C25A
470PF
C25
180pF
Y1
8MHz
R35
910
R25
910
R26
4.7K
R27
4.7K
R70
4.7K
R86A
10K
RP3
1K
DSO* J6-10
DS1* J6-12
MTRON* J6-16
WEN* J6-24
SIDESELECT* J6-32
WRDATA* J6-22
DIR* J6-18
STEP* J6-20
WRPRT* J6-28
TRK0* J6-26
DRVRDY* J6-34
INDEX* J6-08
RDDATA* J6-30
LATE
NOMINAL
EARLY
LOAD
4MHz
2MHz
8MHz
GROUND INPUT WHEN READY SIGN FROM DRIVES IS NOT USED
NOTE: ALL ODD NO. PINS ON J6 ARE CONNECTED TO LOGIC GROUND
FLOPPY DISK CONTROLLER
DWG NO 8000226
REV A-2
SCALE
SHEET 9 OF 12

Pg 131/132
85%


SOUND / CASSETTE / JOYSTICK INTERFACE
DWG NO 8000226
REV A-1
SCALE
SHEET 10 OF 12
U96 76496
U105 14529
U118 LM386
U119 LM358
U117 74LS08
U18 74LS244
U19 LM339
U17 74LS32
U40 74LS04
Q2 VN010
Q1 2N3906
CR1 IN5235
3.579 MHz
PPI/TIMER AUDIO
I/O AUDIO
FUNCTION AUDIO
AUDIO IN
SNDCNTL0
SPKRDATA
TMROUT2
INTEGRATOR RESET
INTEGRATOR
8 OHM SPEAKER
JOYSTICK ONE
JOYSTICK TWO
WAIT*
AUDIO
+5V
+12V


PARALLEL PRINTER INTERFACE
DWG NO 8000226
REV A-1
SCALE
SHEET 11 OF 12


OUTPUTS TO EXPANSION CARDS
INPUTS FROM EXPANSION CARDS
+5V
RP4 10K
RP8 2.2K
D7
D6
D5
D4
D3
D2
D1
D0
AEN
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A09
A08
A07
A06
A05
A04
A03
A02
A01
A00
RESET
+5V
-5V
FDCDMARQ#
-12V
+12V
MEMW#
MEMR#
IOW#
IOR#
DACK3#
DRQ3#
DACK1#
DRQ1#
REFRESH#
CLK
RFSHRQ
IRQ
ALE
+5V
OSC
NMI
READY
IRQ2
AUDIO IN
BREQ#
IRQ4
IRQ3
FDCDACK#
DMATC
EXPANSION BUS
DWG NO 8000226
REV A-1
SCALE
SHEET 12 OF 12

RADIO SHACK, A DIVISION OF TANDY CORPORATION

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CANADA: BARRIE, ONTARIO L4M 4W5

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